SECTION II

CIRCUIT DESCRIPTION

2.1 GENERAL

The operation of the VLF receiver is discussed using the functional block diagrams, Figures 2-1 and 2-2, and the schematic diagrams at the rear of this manual. In the functional analysis which follows, operation of the receiver and the frequency display will be discussed separately. Note that the unit numbering system is used for electrical components. This means that parts on subassemblies and plug-in modules carry a prefix before the usua class letter and number of the item (such as A1C1 and A2R2). These subassembly prefixes are omitted in the text and on illustrations except in those cases where confusion might result from their omission.

2.2 FUNCTIONAL ANALYSIS, RECEIVER

The VLF receiver is an all-solid state superheterodyne covering the frequency range of 1 to 600 kHz in on band. AM, CW, SSB, FSK, or MCW signals may be received. Four IF bandwidths are provided: 150 Hz, 1 kHz, 3 and 6 kHz. A direct-reading digital readout is used which makes it possible to read the frequency to which the receiver is tuned within 10 Hz. By using the receiver's DAFC circuit the local oscillator can be locked to any frequency within the tuning range and maintained within 10 Hz of the desired frequency for an indefinite period. The functional operation of the digital readout counter assembly and the DAFC circuit is discussed in paragraph 2.3.

2.2.1 Input signals to the receiver are applied to an input transformer which has a tapped primary to provide input impedances of 50 ohms or 1000 ohms. A rear-panel switch is used to select the proper impedance for the antenna being used. From the transformer the signal is passed through a bandpass filter which prevents signals outside the receiver's tuning range from entering the RF circuits. The filter has a pass band extending from 500 Hz to 603 kH A variable attenuator is connected between the filter and input amplifier. It prevents strong signals from overloadi the receiver. The input signal may be attenuated by a factor of 0, -20, -40, or -60 dB.

2.2.2 The incoming signal is next fed to a two-stage, untuned wideband amplifier made up of transistors A3A1Q1 and A3A1Q2. After amplification the input signal is passed through emitter follower A3A1Q3 to a balanced mixer where it is beat with the local oscillator signal. The 2-MHz difference frequency which results from the mixing action is then fed to the noise IF and gate assembly. A push-pull RF amplifier, A3A1Q4 and A3A1Q5, amplifies the local oscillator signal to drive the balanced mixer.

2.2.3 The balanced mixer output is fed to both signal and noise IF amplifier circuits in the noise IF and gate assen If the NOISE CANCELLER THRESHOLD control is in the OFF position the noise IF amplifier is de-energized and th noise gate is closed so that signals can pass. Thus, the amplified 2-MHz output from the signal IF amplifier, A5A2Q1, is passed through the gate to the IF and BFO assembly, A5. Rotating the NOISE CANCELLER THRESHOL control from the OFF position energizes the noise IF amplifier which controls the noise gate. Noise spikes above a level determined by the threshold control cause the gate to open before signals can pass out, thus blocking both the noise and signal at this point. This is made possible by using a relatively wide bandwidth for the noise IF amplifier and using a tunnel diode to trigger the gate pulse generator, A12A2Q2. The wider bandwidth of the noise IF amplifier permits the rise time of noise pulses to exceed that of the same pulses passing through the signal IF amplifier, A12A2Q1. This faster pulse rise time, combined with the extremely fast switching time of the tunnel diode, results in a gate pulse which opens the gate before the signal IF output can pass through. Note that the noise IF amplifier i gain controlled by its own AGC amplifier circuit.

2.2.4 The 2-MHz output from the noise gate is amplified by IF stages A5A1Q1 and A5A1Q2, and applied in parallel to transistors A5A1Q3 through A5A1Q6, which function as switches, and to the SM OUTPUT jack. Depending on the position of the IF BANDWIDTH switch one of the switch transistors will be energized, so that the signal passes through it and into the associated bandwidth filter. Crystal filters are used to determine all four IF bandwidths. Emitter follower stages A5A2Q1 through A5A2Q4 are also controlled by the IF BANDWIDTH switch. The outputs of all four stages are connected in parallel. The proper stage is energized to pass the filter output on to the following IF amplifier stages. There are four additional IF amplifier stages before the AM detector, A5A3Q1 through A5A3Q The IF signal is also taken at the output of A5A3Q4 and fed to the BFO product detector and to the IF OUTPUT jack. The AM detector provides the input to the AGC amplifier, and with the BFO off, the input to the audio amplifier.

2.2.5 The frequency of the local oscillator, A4A1Q1, is maintained 2 MHz above the frequency to which the receiver is tuned. The output signal from the oscillator is fed to two paralleled limiters, A4A1Q2-Q3 and A4A1Q6-Q7. Limiters are used to square the sinusoidal oscillator signal to produce a square wave output. The output from the limiters is fed to identical complementary symmetry amplifiers. The output from A4A1Q4-Q5 is used as the switching voltage for the diodes in the balanced mixer. By using a square wave for switching, intermodulation products inherent in the mixing process are minimized. The output from A4A1Q8-Q9 is fed to the counter assembly and to the rear-panel LO OUTPUT jack.

2.2.6 There are five separate beat frequency oscillators. The desired one is energized by the BFO switch. With a BFO operating the input to the audio amplifier is switched from the AM detector to the BFO balanced mixer and the AGC circuit is defeated, even if the function switch is in the AGC position. Thus the gain of the receiver must be manually controlled when the BFO switch is moved from the OFF position. The variable frequency BFO, A5A4Q1, may be shifted in frequency ±7 kHz each side of the 2-MHz center frequency. Its output is fed through buffer-amplifier stage A5A4Q5 to the product detector where it is heterodyned with the output of IF amplifier stage A5A3Q4. The difference frequency which results is fed to the audio amplifier. The four other beat frequency oscillators are crystal controlled. When used, the output of the one selected is fed through an additional buffer stage, A5A4Q4, before being applied to A5A4Q5. This buffer isolates the variable frequency oscillator from the crystal oscillators to prevent it from locking on a crystal frequency when tuned past one. The crystal-controlled beat oscillators provide upper or lower sideband reception of SSB signals (depending on the sideband transmitted) when used with the 3-kHz IF bandwidth, give a 2-MHz output to zero beat with the IF frequency, and a signal to provide a 5.5-kHz beat note.

2.2.7 With the IF GAIN control in the AGC position, and the BFO off, receiver gain is controlled by the signal AGC amplifier. AGC action begins when the input signal attains an approximately 10-dB (s plus n)/n ratio at the receiver's output. Until this signal level is attained the receiver operates at maximum gain. Input to the AGC amplifier is from the AM detector. The AGC circuit consists of an input emitter follower, A6Q1, a dc amplifier, A6Q3, and the AGC regulator, A6Q2. The AGC regulator is connected in series with the +12 volt supply and the base bias circuits of A5A1Q1, A5A1Q2, and A5A3Q1. Once AGC action begins, as the output from the AM detector becomes more positive with increasing signal strength, the output from the AGC regulator becomes less positive, decreasing the gain of the gain-controlled stages. If the IF GAIN control is moved from the AGC position, or if the BFO is turned on, the receiver gain is manually controlled by the IF GAIN control. This control varies the base bias of the same two stages controlled by the AGC amplifier. Transistor A6Q4 functions as a driver for the signal strength meter. Its input is derived from A6Q1. When the BFO switch is moved from the OFF position the output of A6Q1 is passed through a fast attack, slow decay network which decreases the sensitivity of the signal strength meter to the on-off characteristics of CW signals. This is to make the response of the meter to CW signals closely resemble the response to AM signals.

2.2.8 The noise IF amplifier AGC circuit is energized only when the NOISE CANCELLER THRESHOLD control is moved from the OFF position. It consists of A6Q5 and A6Q6 which control the gain of all four noise IF amplifier stages. These stages operate as described above for A6Q2 and A6Q3, except they have a much faster response time to maintain a constant input to the noise AGC detector, A12A1CR2, which provides the input to the noise AGC amplifier.

2.2.9 Separate audio amplifiers are used for the 600-ohm balanced output and to feed the front-panel PHONES jack. Both share a common input emitter follower, A7Q1. The input to the module is from the AM detector when the BFO is off, and from the BFO balanced mixer when the BFO is on. With the AUDIO BW switch in the NORMAL position, the output is applied directly to the two audio amplifier circuits. Placing the switch in the NARROW position routes the output of A7Q1 through a filter which restricts the audio bandwidths to 350 Hz (825 to 1175 Hz). The front-panel AUDIO GAIN control adjusts the volume at the PHONES jack only. A potentiometer on the audio amplifier module is used to set the level at the 600-ohm balanced output. The amplifier supplying this output contains a voltage amplifier, A7Q2, an emitter follower, A7Q4, used for impedance matching, and an output power amplifier, A7Q6. The headphones amplifier uses a two-stage circuit consisting of A7Q3 and A7Q5.

2.2.10 All receiver circuits operate from +12 or -12 Vdc. The +200, +4.5, and -4.5 Vdc outputs from the power supply are used by the counter assembly. Input power may be 115 or 230 Vac, 50-400 Hz. Power consumption is approximately 25 watts.

2.3 FUNCTIONAL ANALYSIS, FREQUENCY DISPLAY AND DAFC

The frequency display and DAFC circuit consists of the counter assembly, A11, and the +200, +4.5, and -4.5 Vdc power supplies. It displays the frequency to which the receiver is tuned by counting the local oscillator frequency and automatically subtracting the IF frequency. The frequency is normally displayed with an accuracy of ±100 Hz; however, by placing the MODE switch in either Decimal Shift positions the display is expanded by a factor of 10 so that the accuracy increases to ±10 Hz. When the decimal shift function is not used the oscillator frequency is counted for precisely controlled 10-millisecond intervals and displayed 50 times per second. Thus the display appears continuous and without flicker. Use of the decimal shift function increases the counting interval to 100 ms and decreases the display to five times per second. Under these conditions flicker is quite evident. In the function description of the frequency display which follows it will be assumed that the Decimal Shift mode is not used unless specifically noted. The DAFC circuit is in an encapsulated module which is a part of the counter assembly. Extensive use is made of integrated circuits (IC) in the counter assembly to minimize size and increase reliability. Figure 2-2 is the functional block diagram for the frequency display and DAFC.

2.3.1 Gating pulses are derived from the 1-MHz oscillator, A1Q1. A variable capacitor in series with the crystal is used to set the oscillator frequency at exactly 1 MHz by zero beating with WWV. The oscillator output is a train of positive pulses at a 1-MHz rate. The pulse train is fed through five IC decade scalers (counters which count to 10 and then reset) in series (A1Z1 through A1Z5) which divides the 1-MHz frequency by a factor of 10,000 or 100,00 Thus the output frequency from A1Z4 is 100 Hz and 10 Hz from A1Z5. The output from both these ICs is fed to secti S1A-W of the MODE switch. When the switch is in either of the NORMAL DISPLAY positions the output of A1Z4 is passed to the level shifter, A1Q3-Q7, and the 100-Hz pulse train is used to control the gating, reset, and display functions of the counter assembly. Placing the MODE switch in either of the DECIMAL SHIFT positions results in the 10-Hz output of A1Z5 controlling these functions.

2.3.2 The level shifter (A1Q3-Q7) performs two functions: it shifts the level of the output pulses from the ICs fron approximately 2 volts to 6 volts to operate subsequent discrete component circuits, and it provides both an output pulse and its complement. Complementary pulses are not available from the ICs. The "eight" output pulse from the level shifter switches flip-flop A2Q1-Q2 which directly controls the gate transistor, A2Q10. It is A2Q10 which permits, or cuts off, the local oscillator signal flow into the counter by cutting Schmitt trigger A2Q9-Q11 on and off Flip-flop A2Q3-Q4 is triggered by the complementary pulse from the level shifter, the "not-eight" pulse. This flip-flop controls transistors A2Q7-Q8 which gate the +200 Vdc to the Nixie tube anodes each display period, and also controls the reset pulse generator, A2Q5-Q6, which resets the associated decade scalers at the end of each display period.

2.3.3 The local oscillator signal is fed to Schmitt trigger A2Q9-Q11 which shapes the input signal so that the outpu to decade scaler A3Z1 is a train of positive pulses having a very fast rise time. These pulses are gated into A3Z1 in 10-ms bursts at a 50-Hz rate. When a gate pulse is received from A2Q10 the signal flow is cut off and a 10-ms display and reset interval begins. During the first 8 ms of this interval the gated +200 volts is applied to the Nixie readout so that they can display the count which accumulated during the preceding 10-ms interval. Following the 8-ms display period the gated +200 volts for the Nixies is cut off, extinguishing the display, and a 2-ms reset interval begins. A 0.5-ms reset pulse from the reset pulse generator resets A3Z1, A4Z1, A5Z1, and A6Z1 to all zeros, and 1.5 ms later the next 10-ms counting interval begins. The timing operations can be summarized as follows: A 10-ms counting interval is followed by a gate pulse which cuts off the flow of the local oscillator signal into the counter. When the gate pulse is generated the +200-Vdc Nixie supply is turned on for 8-ms and the count held by the decade scalers is displayed. Following this interval the display is extinguished, and the reset pulse is simultaneously generated. Two ms later another 10-ms counting interval begins. Thus each count and display interval requires 20 ms, so that the local oscillator frequency is updated and displayed at a 50-Hz rate.

2.3.4 All decade scalers in the counter assembly count in the binary coded decimal (BCD) system. That is, the scaler counts from 0 to 9 for a total count of 10, and then resets itself to 0. The readout decoder and Nixie driver ICs continuously decode the contents of their associated decade scalers from binary to its decimal equivalent, but readout cannot occur until the +200 Vdc is gated to the Nixies at the beginning of the display period.

2.3.5 Although the local oscillator signal is counted for only a 10 ms (or 100 ms) interval, the frequency is display in kilohertz per second. This is done by placing the decimal point in the display where it would appear if the signal were actually counted for a full second, and by not displaying the "2" which would always appear as the most signifi cant digit in the readout. For example, assume the receiver is tuned to 500 Hz. The local oscillator frequency wil

then be 2500 kHz. In 10 ms 25,000 Hz will be counted. The "2" is dropped and the decimal point is placed so that the display reads 500.0 kHz. When the decimal shift mode is used the counting interval is increased to 100 ms, the two most significant digits are not displayed, and the decimal point is shifted one place to the left. Assuming that the receiver is tuned to 500.55 kHz, the oscillator frequency will be 2500.55 kHz. Before going to the decimal shift mode the display will read 500.5 kHz. Once the MODE switch is placed in a DECIMAL SHIFT position 250,055 Hz will be counted in each 100 ms counting interval. The "2" and "5" are dropped from the display and the readout is 00.55 kHz. It is necessary to mentally add the "5" to get the true frequency reading: 500.55 kHz.

2.3.6 When used in the DAFC mode the receiver's local oscillator is locked to the last digit of the decimal display in either the normal display or decimal shift mode. The desired digit is set by the DAFC LAST DIGIT switch. A correction voltage is obtained from the DAFC module, Z1, and applied to a voltage-variable capacitor in the local oscillator circuit if the frequency should drift, pulling the oscillator back on frequency. Note in Figure 2-2 that the DAFC LAST DIGIT switch, S2, connects to the decoded output of the last digit readout decoder and Nixie driver A3Z2. As shown in the figure, the switch is set in the "0" digit position, so that the "0" output of A3Z2 terminates at the switch. Digits "6" through "9" are connected through S2A and S1B-W to the "up pulse" input of the DAFC module; digits "1" through "5" are connected through S2B and S1A-Y to the "down pulse" input to the DAFC module. As long as the local oscillator remains on frequency an output from A3Z2 appears only on the "0" line each time the Nixie display is gated on, and no correction pulses reach Z1. If, for example, the receiver frequency is set to 300.0 kHz and it drifts to 300.1 kHz, then pulses appear on the "1" output line from A3Z2. These pulses are conducted from the wiper of S2B, through S1A-Y to the down pulse input of Z1. These pulses are processed in the DAFC module to produce an analog correction voltage which will pull the local oscillator down in frequency. Once the receiver is back to 300.0 kHz no additional correction pulses are applied to Z1. Should the receiver drift to a lower frequency, say 299.9 kHz, then pulses from the "9" output line of A3Z2 are fed to the up pulse input of Z1 to produce an output which will pull the local oscillator up in frequency to 300.0 kHz. When the MODE switch is placed in either TUNE position, switch sections S1A-Y and S1B-W disconnect S2 from the DAFC module, and a fixed prelock positioning voltage of approximately 9 Vdc is obtained from the module and fed to the voltage-variable capacitor in the local oscillator circuit.

2.4 INPUT TRANSFORMER AND FILTER ASSEMBLY

Figure 6-1 is the schematic diagram for the input transformer and filter assembly. Its reference designation prefix is A1. The incoming signal is fed into the receiver through input transformer T1. The primary of T1 is tapped, providing balanced input impedances of 1000 ohms or 50 ohms, depending on the position of selector switch S1. To prevent ground loops and minimize hum the balanced circuit is maintained through the filter portion of this module, the input attenuator, A2, and into the input amplifier, A3. The entire transformer-filter assembly is encased in a steel inner chassis to prevent the pick up of 60 Hz radiation from the receiver's own power transformer and from outside sources. From the secondary of T1 the signal is fed through a bandpass filter which passes only those signals in the 500 Hz to 603 kHz frequency range. It contains series traps for 1-MHz and 2-MHz signals. The purpose of the filter is to prevent interference from signals outside the receiver's tuning range, particularly those near the receiver's 2-MHz IF frequency, or harmonics of this frequency.

2.5 INPUT ATTENUATOR

The input attenuator is used to prevent overloading the receiver on strong signals. It is connected between the input filter and the input amplifier. Figure 6-2 is the schematic diagram for the attenuator; its reference designation prefix is A2. The front-panel INPUT ATTENUATOR switch, A2S1, selects various combinations of resistors to provide attenuations of -20, -40, and -60 dB. When the 0 dB switch position is selected, the signal is routed through the attenuator without encountering any resistors.

2.6 INPUT AMPLIFIER AND BALANCED MIXER

Figure 6-3 is the schematic diagram for the input amplifier and balanced mixer; A3 is its reference designation prefix.

2.6.1 Input Amplifier. - The input amplifier consists of transistors A1Q1 and A1Q2 in a dc-coupled, complementary configuration. A1Q1 is an ultra-low noise, high-gain transistor. Capacitor A1C2 and resistor A1R3 provide a negative feedback path from the collector of A1Q1 to its base. This network is used to cause the input impedance to be approximately 1000 ohms, matching the impedance through the input transformer, filter, and attenuator. A second negative feedback path is from the collector of A1Q2 through A1R6 to the emitter of A1Q1. This feedback is

to equalize the response of the input amplifier over the receiver's 1-kHz to 600-kHz tuning range. Capacitor A1C3 and resistor A1R5 in the emitter of A1Q1 cause the response of the amplifier to roll off rapidly below 500 Hz. Silicon diodes A1CR1 and A1CR2 are shunt limiters at the input to A1Q1 to prevent the incoming signal from exceeding 1.2 volts peak-to-peak and overloading the amplifier. Emitter follower A1Q3 is connected between A1Q2 and the balanced mixer to prevent the modulator from loading down the amplifier. The signal output from A1Q3 is beat with the local oscillator signal in the balanced mixer to produce a 2-MHz output.

2.6.2 Balanced Mixer. - A balanced mixer is used rather than a conventional mixer, to prevent the local oscillator signal from entering the IF amplifier stages when the receiver is tuned near the end of its low-frequency range.

2.6.2.1 The balanced mixer suppresses the input signal to the receiver and the local oscillator signal, passing the sum and differences of the two signals. Since the following IF stage is tuned to the difference frequency (2 MHz) only this frequency is passed. The balanced mixer consists essentially of diodes A1CR3 through A1CR6 connected in a symmetrical lattice configuration, and transformers A1T1 and A1T2. Resistors A1R14, A1R15, A1R21, and A1R22 equalize the current through the diodes. The square wave oscillator (LO) signal is used to switch the diodes in the balanced mixer, and is applied to the mixer circuit through A1T1 which is driven by an amplifier made up of A1Q4 and A1Q5. The amplifier provides a push-pull output from an unbalanced input.

2.6.2.2 The LO signal from A4 is coupled to the base of A1Q4 through dc-blocking capacitor A1C10. Capacitor A1C13 couples the signal from A1Q4 to A1Q5. The positive-going half cycle of the LO signal drives A1Q4 to saturation. This results in a positive-going signal on the emitter of A1Q5 which cuts this transistor off. On the negative-going half cycle of the LO signal A1Q4 is cut off and A1Q5 goes into saturation. Capacitor A1C11 holds the base of A1Q5 at RF ground potential. Its dc base voltage is set by A1R30. This potentiometer is used to adjust the output square wave from the amplifier for maximum symmetry. Resistor A1R32 across the primary of A1T1 damps out an undesirable ringing in the square wave. The LO signal switches the diodes in the mixer circuit at a rate twice the oscillator frequency (once every positive half cycle, and once every negative half cycle). When the LO voltage is positive at the junction of A1R14 and A1R15 diodes A1CR3 and A1CR5 are forward biased. When the voltage reverses, A1CR4 and A1CR6 are forward biased. As a result, the input signal current flowing in the primary of A1T2 changes direction each time the diodes switch. The amount of current flowing will depend on the instantaneous value of the input signal voltage. The output contains the upper and lower sidebands which result from mixing the input and LO signals. Since the following IF stage is tuned to the lower sideband frequency (2 MHz) only this frequency will pass. The input and LO signals are cancelled by the balanced mixer. Variable resistors A1R19 and A1R27 are dc balance controls for the mixer, and A1C8 and A1C15 are ac balance controls. These controls compensate for any inherent unbalance in the circuit. They are adjusted for maximum suppression of the LO signal.

2.7 NOISE IF AMPLIFIER AND GATE

The schematic diagram for the noise IF amplifier and gate is Figure 6-18; A12 is its reference designation prefix. The 2-MHz output from the balanced mixer is applied in parallel to both a four-stage noise IF amplifier and to a single-stage signal IF amplifier.

2.7.1 Noise IF Amplifier. -

2.7.1.1 The four noise IF amplifier stages A1Q1 through A1Q4 have a bandwidth of 50-kHz and are energized by the +12 volts applied through feedthru capacitor C3 when the NOISE CANCELLER THRESHOLD control is moved from the OFF position. Due to the similarity of the stages, only one will be discussed in detail. The 2-MHz input signal is coupled through dc-blocking capacitor A1C2 to the base of A1Q1. Resistor A1R1 terminates the input for both the noise and signal IF stages. Resistors A1R2, A1R3, and A1R4 form a voltage divider for the biasing of A1Q1. The biasing voltage is obtained from the noise AGC amplifier. Stages A1Q1, A1Q2, and A1Q3 are AGC controlled. The bias voltage is driven increasingly less positive with increasing input signal strength so that the gain of the stages is reduced. The tuned collector circuit of A1Q1 consists of A1L1, A1C6, A1C7, plus the distributed capacity of the inductor. Resistor A1R9 shunts A1L1 to lower its Q to obtain the required 50-kHz bandwidth. Resistor A1R6 is included for parasitic suppression. In the emitter circuit of A1Q1 resistor A1R7 is unbypassed to provide a slight amount of degeneration to stabilize the stage due to its high gain. High-frequency transistors are used for all the IF stages to make neutralization unnecessary. The output of A1Q1 is coupled through an impedance-matching voltage divider consisting of A1C6 and A1C7 to the base of A1Q2.

2.7.1.2 Transistor A1Q4 is a PNP type so that the outputs of diodes A1CR1 and A1CR2 can be referenced to zero

Vdc. These diodes are the noise detector, and the noise AGC detector, respectively. Diode A1CR2 conducts on the positive half cycles of the output from A1Q4, and A1CR1 conducts on the negative half cycles. The noise AGC circuit results in a relatively constant level, largely free of modulation, at the output of A1Q4 so that the triggering of the noise gate is determined by the biasing of emitter follower A1Q5. This, in turn, is determined by the position of the NOISE CANCELLER THRESHOLD control. Biasing voltage for the transistor is obtained from the wiper of the control and applied to the base through C4 and A1R29. As the control is turned clockwise the voltage becomes increasingly positive, increasing the threshold level. Sufficient negative bias voltage cannot be obtained from the threshold control to cause A1Q5 to conduct without the addition of rectified noise voltage. The rectified noise spikes from A1CR1 and coupled through A1C21 to the base of A1Q5. If the amplitude of the spikes exceeds the dc threshold level established on the base sufficiently to cause the transistor to conduct, the noise gate is opened so that the noise does not appear at the receiver's output. Diode A1CR3 and resistor R33 clamp the voltage at the junction of A1R32 and A1E8 at approximately -0.4 Vdc. When the NOISE CANCELLER THRESHOLD control is in the maximum counterclockwise position (without being OFF) the wiper of the control is connected to this point. With this negative voltage at the control wiper the noise threshold is at the lowest point. That is, the least amount of rectified noise voltage is required to cause A1Q5 to conduct, and thus open the noise gate.

2.7.2 Signal IF Amplifier and Noise Gate. -

2.7.2.1 The 2-MHz input signal is coupled through dc-blocking capacitor A2C1 to the base of A2Q1. Resistors A2R1, A2R2, and A2R4 form the base-biasing voltage divider. The collector circuit of the transistor is double tuned to achieve a 20-kHz bandwidth. One tuned circuit consists of A2L1 in parallel with A2C3; the other is made of A2L2 paralleled by A2C6 and A2C7. Capacitor A2C5 couples the tuned circuits for a slightly undercoupled response. The output from the stage is fed through an impedance-matching, capacitive voltage divider consisting of A2C6 and A2C7 to the noise gate circuit.

2.7.2.2 If A1Q5 is not conducting diodes A2CR1 and A2CR2 are forward biased, and A2CR3 and A2CR4 are reverse biased. The input signal to A2T1 is then passed by A2CR1 and A2CR2, and then coupled through A2T2 to the switching amplifier assembly, A6. With the noise gate passing signals A2Q2 is cut off. The forward bias voltage for the two conducting diodes is obtained from the -12 Vdc supply through a voltage divider consisting of A2R9, A2R10, and A2R11. Potentiometer A2R6 is adjusted to equalize the current through the same two diodes. Resistors A2R7 and A2R8 bias the cathodes of A2CR3 and A2CR4 from the -12 Vdc supply. With A2CR1 and A2CR2 conducting, this bias voltage is not sufficient to forward bias A2CR3 and A2CR4. Capacitor A2C9 forms a parallel tuned circuit with the primary of A2T2 which resonates at 2 MHz. A balanced circuit is maintained through the noise gate to prevent the generation of transient voltages when the noise gate is opened and closed.

2.7.2.3 When a noise pulse causes A1Q5 to conduct, current flows through A2R12 and tunnel diode A2CR5. The tunnel diode rapidly switches from the stable peak point on its characteristic curve, through the unstable valley point, to a stable high-voltage point. As the tunnel diode switches, A2Q2 is simultaneously switched with it, going from the off to the on condition. By using the tunnel diode-transistor combination a switching speed is obtained which is much faster than that possible with the transistor alone. Once A2Q2 conducts, the voltage on the cathodes of A2CR1 and A2CR2 drops to essentially ground potential, reverse biasing the diodes. With these two diodes not conducting, the voltage from divider A2R7 and A2R8 constitutes a forward bias for A2CR3 and A2CR4. A short circuit now exists across the primary of A2T2 so that any signal which leaks through the reverse biased A2CR1 and A2CR2 cannot be coupled through the output transformer.

2.7.2.4 Since the noise pulse, in effect, passes through the 50-kHz bandwidth noise IF stages faster than through the 20-kHz bandwidth signal IF stage, the noise gate would close on the trailing edge of the pulse, allowing a part of the pulse which was passing simultaneously through A2Q1 to appear at the output. To prevent this a delay is built into the noise gate circuit to insure that the gate remains open long enough that the pulse which triggered the gate has decayed in the 20-kHz signal IF stage before the gate closes. This delay is provided by A2C10 and A2R11. Before the gate is triggered A2C10 is charged to the same voltage as the collector of A2Q2. When the transistor is turned on the capacitor rapidly discharges through the collector-emitter junction to ground. On the trailing edge of the noise pulse A2CR5 switches back to a stable point on the peak current side of its characteristic curve, cutting off A2Q2 as it does so. If it were not for A2C10 the voltage on the collector would instantaneously return to the normal value so that diodes A2CR1 and A2CR2 would be forward biased and A2CR3 and A2CR4 reverse biased, causing the gate immediately to close. However, the collector voltage must build up at a rate determined by the RC time constant of A2C10 and A2R11 as the capacitor recharges through the resistor, resulting in a delay in closing the noise gate.

2.8 IF AND BFO ASSEMBLY

The IF and BFO assembly is included on the main chassis schematic diagram, Figure 6-20. It contains five subassemblies, each of which is discussed separately below. A5 is the reference designation prefix for the entire assembly.

2.8.1 IF Bandswitching Amplifier "A". - Figure 6-5 is the schematic diagram for this subassembly; its reference designation prefix is A5A1. The input signal from the balanced mixer is applied through dc-blocking capacitor C2 to IF amplifier Q1. The stage is tuned by means of variable inductor L1 in its collector circuit. The inductor resonates with its distributed capacitance, and capacitors C3 and C4. It is tuned to 2 MHz. Resistor R3 in the collector circuit is included for parasitic suppression. Unbypassed emitter resistor R5 provides degenerative ac feedback to stabilize the stage. Gain of the stage is controlled by the AGC amplifier when in the AGC mode and the BFO is off. With the BFO in use, or when using the manual gain mode, the gain of Q1 is determined by the front-panel IF GAIN control. The gain control voltage is applied to the base voltage divider, R2-R4, and varies the stage gain by varying the forward bias on the base-emitter junction of the transistor. The output of the stage is coupled through an impedance-matching capacitive voltage divider made up of C3 and C4 to the second IF amplifier stage, Q2. This stage is identical to the first. Neutralization of the IF stages is not required due to the use of high-frequency transistors and operating them at nominal gain. The output of Q2 is applied in parallel to Q3 through Q6 and through an impedance-matching resistive pad to the SM OUTPUT jack. These latter four transistors provide no gain, functioning only as switches. They isolate Q2 from the three unused IF bandwidth filters, and provide a closed circuit to the filter being used. The IF BANDWIDTH switch determines which transistor will be turned on by applying +12 Vdc to the base voltage divider. This forward biases the base-emitter junction so that the signal can pass through to the bandwidth filter.

2.8.2 IF Bandwidth Switching Amplifier "B". - Figure 6-6 is the schematic diagram for this subassembly; its reference designation prefix is A5A2. It contains four emitter followers, Q1 through Q4, which share a common emitter load resistor, R6. The IF BANDWIDTH switch turns on the proper transistor to receive the output of the selected bandwidth filter by applying a forward bias to its base-emitter junction. Resistive pads are in the base circuit of each transistor to equalize the noise output from each bandwidth filter. A 47-ohm resistor is included in the collector circuit of each stage to prevent parasitic oscillations. The output from the selected filter is coupled through C5 and R12 to IF amplifier assembly A5A3.

2.8.3 IF Amplifier and AM Detector. - The schematic diagram for this subassembly is Figure 6-7; A5A3 is its reference designation prefix. The 2-MHz input signal is received from the IF amplifier "B", and is fed through four additional IF amplifier stages, Q1 through Q4. Except for Q4 the stages are quite similar to those described in paragraph 2.8.1. Depending on the type of receiver operation, Q1 is gain controlled by the AGC amplifier or the IF GAIN control. A PNP transistor is used in the Q4 position to reference the AM detector, CR3, output level to zero Vdc. The IF output for the BFO product detector and IF OUTPUT jack is taken at the junction of capacitors C15 and C16. Silicon diodes CR1 and CR2 clamp the anode of CR3 at approximately 1.2 Vdc to keep it forward biased. This is done to improve the linearity of the AM detector output. A low-pass filter made up of R25, C19 and C20 removes RF components which appear in the detector output. This output is fed to the AGC amplifier, the rear-panel DETECTOR LEVEL OUTPUT jack, and when the BFO switch is in the OFF position, to the audio amplifier.

2.8.4 BFO and Product Detector. - Figure 6-8 is the schematic diagram for the BFO and product detector; its reference designation prefix is A5A4. There are five separate beat frequency oscillators. Four are crystal controlled: Q2, Q3, Q6, and Q7. The frequency of the other, Q1, may be varied approximately 7 kHz each side of the 2-MHz center frequency. The oscillator in use depends on the position of the front-panel BFO selector switch. With the switch in the ZERO position Q2 is energized. Placing the switch in the VAR position turns on Q1. Moving it to the 5.5 kHz, USB, or LSB position energizes Q3, Q6, or Q7, respectively. The output from the "on" oscillator is mixed with the output from the IF amplifier in the product detector to produce an audible beat note, or in the case of single sideband reception, to render the transmission intelligible.

2.8.4.1 Variable Oscillator. - Transistor Q1 is the variable oscillator. The basic oscillator circuit is a modified Clapp with regenerative emitter-to-base feedback to sustain oscillation taken at the junction of C10 and C11 through R8. The purpose of R8 is to improve the linearity of the oscillator output. Capacitor C16 maintains the collector at RF ground potential. The oscillator frequency is shifted by varying the dc voltage across voltage-variable capacitors CR1 and CR7 by means of the BFO FREQ control. A voltage-variable capacitor is a semiconductor device whose capacitance varies inversely with the voltage applied across it. Thus, if the voltage across them increases, their capacitance decreases so that the oscillator frequency increases. The output from Q1 is coupled through

capacitor C17 to buffer-amplifier Q5. This transistor isolates the variable frequency oscillator from the product detector to prevent the detector from loading the oscillator and affecting its frequency stability. In addition, Q5 amplifies the output signal of the oscillator in use to switch the diodes in the product detector. The collector circuit of Q5 is broadly tuned to 2 MHz by a parallel resonant circuit made up of C22 and the primary of T1. Zener diode CR2 regulates the voltage for the selected oscillator at +10 Vdc.

2.8.4.2 Crystal-Controlled Oscillators. - All four of the crystal-controlled oscillator circuits are identical, therefore, only the zero-beat oscillator, Q2, will be discussed. The oscillator circuit is a crystal-controlled Colpitts. Regenerative emitter-to-base feedback is taken at the junction of C12 and C13 through R10. Capacitor C6 holds the collector of Q2 at RF ground potential. The oscillator output is applied through CR8 to the base of buffer stage Q4. This transistor isolates the variable frequency oscillator from the crystal oscillators to prevent the VFO from locking onto a crystal frequency as it is tuned past. The buffer stage has no gain. Capacitor C22 and T1 are also the collector load for Q4. Diodes CR8 through CR11 isolate the unused crystal oscillators from the one in operation to prevent the inactive components from shunting the output signal.

2.8.4.3 Product Detector. - The product detector provides an output which is proportional to the product of the IF input signal and the injected BFO signal. When either is not present there is no output. This type of detector is used to minimize the intermodulation distortion inherent in the demodulation process. The detector consists essentially of diodes CR3 through CR6 connected in a ring configuration. Resistors R23, R24, R27, and R29 equalize the current through the diodes. Potentiometer R26 is used to adjust the IF signal voltage applied across the detector to obtain maximum cancellation of RF currents in the detector. The switching voltage for the diodes is supplied by the BFO. If, for example, the BFO voltage causes the junction of R23 and R24 to go positive, then CR3 and CR4 will be forward biased. The IF signal will be shorted to ground through CR3 or CR4, depending on the polarity of the IF signal, and there will be no output from the detector. When the BFO voltage reverses so that the junction of R27 and R29 is positive, CR5 and CR6 will be forward biased. Under this condition there will be an output from the detector. When the IF signal is positive current flows through CR5. When the signal reverses polarity the current flows through CR6, and the current through the load is reversed. Capacitors C27 and C28 and resistor R34 form a low-pass filter at the output of the detector to bypass high-frequency signal components.

2.9 LOCAL OSCILLATOR

2.9.1 Figure 6-4 is the schematic diagram for the local oscillator; its reference designation prefix is A4. The frequency of the local oscillator A1Q1 is maintained 2 MHz above the frequency of the incoming signal. A modified Clapp circuit is used for the oscillator. Regenerative emitter-to-base feedback to sustain oscillation is taken at the junction of A1C3 and A1C4. Variable capacitor C5 is the main tuning control. Fine tuning is accomplished by varying the dc voltage across voltage-variable capacitor A1CR2 which is effectively in parallel with inductor A2L1. (See paragraph 2.8.4.1 for the operation of a voltage-variable capacitor.) Capacitor C6 is a variable temperature compensating trimmer. Its capacitance varies with temperature changes in the direction required to compensate for the shifts in value of the temperature-dependent components to maintain the oscillator frequency constant. The DAFC correction voltage, when the receiver is used in the DAFC mode, is applied across A1CR5. When the receiver is in the normal tuning mode a fixed voltage of approximately 9 Vdc is applied across A1R27 and A1CR5 from the DAFC module in the counter assembly. To minimize loading of the oscillator, the output is tapped down through a capacitive divider consisting of A1C7 and A1C8, and fed to limiter circuits.

2.9.2 The limiters convert the sinusoidal oscillator output to a square wave for more efficient operation of the balanced mixer, and for more reliable counting by the frequency display. Both limiters are nearly identical. They are essentially differential amplifiers with ac coupling between the two transistors. On positive half-cycles of the input to A1Q2, the positive-going signal developed across A1R9 is coupled through A1C9 to the emitter of common-base amplifier A1Q3. This positive signal on the emitter of A1Q3 is a reverse bias which cuts the transistor off. On the negative half-cycle of the input signal the transistor is driven into saturation. Thus, the transistor operates between the cut off and saturated conditions so that the signal is limited on both the positive and negative excursions. The limited output is fed to emitter followers A1Q4 and A1Q5 which are connected in a complementary symmetry configuration. They are biased to operate as Class B amplifiers. Silicon diodes A1CR1 and A1CR3 eliminate crossover distortion and prevent thermal runaway. Since the transistors and diodes are made of the same material they exhibit the same temperature coefficient of resistance characteristics. A rise in temperature lowers the base-emitter resistance of the transistors, tending to make them conduct harder. However, the diode resistance changes by approximately the same amount, so that the forward bias on the transistors is decreased. As a result, the

emitter current through the transistors is held within safe limits. Because of the very low impedance output of the emitter followers, the amplifier output impedance is determined largely by A1R17.

2.10 AGC AMPLIFIER AND +200V POWER SUPPLY

This module contains separate AGC circuits for the signal and noise IF amplifiers, as well as the rectifier and filtering for the +200 Vdc supply used by the frequency display Nixie tubes.

2.10.1 Signal IF AGC Amplifier. - AGC action begins when the (s plus n)/n ratio at the receiver's output attains a level of approximately 10 dB.

2.10.1.1 The input to the signal AGC amplifier is obtained from the AM detector. It is applied to an emitter follower, Q1, which drives dc amplifier Q3 and the signal strength meter driver, Q4. Resistor R3 and capacitor C1 form a modulation filter to remove audio variations from the detector output so that the base of Q3 receives a dc voltage which varies in direct proportion to the average value of the input carrier to the receiver. Thus, as the input signal strength increases the AM detector output becomes more positive, as does the base of Q3. As a result Q3 conducts harder causing its collector, and the base of series regulator Q2, to go less positive due to the voltage drop across R4. Transistor Q2 is connected in series with the +12 volt supply and the base-bias circuits of the AGC-controlled IF stages, so that as its base voltage drops it conducts less, and the AGC output voltage becomes less positive. As a result, the forward bias on the gain-controlled stages decreases so that receiver gain is reduc Should the input signal strength decrease, the AM detector output also decreases, so that the AGC voltage becomes more positive, increasing the gain of the receiver.

2.10.1.2 Input to the signal strength meter driver is taken from Q1 before the modulation filter. There are two possible paths for the signal to reach Q4. The path taken depends on the position of the BFO switch. With the switc in the OFF position the signal is fed through R6 to the base of Q4. Placing the switch in any of the BFO positions routes the signal through CR1 and R8 to Q4. This is done to make the response of the meter to CW approximate its response to AM signals. Diode CR1 and resistor R8 provide a low-impedance charge path for C2 so that the capacitor charges rapidly. When there is a break in the signal C2 discharges slowly through R7 so that the meter needl does not drop rapidly back to zero before the next signal burst. Transistor Q4 operates as an emitter follower. Silicon diodes CR2 and CR3 in the emitter circuit protect the meter from damage in the event of an excessively strc signal. If the output from Q4 exceeds approximately 1.2 volts the diodes conduct and clamp the output at this value Should the input signal continue to increase no additional current can be forced through the meter.

2.10.2 Noise IF AGC Amplifier. - The noise IF AGC amplifier consists of a dc amplifier, Q6, and a regulator transistor, Q5. The circuit is energized only when the NOISE CANCELLER THRESHOLD control is moved from th OFF position. This applies +12 Vdc through S7 to pin 19 of the AGC amplifier module, providing collector voltage to Q5 and Q6. The operation of these two stages is identical to that described above for Q2 and Q3. The circuit ha a much faster response time, however, so that it can follow the modulation on a signal to maintain a constant input to the noise detector, A12A1CR1. The signal input is obtained from the noise AGC detector, A12A1CR2.

2.10.3 +200V Power Supply. - The +200-Vdc power supply provides the anode voltage for the Nixie tubes when they are gated on. Secondary winding 8-10 of T1 provides the ac input to silicon diodes CR4 and CR5 which are con nected in a full-wave rectifier circuit. The pulsating dc output from the rectifiers is filtered by electrolytic capacitor C5. Resistor R15 functions as a bleeder to discharge C5 when the unit is turned off.

2.11 AUDIO AMPLIFIER

Separate audio amplifiers are used to supply the front-panel PHONES jack and balanced 600-ohm output at the rear of the receiver. The front-panel AUDIO GAIN control affects only the PHONES jack amplifier. Both amplifiers are built on the same plug-in etched circuit board. Figure 6-10 is the schematic diagram for the audio amplif board; A7 is its reference designation prefix.

2.11.1 Input to the audio amplifier is from the AM detector when the BFO is off, and from the product detector whe the BFO is on. The input is fed to an emitter follower, Q1, which is common to both amplifiers. When the audio bandwidth switch, S5, is in the NORMAL position, the output from Q1 is fed directly to the balanced output amplifie and through the AUDIO GAIN control to the PHONES amplifier. Placing S5 in the NARROW position routes the signal through an audio filter before it is fed to the two amplifiers. The filter consists of capacitor C2 on the amplifier board in series with variable inductor L1 on the main chassis. It is tuned to 1 kHz. Resistor R9 is shunted across L1 to lower the Q of the inductor sufficiently to attain a 350-Hz filter bandwidth.

2.11.2 The headphones amplifier consists of transistors Q3 and Q5 in a direct-coupled complementary configuration. Silicon diode CR1 provides thermal protection for the amplifier. When the base-emitter resistance of silicon transistor Q3 decreases due to an increase in temperature it will conduct harder. The conduction of the diode, which is made of the same material, will also increase by approximately the same amount. This results in a decrease in the forward bias on the transistor so that its conduction drops to a safe value. Negative feedback from the collector of Q5 to the emitter of Q3 is obtained through R15. Resistor R12 and capacitor C5 in the emitter circuit of Q3 cause the amplifier response to fall off rapidly above 7000 Hz. Output from the amplifier is fed through R20 and C7 to the PHONES jack.

2.11.3 Gain of the balanced output amplifier is controlled by potentiometer R4 on the amplifier board. Three direct-coupled transistors, Q2, Q4, and Q6, are used for the amplifier. The first stage, Q2, is a conventional voltage amplifier in a common emitter configuration. The second stage is an emitter follower used to match the high output impedance of the first stage to the low input impedance of the third stage, a power amplifier. Paralleled capacitor C6 and resistor R18 couples the signal from Q4 to Q6. This arrangement is used to increase the stability of the amplifier. Resistor R21 provides negative feedback from the output stage to the emitter of Q2. Capacitor C1 and resistor R24 in the emitter circuit of Q6 causes the amplifier response to roll off at 7000 Hz. Capacitor C8 across the secondary of input transformer T1 is also included to attenuate output signal components above 7 kHz.

2.12 COUNTER ASSEMBLY

The counter assembly contains all logic circuitry required for the counting, decoding, and display of the receiver's local oscillator frequency, as well as the encapsulated DAFC module. It is built as a self-contained, shielded assembly to minimize RFI. Figure 6-14 is the schematic diagram for the counter assembly; it carries the reference designation prefix A11.

2.12.1 Oscillator-Divider Module. - Figure 6-15 is the schematic diagram for this module; A11A1 is its reference designation prefix.

2.12.1.1 1-MHz Oscillator. - Transistor Q1 is the 1-MHz oscillator. The basic oscillator circuit is a crystal-controlled Colpitts with the crystal on the counter assembly. Trimmer capacitor C1, also located on the counter assembly, is used to set the oscillator frequency to exactly 1 MHz by zero beating with WWV. Emitter-to-base feedback to sustain oscillation is taken at the junction of C4 and C5. Transistor Q2 is biased off so that it conducts only when the collector voltage of Q1 is negative-going. When Q2 conducts positive-going pulses are formed at its collector. These pulses are differentiated and shaped by R5, L1, and C6. These pulses at a 1-MHz rate constitute the input to the dividers. Diode CR1 damps out the negative spike produced by the differentiating action of L1.

2.12.1.2 Frequency Dividers. - Integrated circuits Z1 through Z5 are decade scalers, so that each divides the oscillator output by a factor of ten. The output from each IC is a train of positive pulses swinging between ground potential and +2 volts. If the front-panel MODE switch is in either NORMAL DISPLAY position the 100-Hz output of Z4 controls the timing operations in the counter. Placing the MODE switch in either DECIMAL SHIFT position results in the 10-Hz output of Z5 controlling the timing. Silicon diode CR2 drops the +4.5 Vdc input voltage approximately 0.5 volt to obtain the proper operating voltage for the ICs.

2.12.1.3 Level Shifter. - Transistors Q3 through Q7 shift the 2-volt pulse level from Z4 or Z5 to 4.5 volts to operate discrete-component flip-flops in the gate generator circuit, and they also provide the complement to the "not-eight" output from the ICs which is also required in the gate generator operations. Transistors Q4 and Q5 form a flip-flop which is triggered by grounding the collector of the "off" transistor. This is done by Q3 and Q6; Q7 performs a required phase inversion. Assume that Q5 is conducting and Q4 is off. On the leading edge of an output pulse from Z4 or Z5 transistor Q3 will conduct, causing the voltage at the junction of R8 and R12 to increase in the negative direction. This starts Q5 moving towards cut off. As it does so the positive-going voltage developed across load resistor R14 is coupled through R13 and C2 to the base of Q4, so that this transistor starts turning on. These two actions continue regeneratively until Q5 is cut off and Q4 is conducting to saturation. Transistor Q7 is also turned on at the same time as Q3, however, the negative-going voltage developed across load resistor R9 turns off Q6 so that it does not affect the switching action at this time. On the trailing edge of the pulse from the frequency divider transistors Q3 and Q7 are turned off. The positive-going voltage across R9 now turns on Q6, starting the regenerative action which causes the flip-flop to again switch states. As a result, the two outputs from the flip-flop are 180 degrees out of phase with each other, but have the same frequency as the output from Z4 or Z5 and a voltage swing of 4.5 volts.

2.12.2 Amplifier and Gate Generator. - The schematic diagram for this module is Figure 6-16; A11A2 is its reference designation prefix. The amplifier and gate generator are independent circuits.

2.12.2.1 Gate Generator. -

2.12.2.1.1 Transistors Q1 through Q8 comprise the gate generator circuit. Gating operations are controlled by two flip-flops, Q1-Q2 and Q3-Q4, which receive their inputs from the level shifter in module A11A1. The flip-flops are switched by applying a negative trigger pulse through a steering diode to the base of the conducting transistor, cutting it off. For purposes of discussion, assume that Q1 is conducting, and Q2 is cut off. The positive input pulse is passed through C6 and C7 and differentiated into positive-going and negative-going spikes. Steering diodes CR1 and CR2 are connected so that the positive-going spikes can never reach the transistor bases. However, due to the positive base voltage of conducting transistor Q1, diode CR1 is forward biased to the negative-going spike so that it reaches the base of Q1. This transistor will now move toward cut off. The positive-going voltage at its collector is coupled through R8 and C1 to the base of Q2. As Q2 begins to conduct the negative-going voltage at its collector is coupled through R9 and C2 to the base of Q1, assisting the cut off of the latter transistor. This regenerative acti continues until a stable condition is reached with Q2 conducting and Q1 held at cut off due to the drop across voltage divider R13 and R9 from the -4.5 Vdc supply. With the flip-flop in this condition steering diode CR1 will be reverse biased due to the negative voltage at the base of Q1, and CR2 forward biased due to the positive potential at the base of the conducting transistor. The negative spike resulting from the next input pulse will then be conducted through CR2 to reverse the state of the flip-flop.

2.12.2.1.2 Operation of the entire gate generator circuit is best explained by referring to the generator timing chart, Figure 2-3. This chart applies if the MODE switch is in either NORMAL DISPLAY position. If the switch is in a DECIMAL SHIFT position, then the timing given on the chart must be multiplied by ten. The top line on the chart, the 1-kHz pulse train, is included for reference. This is the pulse train entering decade scaler A1Z4, whose output controls the gate generator timing for a normal display. The "eight" and "not-eight" pulses are from the level shifter and occur at a 100-Hz rate. Operation of the gate transistor, Q10, is determined by the collector potential of Q1. When Q1 is conducting its collector potential is 0 Vdc and the gate is closed, permitting the flow of the local oscillator signal into the counter. With Q1 cut off its collector voltage rises to approximately 4.5 Vdc and the gate opens, inhibiting the flow of information into the counter. Referring to Figure 2-3, assume that reset pulse No. 1 has just occurred with the leading edge of the first "eight" pulse. The gate will be open since the collector voltage of Q1 is high. The Nixie display, which is controlled by Q4, goes off at the time the reset pulse is generated On the negative-going trailing edge of the "eight" pulse Q2 is cut off which cuts Q1 on. This closes the gate and the counting interval begins. The positive-going transition at the collector of Q2 is coupled to Q4 through C5, but can have no effect due to steering diode CR4. Following a 10-ms counting interval, on the trailing edge of the second "eight" pulse, the conducting Q1 is cut off and the gate is opened. During the counting interval Q7 and Q8 are cut off so that the Nixie display is extinguished. Also during this interval Q5 is conducting to saturation and Q6 is biased off. Diode CR5 clamps the reset line at approximately 0.2 Vdc except when the reset pulse is generated. The negative transition which occurs at the collector of Q2 when Q1 is cut off is coupled through C5 and CR4 to the base of Q4, cutting this transistor off. At this point the 8-ms display period begins. The positive-going voltage at the collector of Q4 turns on Q7. The voltage drop across R23 turns on Q8, a PNP transistor, so that the 200 Vdc is gated out to turn on the Nixie display. With Q4 turned off during the display interval C9 charges from its nominal voltage of 3 Vdc up to approximately 6 Vdc. Eight ms after the beginning of the display interval the negative-going leading edge of the third "not-eight" pulse is coupled through C8 and CR3 to turn off Q3. This turns on Q4 which, in turn, cuts off Q7 and Q8 so that the Nixie display is extinguished. When the collector voltage of Q4 switches in the negative direction, the voltage at the plus end of C9 suddenly changes from 4.5 Vdc to 3 Vdc. Since the voltage across the capacitor cannot change instantaneously, the voltage at its minus end drops to approximately -3 Vdc. This pulls Q5 out of saturation, and drives it to cut off. The rise in voltage across R6 cuts on Q6. With Q6 conducting a positive pulse is developed across R20. The width of the pulse, approximately 0.5 ms, is determined by the RC time constant of C9 and R5. When C9 has discharged sufficiently for Q5 to start conducting again, Q6 cuts off and the voltage on the reset line drops back to the clamp level. Two ms after the display is cut off the negative-going trailing edge of the third "eight" pulse cuts off Q2 and another counting interval begins.

2.12.2.2 Amplifier. - The local oscillator input signal is passed through silicon diode shunt limiters CR6 and CR7 These diodes prevent the input signal amplitude from exceeding approximately 1.2 volts peak-to-peak. The limited signal is coupled through C13 to a Schmitt trigger made up of Q9 and Q11. Transistor Q10 functions as the gate. With Q10 conducting the Schmitt trigger is disabled and the input signal cannot reach the counting circuits. The Schmitt trigger squares up the input signal to improve the rise time. With no signal input Q9 is conducting and Q11

Figure 2-3

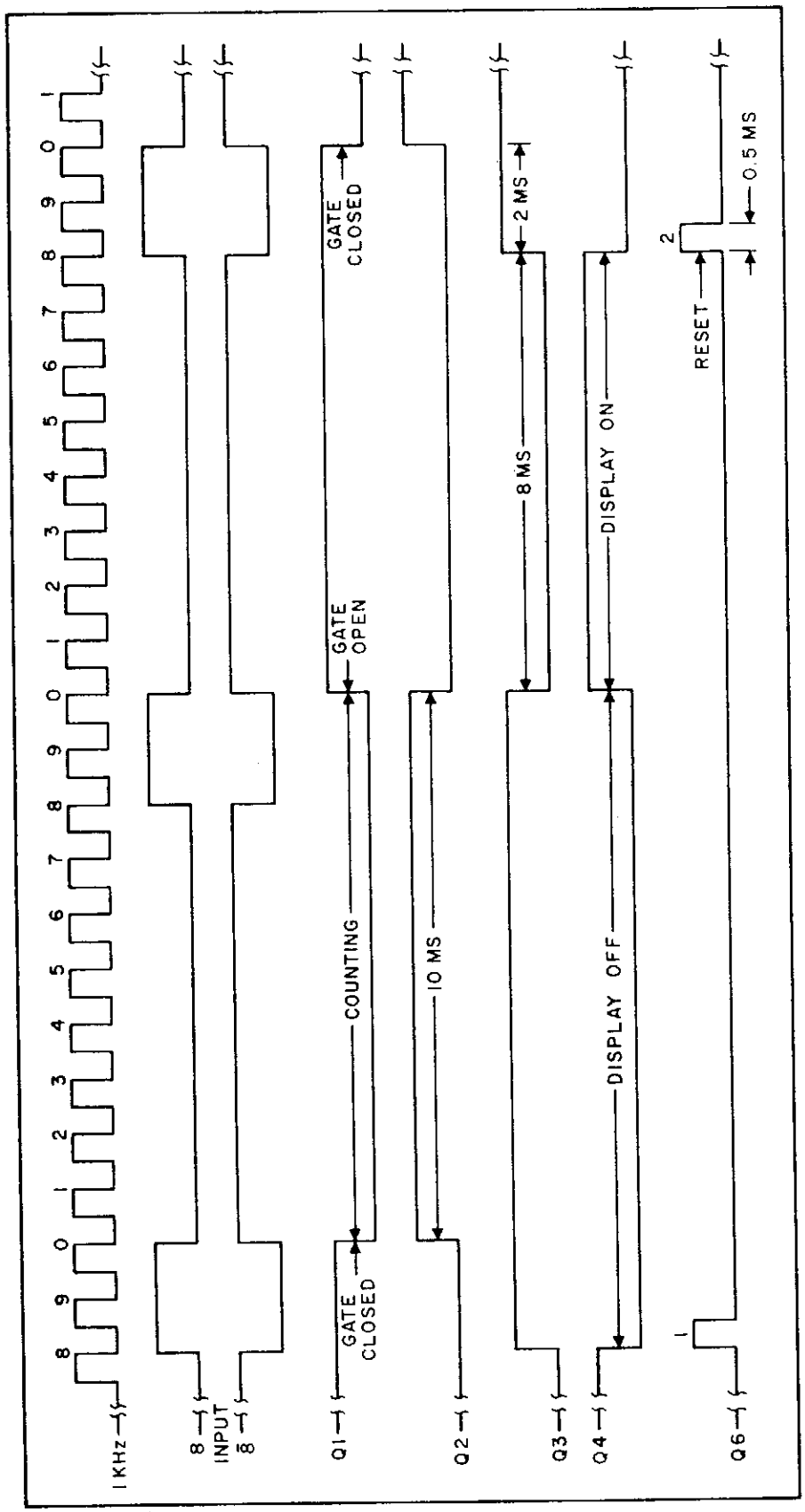

Figure 2-3. Gate Generator Timing Chart

is cut off. When the signal goes negative Q9 moves toward cut off. As the collector voltage of Q9 goes positive, the increasing voltage is coupled through R31 and C15 to start turning Q11 on. In addition, as the emitter current of Q9 decreases, the voltage drop across R29 decreases. As a result, the emitter voltage of Q11 moves in the negative direction, increasing the forward bias on the transistor. This regenerative action continues until Q11 is conducting to saturation and Q9 is cut off. The circuit remains in this stable condition until the input to Q9 swings in the positi direction, cutting Q9 back on. The regenerative action which results from turning Q9 on turns Q11 off. This switch ing action results in negative-going pulses at the collector of Q11 with an extremely fast rise time, and having the same frequency as the input signal to the unit. When the readout interval begins the level at the collector of Q1 rise to approximately +4.5 Vdc. This forward biases gate transistor Q10 through the R30-R32 divider so that it turns or and conducts to saturation. The additional current through R29 causes a voltage drop across the resistor which reverse biases the base-emitter junction of Q9 to the extent that the Schmitt trigger is disabled. When the gate inpu drops to 0 Vdc at the end of the display interval, operation of the circuit returns to normal. Emitter follower Q12 conducts to saturation when Q11 is off, and is cut off when Q11 turns on because of the negative-going voltage couple through C16. The pulse output of Q12 developed across R37 is fed to the first decade scaler module, A3.

2.12.3 Readout Scaler and Nixie Driver. - There are four of these modules. They carry reference designation prefixes A11A3 through A11A6. Figure 6-17 is the schematic diagram. Each module contains an IC decade scaler, Z1, an IC decoder and Nixie driver, Z2, and a Nixie tube, DS1. Each decade scaler divides the local oscillator signal by a factor of ten, and passes a carry pulse to the next higher decade, except for the mose significant digit decade, A6Z1. Each decade scaler is reset to zero at the end of each display period by a positive pulse from the amplifier and gate generator module. Silicon diode CR1 drops the +4.5 Vdc input voltage approximately 0.5 volts to obtain the proper operating voltage. Except for A3Z2 all Nixie driver ICs continuously decode the binary outputs of their associated decade scalers, but readout can occur only when the +200 volts is gated to the Nixies at the beginning of the display period. The +4.5-Vdc operating voltage for A3Z2 is gated on with the +200 Vdc through the DAFC module. This is done to prevent "trash" which appears on the output lines of the Nixie drivers during the counting intervals from causing erratic DAFC operation.

2.13 POWER SUPPLIES

The receiver contains four separate power supplies. Three are built on independent plug-in etched circuit boards and provide regulated outputs of +4.5 and -4.5 Vdc, +12 Vdc, and -12 Vdc. The fourth is built on the AGC module and provides an output of +200 Vdc. This power supply was discussed in paragraph 2.10.3. All operate from a common power transformer. Input power to the unit may be 115 or 230 Vac. When switch S1 is in the 115-V position the two primaries of power transformer T1 are connected in parallel (see main chassis schematic diagram, Figure 6-20). Placing the switch in the 230-Vac position connects the primaries in series and adds fuse F2 to the circuit.

2.13.1 +12-Vdc Power Supply. -

2.13.1.1 Figure 6-11 is the schematic diagram for this power supply; it carries the reference designation prefix A8. The ac input from power transformer T1 is rectified by full-wave rectifier, CR1. Initial filtering of the pulsating dc output from the rectifier is by electrolytic capacitor C1. Transistor Q1 functions as a series regulator whose conduction is controlled by a differential amplifier consisting of Q3 and Q4. The differential amplifier amplifies any difference between the voltages at the bases of the two transistors. The base of Q4 is fixed at approximately 6.2 Vdc by Zener diode CR2. Transistor Q3 has its base connected to the regulated output through a sampling circuit consisting of R6, R7, and R8. Any fluctuation in the output voltage is amplified and inverted by Q3, and applied to the base of the series regulator through emitter follower Q2. If, for example, the output voltage tends to rise, Q3 conducts harder, causing an increased voltage drop across load resistors R2 and R3. This lowers the forward bias on Q2, so that it conducts less, causing a decreased voltage drop across emitter resistor R5. As a result, the forward bias on Q1 is also decreased, so that its conduction is lowered sufficiently to return the output voltage to the nominal value. Resistor R4 connects the base of Q3 to the input side of the regulator so that any voltage fluctuations at this point can be sensed and cancelled out.

2.13.1.2 A differential amplifier is used in the comparison circuit as the base-emitter variations with temperature changes in one transistor tend to cancel the change in the other. In addition, the reference diode CR2 can be placed in a base circuit, rather than in the emitter circuit as is the case with a one-stage error amplifier. Thus, much less current is drawn through the diode, resulting in a stabler reference voltage. An emitter follower is necessary to amplify the low-current output of Q3 to provide sufficient current drive for the low-impedance base input of Q1.

Temperature compensation for CR2 is provided by silicon diode CR3. Its negative temperature coefficient counteracts the positive temperature coefficient of CR2, so that the Zener voltage remains nearly constant over a wide temperature range. Potentiometer R7 permits the output voltage from the regulator to be set precisely at +12 Vdc.

2.13.2 -12-Vdc Power Supply. - Figure 6-12 is the schematic diagram for this power supply; its reference designation prefix is A9. The ac input from power transformer T1 is rectified by silicon diodes CR1 and CR2 which are connected as full-wave rectifiers. Initial filtering of the pulsating dc output is by electrolytic capacitor C1. Transistor Q1 functions as a series regulator whose conduction is controlled by Q2. Zener diode CR3 is the emitter reference element for Q2. If, for example, the output voltage from the regulator module tends to increase, the base of Q2 goes more negative, causing it to conduct harder. This increases the voltage drop across R1 and R2 so that the base of Q1 becomes less negative, and the conduction through the transistor decreases. As a result, the voltage output from the module drops to its nominal value. A decrease in the output voltage has the opposite effect, with the base voltage of Q2 decreasing so that it conducts less. The voltage drop across R1 and R2 now decreases, causing the base voltage of Q1 to go more negative. The conduction of the regulator transistor will now increase so that the output voltage rises. Resistor R3 connects the base of the control transistor to the input side of the regulator so that fluctuations at this point can be sensed and compensated for.

2.13.3 +4.5 and -4.5 Vdc Power Supply. - Figure 6-19 is the schematic diagram for this power supply; it carries the reference designation prefix A13. Silicon diodes CR1 and CR2 rectify the ac input for the positive output and CR3 and CR4 perform the same function for the negative supply.

2.13.3.1 Transistor Q1 functions as a series regulator for the negative supply. Its conduction is controlled by Q3 which senses and responds to fluctuations of the negative output voltage from its nominal -4.5 Vdc value. Transistor Q2 serves as a constant current source for Zener diode CR7 which functions as the reference element for Q3. By providing a constant current for the Zener diode, the Zener voltage is maintained within close limits. This, in turn, improves the regulation of the negative supply. Assuming that the output voltage tends to rise (become more positive), the forward bias on the emitter of Q3 (a PNP transistor) increases since the base voltage is fixed by CR7. This causes Q3 to conduct harder, increasing the voltage drop across R2 and R3 so that the base of Q1 goes more positive. This results in a decrease in the emitter-collector resistance of Q1 since it conducts harder so that the output voltage returns to its nominal value. Should the output voltage increase in the negative direction the opposite action takes place with Q3 conducting less so that the voltage drop across R2 and R3 decreases. The base voltage of Q1 now becomes more negative resulting in an increase in the emitter-collector resistance, and a decrease in the output voltage back to the nominal value. Resistor R5 provides overload protection for the negative supply. If excessive current is drawn the voltage drop across R5 will reverse bias the base-emitter junction of Q3, cutting it off. The base voltage of Q1 then increases in the negative direction, cutting the transistor off and protecting it from damage. Diodes CR5 and CR6 are used to clamp the base of Q2 at a fixed voltage so that the transistor can function as a current source.

2.13.3.2 The series regulator for the +4.5 Vdc supply is transistor Q1 located on the main chassis. Conduction of the transistor is controlled by a feedback loop consisting of a differential amplifier, Q5 and Q6, which drives amplifier Q4, which, in turn, drives an emitter follower, Q7. The output of the emitter follower is connected to the base of the series regulator and directly controls its conduction. The output of the negative supply is used as the reference voltage for the positive supply. It is connected to a sampling network made up of R11, R12, and R13. Potentiometer R12 is used to set the positive output at precisely 4.5 volts. When properly set the base voltage of both Q5 and Q6 will be 0 Vdc. If the output voltage deviates from the set value, the difference voltage is sensed by Q6 as an error signal, and the feedback circuit supplies the series regulator with a compensating voltage to return the output to its normal value. Assuming that the output voltage drops below +4.5 Vdc, the base of Q6 will go negative. This causes Q6 to conduct less, so that the voltage drop across R7 increases in the negative direction. The forward bias on Q5 is thus increased so that it conducts harder, increasing the voltage drop across R6. Amplifier Q4, a PNP transistor, now conducts harder so that the voltage drop across it decreases so that its collector voltage more closely approaches the more positive emitter voltage. This results in an increased forward bias on emitter follower Q7 so that it conducts harder, giving a more positive voltage across its load resistor, R9. Since the base-emitter junction of the series regulator is connected across R9, its forward bias increases so that it conducts harder, lowering its collector-emitter resistance. The output voltages now rises back to its nominal +4.5 Vdc value. Should the output voltage rise above 4.5 Vdc the feedback circuit will have the opposite effect, resulting in a decreased forward bias on the series regulator, so that the collector-emitter resistance of the transistor increases and the output voltage drops to the proper value. Overload protection of the positive supply is given by resistor R10 in conjunction with silicon diodes CR8, CR9, and CR10. If excessive current is drawn from the supply the voltage

drop across R10 will forward bias the diodes so that the base of Q7 will be pulled down to the voltage at the output terminal. This will result in the base of the series regulator being driven sufficiently negative to limit the current drawn from the transistor to a safe value. Diodes CR11 through CR16 are included for temperature compensation. The negative temperature coefficient of the germanium diodes counteracts a tendency of the positive voltage to increase at elevated temperatures.

2.14 FINE TUNING REGULATOR

Figure 6-13 is the schematic diagram for the fine tuning regulator; its reference designation prefix is A10. This assembly provides a regulated output of +10 Vdc which is applied through the front-panel FINE TUNING control, R1, to voltage-variable capacitor A4A1CR2 in the local oscillator assembly. Zener diode CR1 provides the regulation of the +12-Vdc input. Silicon diode CR2 compensates for the positive temperature coefficient of the voltage-variable capacitor. That is, the capacity of the voltage-variable capacitor rises with increases in temperature. Silicon diodes have a negative temperature coefficient so that the voltage drop across them decreases with rising temperature. Thus, as the capacity of A4A1CR2 tends to increase at higher temperatures, more voltage is applied to it due to the decreased drop across CR2, maintaining the capacity nearly constant.