1KW COMMUNICATION TRANSMITTER ATS-1
TYPE 1J66400
VOL. I OF TWO
CH. 1 TRANSMITTER COMPLETE
CH. 2 EXCITER SECTION

HANDBOOK 66400R

1 kW COMMUNICATION TRANSMITTER ATS-1

Type 1J66400

19720406

Handbook 66400R
(3 Chapters)

AMALGAMATED WIRELESS (AUSTRALASIA) LIMITED,
Engineering Products Division,
422 LANE COVE ROAD, NORTH RYDE, N.S.W.

REVISION RECORD

Revision List	Date of Issue	Signature	Date of Incorporation

FORM 6000-B043

CHAPTER 1

ATS-1 TRANSMITTER COMPLETE

CHAPTER 1

TABLE OF CONTENTS

CHAPTER 1

TABLE OF CONTENTS

66400R

1 kW COMMUNICATION TRANSMITTER ATS-1

FOREWORD

This handbook has been divided into three Chapters for ease of reference. Each Chapter is divided into Parts the headings of which are listed below. The Parts are divided into sections and sub-sections, the details of which can be found in the table of contents at the front of each chapter.

Chapter 1. ATS-1 TRANSMITTER COMPLETE

- Part 1 - General Description
- Part 2 - Installation and Setting Up Instructions

Chapter 2. ATS-1 EXCITER SECTION

- Part 1 - General Description
- Part 2 - Principles of Operation
- Part 3 - Circuit Description
- Part 4 - Alignment Procedure
- Part 5 - Maintenance and Repair
- Part 6 - Component Schedule
- Part 7 - Diagrams and Drawings

Chapter 3. ATS-1 LINEAR AMPLIFIER SECTION

- Part 1 - Technical Description
  1. R.F. Section
  2. Power Supplies
  3. Power Control
  4. Automatic Tuning
- Part 2 - Maintenance and Repair
- Part 3 - Component Schedule
- Part 4 - Diagrams and Drawings

PART 1

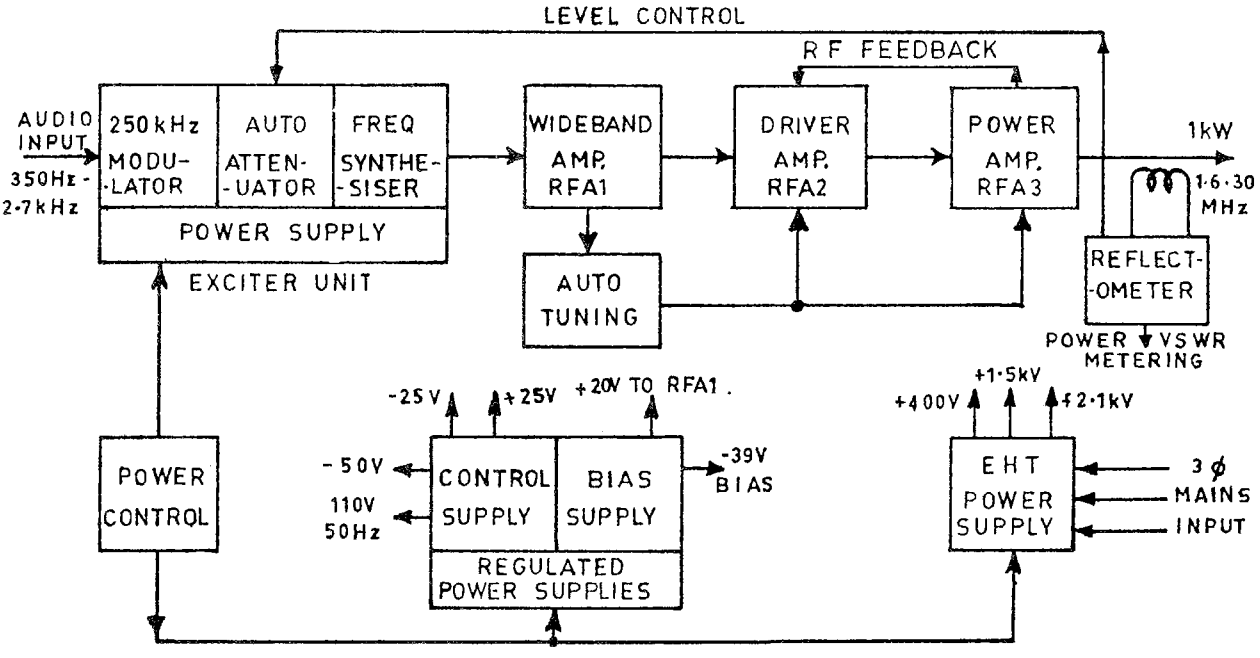
GENERAL DESCRIPTION

1. INTRODUCTION

The AWA Communication Transmitter ATS-1, type 1J66400, is a servo tuned h.f. equipment designed to operate in the 1.6 MHz to 30 MHz frequency band and is capable of producing an output of 1 kW p.e.p. (continuous duty) employing ceramic tetrodes for the power amplifier and its driver amplifier; the remainder of the equipment uses solid state devices for r.f. signal generation, amplification, rectification and control.

It may be used in a fixed or transportable communication system in A1, A3, A3A, A3H and A3J transmission modes on nine pre-determined channel frequencies, and may be tuned and operated locally or interfaced with a suitable remote control system. Manual, override tuning is readily available from the front of the equipment for emergency operation.

The transmitter is forced-air cooled and is suitable for use in tropical climates.



66400G2-1

A T S-1 TRANSMITTER BLOCK DIAGRAM

2. PRINCIPLES OF OPERATION

The functional block diagram below broadly outlines the principles of operation of the transmitter.

The input to the transmitter is a d.c. keying or audio frequency signal in the 350 Hz - 2700 Hz range and is applied to the exciter unit which generates the transmission mode and frequency which have been programmed in nine plug-in printed boards in the control unit. Provision is made for manual override of the programmed transmission mode to another mode, on any channel. The plug-in printed boards may be readily re-programmed to another channel frequency and/or mode.

The exciter employs a highly stable digital frequency synthesiser providing output frequencies in 100 Hz steps which are related to an internal 1 MHz reference. The audio input signal is applied to a sideband generator after amplification in an auto-attenuator module. The latter module is also fed a sample of the transmitter output from the reflectometer which is used to automatically control the exciter output level.

The r.f. signal from the exciter is fed to linear amplifier stages, the first stage being a wide band solid state amplifier (RFA1) and then to a driver amplifier stage (RFA2) consisting of a single type 8122 ceramic beam power tetrode. The power amplifier stage (RFA3) uses three type 8122 valves connected in parallel operating in class AB1. Inverse feedback between RFA3 and RFA2 ensures good linearity, while a gain limiter module provides protection against high anode currents during tuning operations. The gain limiter samples operating conditions of RFA2 and RFA3 and if excessive, provides a control voltage to reduce the gain of the wideband a.g.c. amplifier, RFA1.

The transmitter output is fed to the antenna via a reflectometer which is used for:

(a) Measurement of transmission line v.s.w.r.

(b) Measurement of r.f. power output

(c) Overload protection of the equipment in the event of transmission line failure or v.s.w.r. in excess of 3:1

(d) Development of a control voltage which relates the r.f. output level to the output from the first modulator in the exciter unit and is set by the AUTO GAIN control on the control panel. It is applied to the auto-attenuator providing automatic level control and

(e) External indication of power output falling by more than 3 dB.

An automatic tuning system is incorporated to tune the variable capacitors and inductors in the driver and power amplifier stages. Coarse and fine tuning by servo amplifier controlled motors is employed. During coarse tuning the output of the wideband pre-amplifier is suppressed and the tuning motors are activated by the output of a frequency discriminator. On completion of coarse tuning, the suppression is removed from the wideband amplifier and applied to the frequency discriminator. Fine tuning is accomplished by comparing the

input and output phases of the driver and power amplifier stages respectively in phase discriminators and using the voltage produced to drive the appropriate tuning motors. Automatic transmitter loading is inherent in the servo tuning system employed. The input and output r.f. voltage of RFA3 are compared in an amplitube discriminator, the control voltage so produced being used to drive the loading servo motor via an associated servo amplifier. Manual tuning is possible should a fault occur in the automatic system. Any selected frequency within the operating band will be self-tuned within 10 seconds, the average time for a frequency change being three seconds, while adjacent frequencies are tuned in one second.

The incoming 380 V/440 V, 3-phase, 50 Hz mains supply is fed via circuit breakers located across the lower front of the transmitter cabinet. The power control unit controls the application of the mains supply to the power supply units in an ordered switching sequence the progress of which is indicated by lamps: overload and fault conditions are similarly indicated. A lamp test facility is provided for all indicator lamps. Front panel and removable chassis safety interlock switches, grounding of high voltage circuits and aerial interlock switch provide protection for operating and maintenance personnel.

3. EQUIPMENT UNITS

The main component units of Transmitter ATS-1, type 1J66400 together with associated sub-unit type numbers and circuit prefixes are as follows:

Unit	Type	Prefix
R.F. Unit, comprising:	1J66402	1
R.F. Amplifier Assembly - RFA2 and RFA3	1J66414	1
R.F. Pre-Amplifier RFA1 and Frequency Discriminator	1R66415	2
Gain Limiter	1R66416	7
Phase Discriminator (2)	3J64629	-
Amplitude Discriminator	4J64629	-
VHF Filter	1Q66429	1
Servo Amplifier (3)	2G64639	-
Servo Control Unit and Motor Supply, including:	1J66410	6
Servo Control Board	1R66428	6
RFA2 Tuning Assembly, including:	1J66460	10
Tuning Servo Drive Unit	1R66413	10
Inductor Assembly	1V66461	10
RFA3 Tuning Servo Assembly, including:	1R66411	12
Inductor Assembly	1V64632	-
RFA3 Loading Servo Assembly	1R66412	11
Dial Assembly (3)	2R64638	-
Grounding Switch	2R64634	1
Reflectometer	1J66408	8
Exciter Unit (refer Chap.2 Part 1 for details)	1J66409	9
Transmitter Control Unit, comprising:	1P66406	4
Transmitter Control Board	1R66423	4

Unit	Type	Prefix
Lamp Test Board	1R66424	4
Metering Resistor Board	1R66425	4
Channel Select Board (9)	1R66426	4
R.F. Monitor Board	1R66427	4
Power Supply Unit, comprising:	1H66403	3
Rectifier Assembly (3)	1H66404	-
Zener Diode Assembly	1H66419	3
E.H.T. Metering Resistors	1R66420	3
Grounding Switch	2R64634	3
Regulated Power Supplies, including:	1H66417	5
Bias Supply Board	1R66421	5
Control Supply Board	1R66422	5

4. PILOT LAMPS

Transmitter operating and fault conditions are visually displayed by pilot lamps mounted on the power control unit front panel, which indicate the steps in the switching and tuning sequences and also give an indication of the location of a fault condition. The lamp bezel colours, functions and circuit identification are:

Colour	Function	Circuit Ident.
Green	LT	4LP13
	BIAS	4LP7
	DELAY	4LP6
	REMOTE	4LP14
Amber	POWER-LOW	4LP30
	TUNE COARSE	4LP1
	TUNE FINE	4LP2
	GAIN LIM	4LP9
	O/L FAULT RFA2	4LP3
	O/L FAULT RFA3	4LP4
	O/L FAULT R.F. LINE	4LP5
	CHANNEL 1	4LP16
	2	4LP17
	3	4LP18
	4	4LP19
	5	4LP20
	6	4LP21
	7	4LP22
	8	4LP23
	9	4LP24

Colour	Function	Circuit Ident.
Amber (cont'd)	EMISSION A1	4LP25
	A3	4LP26
	A3A	4LP27
	A3H	4LP28
	A3J	4LP29
Red	HT	4LP8
White	AER I/L	4LP10
	TUNE FAIL	4LP11
	HT I/L	4LP12
	HT LOCKOUT	4LP15

5. SWITCHES

There are two groups of switches on the front of the transmitter, excluding safety interlock switches. The group across the lower front are all hydraulic-magnetic circuit breakers used for a.c. mains switching, the MAINS and MAIN HT switches being 3-pole and the remainder single pole. The second group are operational and are located on the control panel. Switches with functions and circuit identification are :

	Function	Circuit Ident.
Mains Control	MAINS	3CBM
	BLOWER	3CBF
	FILAMENTS	3CBL
	BIAS REGULATOR	3CBB
	MAIN HT	3CBH
	TUNING MOTORS	3CBS
	CONTROL REGULATOR	3CBC
	EXCITER	3CBX
Control Panel Pushbutton	LAMP TEST	4SWD
	LAMP TEST	4SWM
	START	4SWE
	O/L FAULT - CLEAR	4SWF
Toggle	LT	4SWB
	HT	4SWC
	TEST KEY	4SWN
	POWER HIGH-LOW	4SWO
	FEEDBACK	4SWG
Rotary	MULTIMETER (24 position)	4SWA
	CHANNEL (9 position)	4SWJ
	LOCAL/REMOTE (2 position)	4SWK
	EMISSION (6 position)	4SWL

6. METERING FACILITIES

Metering facilities are provided on the control panel for the following:

(a) Hourmeter (RFA2 and RFA3 filaments) (4M4)

(b) RFA3 CATHODE (4M2) 0 - 1.5 A

(c) POWER OUTPUT kW (4M3) 0 - 2 kW

(d) A switched multimeter (4M1) indicating:

Position	Metering
1	CONTROL 0 - 50 V+
2	CONTROL 0 - 50 V-
3	EXCITER 0 - 10 V+
4	EXCITER 0 - 50 V+
5	EXCITER 0 - 50 V-
6	RFA2 CATH 0 - 0.5 A
7	RFA3A CATH 0 - 0.5 A
8	RFA3B CATH 0 - 0.5 A
9	RFA3C CATH 0 - 0.5 A
10	RFA3 SCREEN 0 - 100 mA
11	OFF
12	FORWARD POWER
13	REFLECTED POWER
14	RFA3 OUTPUT
15	RFA2 OUTPUT
16	RFA1 OUTPUT
17	EXCITER OUTPUT
18	EHT 0 - 2.5 kV
19	SCREEN 0 - 500 V
20	BIAS 0 - 100 V
21	RFA1 SUPPLY 0 - 50 V

7. REMOTE CONTROL FACILITIES

Facilities are provided for remote control of low tension and high tension switching and selection of emission mode and pre-set channel frequencies. Control is transferred to the remote control point by the LOCAL-REMOTE switch on the control panel, indication that control has been extended being provided by the green REMOTE lamp.

The following terminations are provided in the control unit for extension of switching and lamp indication to remote control as required: -

Switching		Indication
4SKQ4	LT ON	4SKQ5 LT ON

Switching		Indication
4SKQ1, 2 & 3	POWER HIGH-LOW (includes HT OFF)	4SKQ6 HT ON
4SKP5	KEY	4SKQ7 RF ON
4SKM1 to 10	CHANNEL SELECTION	4SKQ10 TUNE FAIL
4SKM12 to 14 & 16 to 18	EMMISSION SELECTION	4SKQ11 REMOTE AVAILABLE
4SKN1 to 27	ANTENNAE SELECTION (via channel relays) (C/O contact 1)	
4SKN28	ANTENNA I/L	
4SKQ8 & 9	ALARM (circuit closed between terminations during HT lockout)	

8. PERFORMANCE SUMMARY

Frequency Range :	1.6 MHz to 23 MHz to specification below and 23 MHz to 30 MHz to C.C.I.R. performance specification
Frequency Stability :	±10 Hz from -10°C to +50°C
R.F. Power Output :	1 kW p.e.p. (continuous duty) 250 W carrier on a.m.
Output Load Impedance :	75 ohms unbalanced (maximum v.s.w.r. 3:1)
Emission Modes Available :	A1 c.w. A3 d.s.b. A3A s.s.b. (upper sideband) reduced carrier A3H s.s.b (upper sideband full carrier (compatible a.m.) A3J s.s.b. (upper sideband suppressed carrier
Harmonic Radiation :	Second Harmonic better than 50 dB below fundamental, higher order harmonics 55 dB below fundamental
Linearity :	Intermodulation distortion at least 35 dB below either tone of a two-tone test signal up to 1 kW p.e.p.
Wideband Noise : (for 3 kHz bandwidth)	-100 dB relative to p.e.p. at frequencies greater than 30 kHz away from assigned frequency
Audio Frequency Response :	350 Hz - 2700 Hz ±2 dB
Audio Input Level :	+10 dBm to -20 dBm
Limiting :	Output variation of ±1 dB for input level variations of ±10 dB
Audio Input Impedance :	600 ohm
A.M. Distortion :	Better than 5% at 85% modulation
A.M. Noise :	-50 dB relative to p.e.p.

Main Frequency Filtering :	-50 dB at 50 Hz
Test Tones :	Approximately 1100 Hz and 1600 Hz
Power Input (a.c.mains) :	380 V, 400 V, 415 V or 440 V, 3-phase four wire at 50 Hz, 3 kW input at 0.9 power factor. Tolerable voltage variations of ±10% from nominal without external regulator. Tolerable frequency variation ±3 Hz
Air Flow :	150 c.f.m.
Environmental Conditions:	Operating and storage temperature -10 °C to +50 °C at up to 50% relative humidity and up to 40 °C at 95% relative humidity
Dimensions :	Approximately 64 in high (162.5 cm) 23.1/4 in wide (59 cm) 20.1/2 in deep (52 cm)
Weight	508 lb (231 kg)
Equipment Schedule :	One AWA Communication Transmitter ATS-1 type 1J66400 One set working valves type 8122 (qty 4) One Instruction Handbook 66400R

9. MECHANICAL CONSTRUCTION

9.1 General

The transmitter is self-contained in a cabinet fabricated from heavy gauge sheet aluminium mounted on a rigid base. Access to all components is achieved by opening front panels only. The majority of the units are slide in and readily removed from the cabinet, in other cases removal requires the disconnection of multipin connectors and of cabling from easely accessible terminal strips. Most printed circuit boards are plug-in.

The cabinet is divided into four main sections, the lower section housing the e.h.t. and regulated power supplies and the blower. The r.f. section including automatic tuning assemblies is immediately above the power supplies with the exciter unit located in the next compartment above. The top section, behind the control panel houses the transmitter control unit.

Access to the three tuning dials for manual tuning is provided under movable metal slides on the r.f. section front panel, manual tuning crank handles are supplied with the equipment. Tuning dial readings are visible through small perspex windows.

9.2 Control Unit

The control unit is a removable unit, connections being made to the cabinet

9.2 Control Unit (con't.)
wiring via multipin connectors and by a coded wire cable form and terminal strip. It contains plug-in printed boards for power control and overload circuitry and for channel emission selection. Control switches, indicator lamps and four meters, which includes multimeter 4M1, are mounted on the front panel. The unit is retained in the cabinet by front panel knurled retaining secrew.

The reflectometer is mounted at the rear of the cabinet behind the control unit and adjacent to the transmission line entry.

9.3 Exciter Unit

The exciter unit is mounted behind a hinged front panel and consists of eight plug-in modules of which the multipin board connectors provide the interconnection between modules. The large module at the right hand end is the unit power supply with mains entry via a four pin connector on the front panel. The modules may be withdrawn and operated by means of a service tray and r.f. cables supplied.

The modules are normally secured by a retaining bar across the front of the unit and if desired the entire exciter may be withdrawn from the cabinet, for external operation, by removing the two securing screws at each end of the unit.

9.4 R.F. Amplifier Assembly

The r.f. amplifier assembly is located in the lower left of the r.f. unit. It comprises RFA1 and frequency discriminator board fixed mounted at the lower right of the assembly, RFA2 and RFA3 amplifier stages with associated phase and amplitude discriminator boards and a small panel to the left of the RFA1 board on which is mounted the four pre-set bias resistors 1RV2 to 1RV5 and preset frequency discriminator inductor 1L22 and capacitor 1C86.

The r.f. amplifier assembly is held in position by twelve slide clips. Connection to the cabinet wiring is via 1SKH/1PLH and to the RFA2 tuning assembly via silvered spring contacts. R.F. IN and R.F. MONITOR coaxial connectors, 1SKA/13PLC and 1SKB/13PLD respectively, are located on the shelf adjacent to 1SKH. EHT connection is made by a removable connector plate on the upper right hand rear side of the RFA3 valve assembly. Adjustable r.f. pick-up plates are spaced on RFA3 anodes, on the left hand side, 1C42, 1C44, 1C46, and 1C47 are used for neutralising, ampitude discriminator, r.f. monitor and phase discriminator respectively. The long pick-up plate at the right, 1C43, is used for feedback.

The filament transformer for 1V1 to 1V4 is mounted on a vertical panel in the centre of the bottom shelf of the r.f. unit.

9.5 Gain Limiter

This is a removable plug-in unit, located above the loading servo drive unit,

9.5 Gain Limiter (con't.)
connected to the cabinet wiring via multipin strip connector 1SKK/7PLA. It contains a printed wiring board with four pre-set resistors 7RV1 to 7RV4 and GAIN LIMITER ON-OFF switch, 7SWA1, mounted on a small front panel. The unit is secured in position by a knurled locking screw in the centre of the front panel. An extender card is supplied.

9.6 Tuning Assemblies RFA2 and RFA3

The RFA2 tuning assembly consists of a rotating form inductor, 10L9, gear coupled to parallel connected 3 gang variable capacitor 10C14. Capacitor 10C13 is mounted forward of 10C14 to which it is connected by an extension drive shaft. The RFA3 and loading tuning assemblies are both variable spiral form inductors coupled to variable ceramic vacuum capacitors and are 1L17/1C61 and 1L18/1C6 respectively. The inductors are located on the rear wall of the r.f. unit, 1L17 above the servo control unit and 1L18 behind the r.f. amplifier assembly.

9.7 Servo Drive Assemblies

Three servo drive assemblies are used and are basically similar to each other except for the method of drive to the separately mounted inductors and capacitors. The tuning of the variable components and rotation of the dial is by gearing driven by a servo motor. The manual tuning crank-handle engages in a keyway in the centre of the dial.

A drive shaft couples RFA2 tuning inductor 1L7 and capacitors 1C13 and 1C14 to the drive assembly.

Belt drives are used to couple the drive assemblies to the drive shafts of RFA3 tuning inductor 1L17 and capacitor 1C61 and to loading inductor 1L18 and capacitor 1C62.

9.8 Servo Amplifiers

The servo amplifier assembly is located between the RFA3 and loading servo drive assemblies and is fixed in position. It contains the three plug-in amplifier boards which may be removed by withdrawing to the right. Load comparator pre-set resistor 1RV6 is mounted on the assembly front panel.

9.9 Servo Control Unit

This is a removable unit located at the lower right of the r.f. unit and retained in position by two spring loaded thumb screws. It is connected to the cabinet wiring via 6SKG/1PLA and contains the servo control plug-in printed board at the front and the servo motor power supply at the rear. Contactor 6PS is also mounted on this unit. Connector 6SKG and COARSE-NORMAL-FINE switch, 6KSA, are mounted on a narrow horizontal panel immediately behind the printed board.

9.10 EHT Power Supply

The large components comprising the e.h.t. power supply transformer, 3TR1, and filter capacitors 3C1 to 3C4, are mounted on the floor of the cabinet: thyrectors 3VS1 to 3VS3 are located on an insulating strip fixed to the right hand side of 3TR1. The three rectifier assembly boards are mounted on the cabinet right hand wall with the zener diode assembly, 3MR37 to 3MR40, at the rear.

Filter choke 3L1 is floor mounted in the left hand rear corner with the bleeder resistors immediately above.

9.11 Regulated Power Supplies

This is a removable unit located at the left and on the floor of the cabinet: it is retained in position by two spring loaded thumb screws at the front. Connection to the cabinet wiring is via coded cables connected to terminal strips 5TSA and 5TSB.

It consists of two power transformers, 5TR1 and 5TR2, and filter capacitors 5C1 to 5C4, the rectifier and regulator circuitry is provided by two printed boards.

9.12 Blower

The blower is mounted under the shelf immediately below the RFA2 tuning assembly and provides an air draft across the e.h.t. supply via the filter on the cabinet lower front panel. The air is passed upwards through the valve anode cooling fins of the r.f. amplifier assembly and is discharged via the rectangular metal air duct at the left rear of the cabinet in which is located the air flow switch. Air is also circulated throughout the cabinet for general cooling.

10. POWER SUPPLIES

Silicon rectifiers are used throughout. Rectifier outputs are shunted by bleeder resistors to ensure rapid discharge of filter capacitors. Thyrectors are used across transformer primaries to reduce the effect of mains voltage transients.

The outputs from the various power supplies are as follows:

Extra High Tension (EHT) Power Supply (1H66403):	A three phase full wave circuit supplying: +2.1 kV to RFA3 anodes +1.5 kV to RFA2 anode +400 V zener stabilised for RFA2 and RFA3 screens
Regulated Power Supplies (1H66417):	Four single phase bridge rectifier circuits supplying :

10. POWER SUPPLIES (con't.)

	-39 zener stabilised grid bias for RFA2 and RFA3 +20 V regulated for RFA1 and the frequency discriminator +25 V and -25 V regulated for power control -50 V for channel and emission select circuits 110 V 50 Hz for power contactors
Exciter Power Supply (1H66430)	Three single phase bridge rectifier circuits supplying: +24 V and -24 V unregulated +15 V regulated -15 V zener stabilised +5 V regulated
Servo Control Unit Power Supply :	Three single phase bridge rectifier circuits supplying: +18 V/O/-18 V for RFA2 tuning servo +24 V/O/-24 V for RFA3 tuning servo +24 V/O/-24 V for RFA3 loading servo

11. COOLING AND VENTILATION

The transmitter and in particular the r.f. section is cooled by forced air draught from a blower mounted in the power supply section of the cabinet. Metal ducting passes the hot air to the exhaust duct on the top of the cabinet, from where it may be routed away if necessary. Air intake is through a washable filter at the bottom front of the cabinet.

12. PERSONNEL AND EQUIPMENT PROTECTION

Protection of personnel and equipment is afforded by grounding switches, interlock switches, overload circuitry and a blower operated air flow switch.

Two grounding and three interlock switches are fitted to the cabinet framework and are activated by removal of the access panel in front of the power supply section or by either of the two small cover panels in the r.f. section adjacent to and on each side of the servo drive assemblies except that the right hand panel activates an interlock switch only. When any of these panels is removed the h.t. lockout circuit is activated and in turn disables the "h.t. on" circuit preventing application of h.t. to the transmitter. The mechanically operated grounding switches discharge the e.h.t. filter capacitors. An aerial interlock switch will also disable the "h.t. on" circuit if activated at the aerial exchange. Indication of an interlock fault and h.t. lockout is provided by white lamps on the control panel.

Loss of air pressure in the cooling system due to faulty blower operation or by removal of the r.f. unit metal covers causes the air flow switch to release

12. PERSONNEL AND EQUIPMENT PROTECTION (con't)
and the filament, bias and h.t. supplies to be switched off.

An overload occurring in the circuits of RFA2 or RFA3 or a fault in the transmission line causes the h.t. to be removed and re-applied after one second. Three such re-applications of h.t. are made, after which, if the overload persists, h.t. is locked out. The appropriate amber lamp, O/L FAULT, will remain alight after the initial fault. HT LOCKOUT is indicated by a white lamp on the control panel.

To reapply h.t. after an interlock or overload fault it is necessary to set the HT toggle switch on the control panel off, and then set the same switch on again. If the transmitter is remotely controlled, re-application of h.t. is similarly achieved by setting the remote HT switch to OFF and then to ON. The O/L FAULT lamps may be cleared at any time by operation of the fault CLEAR pushbutton switch.

Failure of the bias supply causes the h.t. supply to be switched off and the green BIAS indicator lamp on the control unit to be extinguished.

13. LIST OF RECOMMENDED TEST EQUIPMENT

For complete alignment of the transmitter and exciter and for thorough service and maintenance work the following test instruments and equipment or equivalents will be required. A list of miscellaneous items is also included.

1.	Multimeter, sensitivity not less than 20 kΩ/V and accuracy ±5%	AVO Model 8
2.	R.F. Millivoltmeter	H.P. type 411A with open and V.H.F probes
3.	Vacuum Tube Voltmeter	AWA A56074 H.P. 411A
4.	Signal Generator, A.F.	AWA A57100 (2 off)
5.	Signal Generator, R.F.	Marconi TF2002 (2 off) H.P. 608D (V.H.F.) (2 off)
6.	Level Measuring Set	Wandel and Goltermann PSM-5
7.	Frequency Counter	G.R. 1192 H.P. 5245 with V.H.F. converter
8.	Spectrum Analyser	H.P. fitted with 140T display, 1552B I.F. section, 8553B and 8554L R.F. sections

13. LIST OF RECOMMENDED TEST EQUIPMENT (con't.)

9.	Distortion and Noise Meter	AWA F240
10.	Cathode Ray Oscilloscope	Telequip S34 Tektronix 454 Tektronix 535A with CA plug-in (0A1094)
11.	Gain Measuring Attenuator	AWA 3R8030
12.	D.C. Power Supply (Regulated)	Perini-Scott T30-2C (2 off)
13.	Auto-Transformer	Variac V5
14.	Vernier Potentiometer	10 kΩ Beckman Model A fitted with RB series turns counting dial
15.	Test Load	75 Ω - 1 kW capacity

Miscellaneous Items

1. Capacitors - 470 pF ±5%, 500 VDCW, metallised mica, style CM06
   1200 pF ± 5%, 500 VDCW, metallised mica style CM06

2. Resistors - 3.3 Ω ±10%, 10 W, wirewound, style RWV5-J
   33 Ω ±10%, 10 W, wirewound, style RWV5-J
   220 Ω ±5%, 3W, wirewound, style RWV4-J
   50 Ω±5%, 1/4 W, composition, grade 2, style RC7-K
   150 Ω±5%, 1/4 W, metal oxide, style RFG5-F
   270 Ω ±5%, 1/4 W, metal oxide, style RFG5-F
   1.2 kΩ ±5%, 1/4 W, metal oxide, style RFG5-F
   4.7 kΩ ±5%, 1/4 W, metal oxide, style RFG5-F
   10 kΩ ±5%, 1/4 W, metal oxide, style RFG5-F
   27 kΩ ±5%, 1/4 W, metal oxide, style RFG5-F
   47 kΩ ±5%, 1/4 W, metal oxide, style RFG5-F
   56 kΩ ±5%, 1/4 W, metal oxide, style RFG5-F

   1 kΩ ±10% 1/4 W, variable, linear
   10 kΩ ±10%, 1/4 W, variable, linear

3. Connectors - BNC "T" Adaptor
   33-way socket, ISEP 12-300-002 (2 off)
   BNC male

4. Transformer -AWA 403V57998

5. Switch, rotary, 6 position (Oak type)

6. Probe, BNC high impedance (x10)

MISCELLANEOUS ITEMS (con't.)

7. Cable, coaxial, 50 Ω type RG-58

8. Clips, alligator, miniature

14. LIST OF RECOMMENDED TOOLS

Standard Screwdrivers :	1 off 1/4 in dia x 1.1/2 in long blade 1 off 1/4 in dia x 4 in long blade
Posidrive Screwdrivers :	1 off 3/16 in dia x 3 in long blade 1 off 1/4 in dia x 1.1/2 in long blade 1 off 1/4 in dia x 4 in long blade 1 off 5/16 in dia x 6 in long blade
Hexagon Wrenches : (Allen or Unbrako)	1 off 1/16 in A/F with 9/16 in x 1.3/4 in arms 1 off 3/32 in A/F with 21/32 in x 2 in arms
Spanners :	1 off 1/4 in x 5/16 in AF - open end 1 off 3/8 in x 7/16 in AF - open end 1 off 1/2 in x 9/16 in AF - open end 1 off 1/2 in x 9/16 in AF - ring 1 off 3/4 in AF - ring and open end 1 off 7/16 in x 1/2 in BSW - ring and open end 1 off 7/16 in AF socket - 1/2 in square drive
1/2 in Square Drive Accessories :	1 off male and female extension - 3 in 1 off male and female extension - 6 in 1 off Tommy bar - 9 in.

- End of Part -

PART 2

INSTALLATION AND SETTING-UP INSTRUCTIONS

1. INSTALLATION

1.1 General

The transmitter may be delivered assembled, by road transport, ready to operate or dismantled and completely packed, as for sea transport. If the transmitter is received assembled, proceed directly to sub-sections 1.3.1 and 1.3.2 for location information, then sub-section 1.5 for external wiring instructions.

1.2 Unpacking

Unpack the equipment and check the items received against the packing list. Heavy equipment, modules and items such as valves and fragile components are packed separately. The components are labelled and numerically indexed to correspond with identical labels or stencils on the cabinet. Unpack these separate assemblies and check against the packing slip. After unpacking, group items bearing the same reference prefix. The type and circuit reference number of each valve are stencilled adjacent to its mounting position. If necessary, further identification of components may be made by reference to the component schedule in Chapter 3 Part 3 of this Handbook and the component layout diagram.

1.3 Assembling

1. Ensure that the selected site for the cabinet is level and well ventilated, with sufficient space for maintenance purposes. The transmitter may be mounted side by side with other equipment, since all operations are carried out from the front of the cabinet.
2. It is recommended that the cabinet be mounted on a 20 s.w.g. cooper plate, well bonded to the station earth system by a 20 s.w.g. copper strap, 6 inches wide.
3. Mount the cabinet in position and instal the heavy components, ensuring that they are carefully aligned.
4. Check the interlock and grounding switches for correct mechanical operation.
5. Fit all components in their correct positions and connect the leads, as indicated on the labelling.
6. Fit the modules, ensuring proper mating of connectors, where applicable or connect the leads, as indicated on the labelling.
7. Set all switches and circuit breakers to the OFF position.
8. If desired, connect the air discharge vent to the station extractor system. Do not, at this time, fit the front panels to the cabinet.

1.4 Internal Wiring Connections

1. The internal wiring is carried out in cable-forms which are attached in position inside the cabinet. Sub-assemblies removed for transportation should be reconnected to the appropriate terminal blocks in accordance with the designations on the numbered fanning strips.

1.5 External Wiring Connections (Refer Figures 3-10 and 3-11)

1. Mains supply input is terminated on terminal block 3TSD located on the cabinet rear wall in the power supply section and remote control facilities on the four multi-pin connectors 4SKM, 4SKN, 4SKP and 4SKQ located at the rear of the power control unit chassis. The external wiring terminations are listed in the table on Figures 3-10.

2. Connect the cabinet frame to the installation earth system by the shortest possible length of heavy gauge conductor. (Refer to the earthing recommendations given in sub-section 1.3.2.)

3. Make the external connections to the transmitter, via the top or bottom cabinet entries as appropriate to the particular installation. Remove and discard only the appropriate cable entry metal cover. Pierce the rubber membrane and pass through the necessary cabling.

4. Pass the 75 ohm coaxial feeder through the cable entry and connect it to the end of the reflectometer. Connect the other end of the feeder to the aerial or aerial exchange. Where an aerial exchange is used, connect the aerial interlock switch to the aerial interlock terminals 4SKN28 on the transmitter. If an external aerial interlock switch is not used, connect 4SKN28 to ground.

1.6 Final Assembly Checks

1. Before proceeding, ensure that all switches and circuit breakers are set to OFF and that the transmitter is positively isolated from the mains supply.

2. Check all external and internal wiring and connections made to components etc. during re-assembly, against the relevant circuit diagrams. It is essential that any wiring errors be detected and rectified at this stage to prevent injury to personnel or damage to equipment.

3. Adjustments on the transmitter which have been preset at the factory prior to delivery should not be altered.

4. Check connections and terminal strips for loose screws, fragments of metal, swarf and packing material which may have accumulated during installation, since this debris may give rise to fault conditions.

5. If necessary clean the transmitter, as detailed in Chapter 3, Part 2.

2. SETTING UP INSTRUCTIONS

2.1 Post Installation Checks and Adjustments

1. The transmitter has been aligned and tested prior to dispatch, however, the following checks and adjustments should be carried out to ensure that all electrical and mechanical parts are functioning correctly and also as an aid to operator familiarisation.

2. If difficulty is experienced in setting-up the control circuits, reference should be made to the Technical Description and Maintenance sections in Chapter 3, Parts 1 and 2 respectively.

WARNING: LETHAL VOLTAGES ARE PRESENT WITHIN THE TRANSMITTER AND CAUTION MUST BE EXCERCISED.

2.2 Preliminary Checks and Settings

1. Ensure that all meters are mechanically "zeroed".

2. Set the following to the positions stated:

   (a) All circuit breakers OFF

   (b) Power Control Unit:

      (i) L.T. and H.T. switches to OFF.

      (ii) LOCAL/REMOTE switch to LOCAL.

      (iii) Test keyswitch to key up position

      (iv) Power HIGH/LOW switch to HIGH

      (v) FEEDBACK switch to OFF.

   (c) Servo Control Unit:

      (i) Switch 6KSA to NORMAL

   (d) Auto-Attenuator Module (exciter unit):

      (i) MANUAL-AUTO switch to MANUAL and AUDIO INPUT switch to OFF

      (ii) R.F. GAIN control turned fully anticlockwise

   (e) Gain Limiter Unit:

      (i) GAIN LIMITER switch to OFF

3. Check that all grounding and interlock switches operate freely.

4. Check that the plastic cover underneath the power control unit is in place, also all of the mains warning covers listed below:

   (a) Power Control Unit

      (i) Over multimeter 4M1 and selector switch 4SWA

   (b) Exciter Unit

(i) Over transformer 30TR1 in the power supply module

(c) R.F. Unit

(i) Over terminal strip 4TSD on right hand wall of cabinet
(ii) Over safety interlock switches 1SWA and 1SWB

(d) Power Supply Unit

(i) Across the top and bottom connections to all circuit breakers
(ii) Over contactors 3PF, 3PH and 3PL.
(iii) Over terminal strips 3TSA, 3TSB and 3TSC on left hand wall of cabinet.
(iv) Over terminal block 3TSD on rear wall of cabinet.

(e) Regulated Power Supplies

(i) Over terminal strip 5TSA on left front of the unit.
(ii) Over transformers 5TR1 and 5TR2

2.3 Transformer Tap-Settings

The phase voltages shown in the table below, i.e. 220 V, 230 V, 240 V and 250 V approximately relate to 3-phase line voltages of 380 V, 400 V, 415 V and 440 V, respectively. Transformer taps, therefore, should be set to the voltage most closely corresponding with the local supply.

TRANSFORMER TAP SETTINGS

	Supply Tap OR line	Voltage Taps 220 V	230 V	240 V	250 V
(a)	Filaments Transformer, 1TR1				
	ID5 (red)	6	6	7	7
	ID6 (black)	5	4	5	4
(b)	Bias and RFA1 Supply Transformer, 5TR1				
	5B1 (red)	7	7	3	3
	5B2 (black)	6	2	6	2
(c)	Control Supply Transformer, 5TR2				
	5B3 (yellow)	6	6	7	7
	5B2 (black)	2	1	2	1
(d)	Servo Motor Supply Transformer, 6TR1				
	6SKG32 (blue)	4	4	5	5
	6SKG33 (black)	2	1	2	1
(e)	Exciter Supply Transformer, 30TR1				
	30SKA2 (red)	3	3	4	4

(e) Exciter Supply Transformer, 30 TR1 Continued

30SKA1 (black)	2	1	2	1

(f) E. H. T. Supply Transformer, 3TR1 (3-phase)

	Voltage Taps			
	380 V	400 V	415 V	440 V
a1 (yellow)	c2	c3	c4	c5
b1 (red)	a2	a3	a4	a5
c1 (blue)	b2	b3	b4	b5

2.4 Mains Supply Switching

1. Switch ON the three phase mains supply by MAINS circuit breaker 3CBM.

2.5 Control Power Supplies

1. Set the CONTROL REGULATOR circuit breaker, 3CBC, to ON.
2. On the control panel, set the multimeter selector to the CONTROL + and - positions, and ensure that the multimeter reads 25 V in both cases.
3. Check that the H. T. I/L lamp is lit.
4. Operate both LAMP TEST pushbuttons. Check that all other lamps are lit.

2.6 L. T. Switching and Blower Operation

1. Attach the lower front panel to the cabinet and the access covers on the r. f. unit. Check that the H. T. I/L lamp is extinguished.
2. Set the BLOWER circuit breaker, 3CBF, to ON.
3. On the control panel, set the L. T. switch to ON.
4. Check that the L. T. lamp lights, the blower starts and that, approximately 30 seconds later, the DELAY lamp lights.
5. While waiting for the above delay to elapse, check that a noticeable draught is present at the air filter and there is negligible leakage from the pressure compartment. Check that a draught is present at the exhaust vent on top of the cabinet.
6. Partially remove one of the r. f. unit access covers to permit pressure to escape. Check that the L. T. lamp extinguishes. (This checks the operation of the air flow switch.) Re-fasten the panel.
7. Check that the L. T. lamp lights and that after a while, the DELAY lamp lights.

2.7 Bias Supply and H. T. Lockout Check

1. Set the FILAMENTS circuit breaker, 3CBL, to ON. Ensure that the signal level from the exciter is zero.
2. Set the BIAS REGULATOR circuit breaker, 3CBB, to ON. Check that the BIAS lamp lights.
3. On the control panel, set the multimeter selector to BIAS and RFA1 SUPPLY in turn and check that the meter reads 75 V and 20 V respectively.

   Set Test Key switch on power control unit to key down position. Check that bias meter reading is now 39 V.
4. Set the H. T. switch to ON after the DELAY lamp lights, but do NOT close the MAIN HT circuit breaker, 3CBH, at this stage. The red HT lamp should not light.
5. Release the bottom front panel to operate the interlock switch. Check that both the H. T. I/L and HT LOCKOUT lamps light.
6. Secure the panel, set the H. T. switch to OFF, then ON again.
7. Check that both the H. T. O/L and HT LOCKOUT lamps are extinguished.
8. Set the H. T. switch to OFF.

2.8 Main HT and Cathode Current Check

1. Switch ON the MAIN H. T. circuit breaker 3CBH, and set the H. T. switch to ON.

   NOTE: If any of the O/L FAULT overload indicators lights, switch OFF the equipment. Refer to Chapter 3, Part 2 Maintenance Instructions and set-up the overload controls before proceeding with this test.
2. Set the multimeter selector to EHT and SCREEN in turn, and check that the meter reads 2150 V and 400 V respectively.
3. Set the multimeter selector to RFA3A CATH, RFA3B CATH and RFA3 CATH in turn and check that the meter reads 120 mA in each case, if otherwise, adjust bias controls 1RV3, 1RV4 or 1RV5 as appropriate to obtain this value.
4. Using the RFA3 CATHODE ammeter, check that the standing current of RFA3 is 0.36 A.
5. Set the multimeter selector to RFA3 SCREEN. Check that the meter reading is zero (no r. f. drive).
6. Set the multimeter to RFA2 CATH and check that the standing current is 150 mA, if otherwise, adjust bias control 1RV2 to obtain this value.

7. Set the H.T. and L.T. switches to OFF.

2.9 Remote Control Facilities

1. Set all circuit breakers except TUNING MOTORS, 3CBS, and EXCITER, 3CBX, to ON.

2. Set the L.T. and H.T. switches to ON and the LOCAL/REMOTE switch to REMOTE. Check that the REMOTE lamp on the transmitter lights and that the blower does not operate.

3. On the remote control unit, set the L.T. switch to ON. Check that the L.T. lamp on the transmitter lights and the blower runs.

4. When the DELAY lamp has lit, set the H.T. switch on the remote control unit to ON. Check that the H.T. lamp on the transmitter lights.

5. Set the LOCAL/REMOTE switch to LOCAL and the H.T. and L.T. switches on the transmitter to OFF. Set the H.T. and L.T. switches on the remote control unit to OFF.

2.10 Channel Frequency and Emission Mode (Refer Figure 3-8)

Before the transmitter can be put into operational service it will be necessary to prepare printed board type 1R66426 for the particular frequency and emission mode desired. Nine printed boards, one for each channel, are supplied each in a plastic bag, each bag also contains 12 silicon diodes type 1N914.

The binary coding for the required synthesiser frequency from the exciter is obtained by soldering the diodes supplied in the appropriate positions as stencilled on the printed board. For the first four digits of the frequency, the positions of the 8, 4, 2, 1 code are selected so that their total equals the digit required. For the 1 kHz and 100 Hz digits, an inverse code is used where the actual digit required is subtracted from the figure 9 to give the code digit required on the board viz. 2 is coded as 7.

As an example it will be presumed that a channel frequency of 19.5736 MHz is required, it will be necessary to solder diodes to the board in the positions shown by a cross in the table below:

10 MHz	1 MHz	100 kHz	10 kHz	1 kHz	100 Hz
2.1	8.4.2.1	8.4.2.1	8.4.2.1	8.4.2.1	8.4.2.1
x	x x	x x	x x x	x x	x x
1	9	5	7	3	6 MHz.

The desired emission mode is obtained by soldering a wire link in the appropriate A1, A3, A3A, A3H or A3J position as stencilled on the board, an earth return path is thus provided for the selected emission mode circuitry in the exciter.

Further details of the foregoing can be found in Chapter 2.

If the above checks and settings are all satisfactory, the transmitter may now be put into operational service. Manual and automatic tuning procedures are contained in the following sections of this part.

3. AUTOMATIC TUNING PROCEDURE

3.1 General

The transmitter is normally operated in the auto-tuning mode. A signal of the desired frequency, from the exciter, which also controls the input signal level, is applied to the r.f. stages causing servos to run to retune for optimum performance at that frequency. It is first necessary to set-up the transmitter which may be operated in either the LOCAL or REMOTE mode. The procedure is given below.

3.2 Preliminary Operations

1. Ensure that the transmitter output is terminated in a 75 ohm load.
2. Set the H. T. and L. T. switches to OFF and remove the centre front panel.
3. Set the following to the positions stated:
   (a) The servo control switch 6KSA to NORMAL.
   (b) The AUTO GAIN control initially to approximately half position.
   (c) The GAIN LIMITER switch to ON.
   (d) The FEEDBACK switch to ON.
   (e) The MANUAL-AUTO switch on the exciter to AUTO.
4. Refit the front panel and switch ON all circuit breakers.
5. Set the multimeter selector to EXCITOR 0-10 V+, EXCITER 0-50 V+ and EXCITER 0-50- in turn, check that the meter reads 5 V, 15 V and 24 V respectively.
6. Set the L. T. and H. T. switches to ON, and, if desired, set the LOCAL/REMOTE switch to REMOTE in which case set the LT and HT switches on the remote control unit to ON also.

3.3 Returning

1. Set the EMISSION switch to position A1.
2. Set the CHANNEL switch to the desired channel.
3. Set the TEST KEY switch to the key down position for LOCAL operation or KEY when REMOTE
4. If tuning does not start depress the START pushbutton momentarily.
5. Check that the TUNE COARSE lamp lights and observe the tuning dials, visible through the perspex panels.
6. When the tuning dials settle, check that the TUNE FINE lamp lights and the TUNE COARSE lamp extinguishes.

7. When the tuning dials settle, check that the TUNE FINE lamp extinguishes.

   NOTE: RFA3 load inductor and capacitor tuning is the last operation. The transmitter is now tuned to the new frequency.

8. Check the power output when the modulator output meter on the exciter is reading its nominal level. Readjust the AUTO GAIN control, if necessary to give an output of 1 kW peak.

4. MANUAL TUNING PROCEDURE

4.1 General

Certain conditions or malfunctioning of the equipment may require that the transmitter be manually tuned. In order to carry out manual tuning, it is first necessary to disable the auto-tuning facilities to prevent damage occurring within the servo system. Additionally, certain internal functions of the transmitter must also be inhibited. The transmitter may be operated in the LOCAL or REMOTE mode after manual tuning but can only be retuned to another channel locally. The procedure is given below.

4.2 Preliminary Operations

1. Ensure that the transmitter output is terminated in a 75-ohm load.
2. Set the H.T. and L.T. switches to OFF and the LOCAL/REMOTE switch, 4SWK, to LOCAL.
3. Remove the centre panel from the front of the cabinet and set the servo control switch, 6SKA, to NORMAL.

4.3 Manual Tuning Procedure

1. Ensure that the exciter is properly connected in the transmitter and that coaxial connector 13PLC is connected to 1SKA on the r.f. unit.
2. Set the FEEDBACK switch on the control panel to OFF, (manual tuning is otherwise impossible), and the GAIN LIMITER switch to ON.
3. Set the MANUAL-AUTO switch on the exciter to MANUAL and turn the R.F. GAIN control to zero.
4. Set the CHANNEL switch to the desired channel and switch to a two-tone test signal, F1 F2, on the exciter.
5. Set the EMISSION switch to position A3J.
6. Set the tuning controls to the positions appropriate to the frequency selected, as determined from the tuning charts (Figures 3-1, 3-2 & 3-3).
7. Switch ON all the mains supply circuit breakers, except TUNING MOTORS, and set the L.T., H.T. and TEST KEY to ON.

8. Set the multimeter selector to RFA1 OUTPUT and adjust the R. F. GAIN control for a meter reading of 4. 0 divisions.

9. Set the multimeter selector to RFA2 OUTPUT and tune RFA2 for a maximum reading on the meter. Limit RFA3 cathode current to 0. 5 A by adjusting the R. F. GAIN control.

10. Set the multimeter selector to RFA3 OUTPUT and tune RFA3 for a maximum reading on the meter. Limit RFA3 cathode current to 0. 5 A by adjusting the R. F. GAIN control. Monitor the r. f. output on an oscilloscope, connected to 1SKB, to ensure that the r. f. envelope is not being clipped by incorrect operating conditions.

11. Slowly increase RFA3 cathode current to 1. 0 A by adjusting the R. F. GAIN control. If the transmitter is correctly tuned RFA3 screen current should be approximately 5 mA and the average power, measured on a test load should exceed 0. 5 kW, the indication on the power output meter will be approximately 0. 35 kW.

12. If the above conditions are not obtained, slightly adjust RFA3 loading, then retune RFA2 and RFA3. Repeat these adjustments until the required output is obtained.

    NOTE: After tuning, the input level is adjusted by the R. F. GAIN control. The above procedure simulates auto-tuning for a given load impedance where the resulting output is acceptable if it exceeds 1 kW p. e. p.

13. Set the FEEDBACK switch to ON and increase the R. F. GAIN control setting to maintain the power output at the required level.

14. Set the MANUAL-AUTO switch to AUTO. Check the power output when the modulator output meter is reading its nominal level. Readjust the AUTO GAIN control, if necessary, to give an output of 1 kW.

- End of Part -

CHAPTER 2

ATS-1 EXCITER SECTION

CHAPTER 2

TABLE OF CONTENTS

CHAPTER 2

TABLE OF CONTENTS

CHAPTER 2

TABLE OF CONTENTS

CHAPTER 2

TABLE OF CONTENTS

CHAPTER 2

TABLE OF CONTENTS

CHAPTER 2

TABLE OF CONTENTS

Part 7 DIAGRAMS

CHAPTER 2

TABLE OF CONTENTS

Part 7 Continued

PART 1

GENERAL DESCRIPTION

1. INTRODUCTION

The Exciter Type 1J66409 is part of the 1 kW Communications Transmitter ATS-1 and provides a highly stable source of r.f. drive at the selected channel frequency, modulated according to the selected emission mode.

The Exciter incorporates a digital frequency synthesiser which employs two phase locked loops which make possible an exciter output frequency directly related to the internal 1 MHz frequency reference in steps of 100 Hz. An external 1 MHz master frequency source can be connected to the Exciter and selected for use in place of the internal source. Frequency and emission mode selection are made by switched digital control inputs derived either from the transmitter channel selection circuits or remotely via an interface.

The Exciter also incorporates an Auto Attenuator unit which maintains overall system gain to a preset level according to a transmitter output level indication fed to the unit.

The Exciter incorporates its own power supply which receives only mains input from the transmitter switching system.

2. PERFORMANCE SUMMARY

Frequency Range:	1.6 MHz to 23 MHz in 100 Hz steps to the following specification and 23 MHz to 30 MHz in 100 Hz steps to C.C.I.R. specification
Emission Modes Available:	A1 c.w. ON/OFF keyed
	A3 d.s.b. amplitude modulation
	A3A s.s.b. (upper side band) reduced carrier
	A3H s.s.b. (upper side band) full carrier (compatible a.m.)
	A3J s.s.b. (upper side band) suppressed carrier
Harmonic Radiation:	Second harmonic approximately 36 dB below fundamental with further attenuation for higher order harmonics
Frequency Stability: (using in-built master oscillator)	

(a) Long term:	24 hours ±1.5 in 10^8. Aging +5 in 10^8 per month
(b) Short term:	One second ±5 in 10^9. Phase jitter, 10 ms sampling r.m.s. deviation less than 3^o.
Wideband Noise: (for 3 kHz bandwidth)	-90 dB relative to p.e.p. at frequencies greater than 30 kHz away from assigned frequency; -100 dB relative to p.e.p. at frequencies greater than 100 kHz away from assigned frequency
Audio Frequency Response:	±2 dB 350 Hz to 2700 Hz
Audio Input Level:	+10 dBm to -20 dBm (preset)
Limiting:	Output variation ±1 dB for input level variations of ±10 dB
Audio Input Impedance:	600 ohm, return loss better than 20 dB
A.M. Noise:	-50 dB relative to p.e.p.
Mains-Frequency Sideband Filtering:	-50 dB relative to p.e.p. at 50 Hz
Test Tones:	Approximately 1100 Hz and 1600 Hz
Power Input:	240 V, 50 Hz (also available for 60 Hz mains supply)
Climatic Conditions:	-10 ^{o}C to +50 ^{o}C at up to 50% relative humidity, and 95% relative humidity at 40 ^{o}C.

3. COMPOSITION

The Exciter 1J66409 comprises a frame (with associated components), a filter box, and eight plug-in modules each of which comprises a frame (with associated components in some cases) and one or more printed circuit boards.

Each module has an identifying number printed on the front panel. This number is the last two digits of the A.W.A. type number for the module and is called the "prefix" number. Each of the associated printed circuit boards has a similar "prefix" number. The frame of the module may have a separate type number, and therefore a different prefix number, to the module. The prefix numbers precede the associated circuit reference numbers in the Component Schedule which is arranged in numerical sequence of prefix number to facilitate reference.

The composition of the Exciter is laid out below:

	Prefix
Exciter 1J66409, comprising:	9
(a) Filter Box 1Q66457	57

(h)	S.S.B. Generator Module 1J66454 containing:	54
	S.S.B. Generator Board 1R66439	39
(j)	Power Supply Module 1H66430 containing:	30
	Power Supply Board 1R66456	56

4. MECHANICAL CONSTRUCTION

4.1 General

The exciter unit is mounted in the ATS-1 transmitter cabinet immediately below the control panel and concealed behind a hinged, pull-down metal panel. With the panel open, the front panels of the exciter modules are visible and all front panel controls, connectors and meter are accessible. Withdrawal of modules is prevented by a restraining bar fixed in position in front of the module withdrawal knobs by two knurled screws. The exciter unit slides into the transmitter cabinet on two metal rails and is secured by the side flanges in the normal rack manner.

4.2 Frame

The frame of the exciter unit is a standard 7-inch high, flange mounted subrack constructed from ISEP components and fitted with top, bottom and rear covers. On the inside of the rear cover is mounted the Filter Box 1Q66457. The bottom and top covers are perforated to allow a cooling air passage through the unit from holes in the transmitter air ducting beneath the exciter. Modules slide in along plastic runners at top and bottom of the frame and, with the exception of the power supply, connectors at the rear of the modules mate with 33-way connectors mounted between the rear rails of the frame. The mating connectors for each module incorporate a particular indexing form to prevent registration with any other connector. Connection to the power supply module is via an 11-way cable mounting connector which is attached to a flying cable harness protruding from a grommet in the rear panel.

4.3 Modules

The front panels of all modules are finished in flat black enamel and are lettered with the module prefix number in white at the top. The module prefix numbers are also lettered along the top front rail of the exciter frame to facilitate replacements.

All modules may be withdrawn from the front of the exciter after removal of the retaining bar. To facilitate withdrawal of modules, a knurled knob is fitted to each module at the bottom of the front panel.

The 2nd I.F. Loop (51), Pulse Swallower (52), Phase Comparator (53), Auto Attenuator (55) and S.S.B. Generator (54) modules each comprises a printed circuit board mounted by means of spacers to a vertical aluminium panel which is folded at the front to form the front panel. The 33-way ISEP connector is attached to the printed circuit board at the rear of the module.

The module slides into the frame with the printed board in two ISEP plastic guides at top and bottom.

The V.C.O. (63) and Frequency Translator (64) modules each comprises a vertical brass panel attached at right angles to the rear of an aluminium front panel to form a "T" shaped frame. The individual printed circuit boards are contained in metal boxes attached to both sides of the panel. The box lids are secured by screws and are stencilled with the printed circuit board prefix. The 33-way ISEP connector is attached to the rear of the panel. The module slides into the frame with the vertical panel in two ISEP plastic guides at top and bottom.

The power supply module (30) comprises a vertical aluminium panel folded at the front to form a front panel. The assembly is fitted with a base plate, perforated for air passage, and an auxiliary vertical panel.

The power transformer is mounted on the base plate at the rear of the module. The large filter capacitors are mounted vertically on the base plate between the two vertical panels. The smaller components, along with the power transistors and heatsinks, are located on a printed circuit board mounted on the auxiliary panel. The 1 MHz master oscillator is mounted vertically, immediately behind the front panel to the left; the frequency adjustment controls are accessible through a hole provided in the front panel. Mains power is connected to the module via a four-way connector on the front panel. Internal connections to the module are made via an 11 way connector mounted in the inside top right-hand corner behind the front panel. The mating connector is mounted on a cable harness which is not attached to the frame members and the module may be withdrawn far enough for the connector to be un-plugged and then the module can be completely withdrawn. The module slides into the frame on two ISEP plastic runners, both mounted between the front and rear bottom rails of the frame.

4.4 Dimensions

The overall dimensions of the assembled exciter unit are as follows:

Width (including flanges) :	520.7 mm	(20.1/2 in)
Width (excluding flanges) :	476.25 mm	(18.3/4 in)
Height:	177.8 mm	(7 in)
Depth (including knobs etc.) :	406.4 mm	(16 in)
The assembled unit weighs	20 kg	(44 lb)

The module widths, from left to right, are as follows:

V.C.O. Module (63)	76.2 mm	(3 in)
Frequency Translator Module (64) :	76.2 mm	(3 in)
2nd I.F. Loop Module (51)	25.4 mm	(1 in)
Pulse Swallower Module (52)	25.4 mm	(1 in)

Phase Comparator (53)	25.4 mm	(1 in)
Auto Attenuator Module (55)	44.45 mm	(1.3/4 in)
S.S.B. Generator Module (54)	44.45 mm	(1.3/4 in)
Blank	28.57 mm	(1.1/8 in)
Power Supply Module (30)	117.48 mm	(4.5/8 in)

- End of Part -

PART 2

PRINCIPLES OF OPERATION

Refer to Functional Schematic, Figure 2-1.

1. GENERAL

The incoming audio signal is applied to the S.S.B. Generator Module via an audio amplifier in the Auto Attenuator Module. The S.S.B. Generator Module is fed with a 250 kHz signal derived from the 1 MHz reference by division by 4 in the 2nd I.F. Loop Module. The S.S.B. Generator Module produces a modulated 250 kHz signal in the emission mode selected. The modulated 250 kHz signal is applied to the Frequency Translator Module via the Auto Attenuator Module which compares the transmitter output level with a local reference level and controls the attenuation of the signal to maintain the overall system gain as set.

In the Frequency Translator Module, the modulated 250 kHz signal is raised to the required frequency by progressive mixing with the outputs of voltage controlled, variable frequency oscillators (V.C.O's) and the output of one fixed oscillator.

Each V.C.O. is part of a phase locked loop in which the oscillator output is frequency divided and compared with the 1 MHz frequency standard in a phase comparator. A d.c. error signal is derived to control the oscillator frequency. In the first (low frequency) phase locked loop, the division ratio is determined by the kHz and Hz x 100 digits of the selected frequency. The output frequency of this loop will determine the kHz and Hz x 100 digits of the output frequency.

In the second (high frequency) phase locked loop, the division ratio is determined by the MHz x 10, MHz, kHz x 100 and kHz x 10 digits of the selected frequency. The output frequency of this loop will determine the MHz x 10, MHz, kHz x 100 and kHz x 10 digits of the output frequency.

In the third (control) phase locked loop, the division ratio is fixed at 10.7 and the resulting oscillator frequency of 10.7 MHz is the input to the control path in the V.C.O. Module.

NOTE: To facilitate the remainder of the description, reference is made to an example channel frequency setting (21.4963 MHz) which corresponds with the figures in parentheses on Functional Schematic, Fig. 2-1.

2. SYNTHESIS OF SELECTED FREQUENCY

2.1 General

The exciter has essentially two paths - the r.f. signal path and the control path. The r.f. signal path is shown in straight-through configuration at the top of Figure 1; the control path is located in the lower part of the diagram.

2.2 Signal Path

In the Frequency Translator Module, the modulated 250 kHz signal is applied to the 2nd I.F. Mixer Board where it is up-mixed with the output of the 10.45 MHz V.C.O. Board which forms part of the low frequency phase locked loop. The output frequency of the 10.45 MHz V.C.O. Board will be 10.45 MHz less the value of the kHz and Hz x 100 digits of the selected channel frequency (for the example setting (21.4963) this will be: 10.45 MHz - 6.3 kHz = 10.4437 MHz). Note that the maximum value of kHz and Hz x 100 subtracted will be 9.9 kHz where the last two digits of the selected channel frequency are 99.

The output of the 2nd I.F. Mixer Board will be 10.7 MHz less the value of the kHz and Hz x 100 digits of the selected channel frequency (for the example setting this will be 10.7 MHz - 6.3 kHz = 10.6937 MHz).

After amplification and filtering of spurious components on the 2nd I.F. Amplifier Board, the nominal 10.7 MHz signal is applied to the Signal Up-Mixer Board where it is up-mixed with a fixed frequency of 123.1 MHz generated on the Control Up-Mixer Board in the V.C.O. Module by doubling the output of a 61.55 MHz crystal oscillator.

The result of the mixing process is a frequency of 133.8 MHz less the value of the kHz and Hz x 100 digits of the selected channel frequency (for the example this will be: 133.8 MHz - 6.3 kHz = 133.7937 MHz).

After filtering of spurious components by means of tuned amplifiers, the signal is passed to the Signal Down-Mixer Board, where after further filtering, it is down-mixed with the output of the Main V.C.O. Board in the V.C.O. Module. The Main V.C.O. is part of the high frequency phase locked loop and its output frequency is determined indirectly by the MHz x 10, MHz, kHz x 100 and kHz x 10 digits of the selected channel frequency. The frequency will be the value of these four digits plus 133.8 MHz and will be in the range 135.40 MHz to 163.79 MHz (for the example this will be 21.49 MHz + 133.8 MHz = 155.2900 MHz). The result of the down-mixing process will be an output frequency in the range 1.6000 MHz to 29.9999 MHz which is the required frequency range for the Exciter. The example channel frequency setting is made up as follows:

	155.2900 MHz	(Main V.C.O. output)
-	133.7937 MHz	(Output from Signal Up-Mixer Board)
=	21.4963 MHz	(Example channel frequency setting)

Note how the frequency difference due to the value of the kHz and Hz x 100 digits of the setting is maintained and determines the value of the corresponding digits of the output frequency: the Main V.C.O. output frequency will always have zeros in these positions. This output frequency is fed to the linear amplifier section of the transmitter by the Wide-band Amplifier Board.

To summarise, the 250 kHz modulated signal from the S.S.B. Generator Module is converted to the required operating frequency in three successive mixing operations:

1. Up-mixed with a frequency of 10.4500 MHz less the value of the kHz and Hz x 100 digits of the selected channel frequency.

2. The result of 1, up-mixed with a fixed frequency of 123.1 MHz.

3. The result of 2, down-mixed with a frequency in the range 135.40 MHz to 163.79 MHz as determined by the value of the MHz x 10, MHz, kHz x 100 and kHz x 10 digits of the selected channel frequency.

For the example channel frequency setting, the process will be as follows:

	250 kHz	(S.S.B. Generator output)
+	10.4937 MHz	(10.45 MHz - 6.3 kHz)
=	10.6937 MHz	(10.7 MHz - 6.3 kHz)
+	123.1000 MHz	
=	133.7937 MHz	(133.8 MHz - 6.3 kHz)
subtracted from	155.2900 MHz	(133.8 MHz + 21.49 MHz)
=	21.4963 MHz	(the selected channel frequency)

2.3 Control Path

While the 250 kHz modulated signal is being converted to the selected channel frequency as described above, the control path of the exciter is synthesising frequencies which correspond with those in the signal path.

The control path synthesis begins with the 10.7 MHz V.C.O. Board which forms part of a phase locked loop similar to that associated with the 10.45 MHz V.C.O. Board. The output of the board is 10.7 MHz with no effect from modulation or from the digits of the selected channel frequency. This 10.7 MHz output is fed to the Control Up-Mixer Board where the action of the Signal Up-Mixer Board is duplicated in up-mixing the 10.7 MHz with the fixed 123.1 MHz to produce 133.8 MHz. Similarly, the action of the Signal Down-Mixer is duplicated on the Control Down-Mixer Board where the 133.8 MHz from the Control Up-Mixer is down-mixed with the output of the Main V.C.O. Board (135.40 MHz to 163.79 MHz) via the V.C.O. Splitter Board. The output of the Control Down-Mixer Board is a frequency in the range 1.6000 MHz to 29.9900 MHz as determined by the frequency of the Main V.C.O. and is fed to the programmable divider in the Pulse Swallower Module.

Thus the output frequency of the exciter has been synthesised independently of the signal path, the only difference being the absence of modulation and the effect of the kHz and Hz x 100 digits of the selected channel frequency.

NOTE: The 61.55 MHz oscillator on the Control Up-Mixer Board (which provides via a doubler the 123.1 MHz fixed mixing frequency used on both the Control and Signal Up-Mixers) is, although crystal controlled, not locked to the 1 MHz reference. Small changes in the frequency of this oscillator are, however, of no consequence; any change which occurs will appear at both inputs to the Signal

Down-Mixer, both via the Signal Up-Mixer, and via the Control Up-Mixer and high frequency phase locked loop. The error will be substracted from itself in the down mixing process and the output frequency is unaffected.

2.4 Phase Locked Loops

The exciter employs three phase locked loops; each loop comprises a voltage controlled, variable frequency oscillator, a frequency divider, and a system of phase comparison which provides an error correction voltage for the oscillator. The division ratio of the frequency divider is programmed by the digits of the selected channel frequency to a value which provides, with the loop locked, a divider output frequency equal to the comparison standard frequency. In this way it is possible to perform the comparison at the same frequency over the range of the oscillator frequency.

The three phase locked loops employed are:

(i) The low frequency phase locked loop controlling the frequency of the 10.45 MHz V.C.O. as determined by the value of the kHz and Hz x 100 digits of the selected channel frequency.

(ii) The high frequency phase locked loop controlling the frequency of the Main V.C.O. as determined by the value of the MHz x 10, MHz, kHz x 100 and kHz x 10 digits of the selected channel frequency.

(iii) The control phase locked loop in which the frequency of the 10.7 MHz V.C.O. is held at 10.7 MHz; the division ratio is fixed and no reference is made to the selected channel frequency.

The low frequency phase locked loop comprises the 10.45 MHz V.C.O. Board along with division and comparator circuitry contained in the 2nd I.F. Loop Module. The 10.45 MHz V.C.O. is controlled over the range 10.4401 MHz to 10.4500 MHz in 100 Hz increments. This range represents 10.4500 MHz less the range of values for the kHz and Hz x 100 digits of the selected channel frequency (0.0 to 9.9 kHz). The 1 MHz reference is used as the comparison frequency in the phase comparator and the division ratio of the frequency divider is programmable over the range 10.4401 to 10.4500 and provides 1 MHz at the divider output over the entire frequency range of the oscillator. For the example channel frequency setting, the value of the kHz and Hz x 100 digits is 6.3 kHz which sets the division ratio to 10.4437 and the oscillator frequency is controlled at 10.4437 MHz.

The high frequency phase locked loop comprises the Main V.C.O. Board, the V.C.O. Control Board, the V.C.O. Splitter Board, and the Control Down-Mixer in the V.C.O. Module, the Phase Comparator Module and Pulse Swallower Module. This loop differs from the low frequency loop in that the frequency applied to the frequency divider is lower by 133.8 MHz than the frequency of the Main V.C.O. due to the action of the Control Down-Mixer. The frequency at the divider input is, in fact, equal to the output frequency of the exciter. The frequency divider is enabled to operate at a lower frequency, simplifying

logic design, and there is a direct relationship between the division ratio and the values of the MHz x 10, MHz, kHz x 100 and kHz x 10 digits of the selected frequency. The 1 MHz reference is again used as the comparison frequency in the phase comparator and the division ratio of the frequency divider in the Pulse Swallower Module is programmable over the range 1.60 to 29.99 and provides 1 MHz at the divider output for a divider input frequency range of 1.6 MHz to 29.99 MHz. The Main V.C.O. is controlled over the range 135.40 MHz to 163.79 MHz in 10 kHz increments: this represents a frequency equal to the value of the MHz x 10, MHz, kHz x 100 and kHz x 10 digits of the selected channel frequency, plus 133.8 MHz. For the example channel frequency setting, the value of the MHz x 10, MHz, kHz x 100 and kHz x 10 digits is 21.49 MHz which sets the division ratio to 21.49 and the oscillator frequency is controlled at 21.49 MHz + 133.8 MHz = 155.2900 MHz.

The control phase locked loop comprises the 10.7 MHz V.C.O. Board along with division and comparator circuits contained in the 2nd I.F. Loop Module. The division rate is fixed at 10.7 and the divider output is 1 MHz. The V.C.O. output is held at 10.7 MHz and provides a phase locked fixed frequency source for the control path synthesis.

- End of Part -

PART 3

CIRCUIT DESCRIPTION

NOTE: Reference in the text to integrated circuit pin numbers is made using the circuit reference number followed by the pin number in brackets. Where it is necessary to identify an individual logic element within an integrated circuit, a lower case alphabetical suffix is used following the circuit reference number.

1. V.C.O. MODULE 1J66463

Refer to interwiring diagram Fig. 2-3 and to Circuit Diagrams as indicated.

1.1 General

The V.C.O. Module contains five printed circuit boards, each contained in a screened box. Interwiring of the five boards is shown in Figure 2-3. The five printed circuit boards are as follows:

(a) Main V.C.O. Board 2R66435 (Part of V.H.F. Oscillator 1R66456)

(b) V.C.O. Control Board 1R66436

(c) V.C.O. Splitter Board 1R66437

(d) Control Up-Mixer Board 1R66445

(e) Control Down-Mixer Board 1R66446

(f) 10.7 MHz Low Pass Filter Board 1R66467

The front panel of the module is equipped with three coaxial connectors as follows:

(i) 123 MHz - 123.1 MHz output to the Frequency Translator Module. Connected internally to the Control Up-Mixer Board.

(ii) 10.7 MHz - Receives 10.7 MHz signal from the Frequency Translator Module.

Connected internally to the Control Up-Mixer Board.

(iii) V.C.O. - Output from the high frequency phase locked loop to the Frequency Translator Module.

Connected internally to the V.C.O. Splitter Board.

1.2 Main V.C.O. Board 2R66435 (Part of V.H.F. Oscillator 1R66456)

Refer to circuit diagram Fig. 2-5.

The Main V.C.O. Board is the voltage controlled oscillator for the high frequency phase locked loop which controls the oscillator over the range

135.40 MHz to 163.79 MHz. The oscillator output provides input to the V.C.O. Splitter Board which in turn feeds the Signal Down-Mixer Board and the Control Down-Mixer Board.

Colpitts oscillator VT1 is controlled over the operating range by a controlling voltage applied across varactor C9. The control voltage comprises three components: a fixed (adjustable) d.c. bias, and the coarse and fine control voltage output of the Phase Comparator Module via the V.C.O. Control Board. The components are applied at opposite ends of C9. The oscillator output at VT1 emitter is fed via C8 to amplifier VT2 which has a transformer coupled output to the V.C.O. Splitter Board. The output level is adjusted using RV1.

The differential voltage on board pins 1, 2 (VHF oscillator pins 1, 4) is approximately 4V for an oscillation frequency of 135 MHz and 24 V for 169 MHz; pin 1 is negative.

Supply voltage for the circuit is a regulated +15 V supplied by regulator MN1 from a +24 V source via filter 34R1 and 34C11.

1.3 V.C.O. Control Board 1R66436

Refer to circuit diagram Fig. 2-6.

The V.C.O. Control Board provides gain/frequency compensation for the V.H.F. phase locked loop error voltages derived from the Phase Comparator Module 1J66453 and used to control the frequency of the Main V.C.O. 2R66435.

The coarse comparator (D/A) output is applied to variable gain d.c. amplifier MN3 via low frequency limit network RV1, R11, R12. The output voltage range is from -10 V, corresponding to 0V input and biased via R13, R19, C9 to +10 V corresponding to an input of +15 V. The gain shaping is controlled by the induction levels of diodes MR2, MR3 and MR4, which change with the output voltage and hence change the negative feedback and gain of the amplifier. For exciter frequencies greater than approximately 20 MHz, (Main V.C.O. frequencies greater than 154 MHz) the amplifier output is negative and the gain is fixed, but for exciter frequencies less than 20 MHz, (Main V.C.O. frequencies less than 154 MHz) the amplifier output is positive and the gain decreases. The minimum gain is approximately six times less than the maximum and occurs for the lowest output frequency (the most positive D/A output).

The fine comparator error voltage from the phase comparator circuit is applied to Four Quadrant Multiplier MN4 and amplified by a factor 4Vx/10. Voltage Vx is derived from the coarse output voltage via R21 - R24 and varies from approximately -8 V at the higher output frequencies to approximately -1.5 V at the lower output frequencies of the exciter; a variation of 5 to 1 over the frequency range and always involving a phase inversion of the error signal. The input offset for the control voltage Vx is corrected by RV2 to give an amplification factor of approximately 0 with 0 V on board pin 11.

Voltage regulators MN1, MN2 provide -15 V and +15 V from -24 V and +24 V unregulated supplies, to operate MN3, MN4 and also for the control

amplifiers on the 10.45 MHz V.C.O. Board 1R66442 and the 10.7 MHz V.C.O. Board 1R66438.

1.4 V.C.O. Splitter Board 1R66437

Refer to circuit diagram Fig. 2-7.

The V.C.O. Splitter Board receives output from the main V.C.O. board and provides two outputs: one to the Signal Down-Mixer Board and one to the Control Down-Mixer Board. The output from the main V.C.O. board is applied to the base of tuned amplifier VT1 and an output is taken from the collector of VT1 to the Signal Down-Mixer board via trimmer C7 which provides output circuit tuning. Also from the collector of VT1 an output is taken via trimmer C8 to a two stage FET isolation amplifier which is included to prevent digital logic noise from being coupled back from the Pulse Swallower Module divider via the Control Down-Mixer and finding its way to the signal path via the Signal Down-Mixer output. This isolation is ensured by the low feedback capacitance of the FETs.

1.5 Control Up-Mixer Board 1R66445

Refer to circuit diagram, Fig. 2-8.

The Control Up-Mixer Board up-mixes the output of the 10.7 MHz V.C.O. board in the Frequency Translator Module, with a 123.1 MHz signal produced by a 61.55 MHz crystal oscillator and doubler circuit.

Quad mixer diode assembly MR2 is connected as a balanced modulator. The 10.7 MHz signal is applied to the modulator via TR1 which is tuned to 10.7 MHz. The 123.1 MHz signal is applied to the modulator at the junction of C22 and C23. The 123.1 MHz component is reduced by virtue of the balanced mixer and the frequency components appearing at the output of the modulator. The output of the modulator is taken from C26/C27 via a 133.8 MHz bandpass filter TR2, C28, C29 and C31 (ensuring rejection of the unwanted components) to a tuned amplifier stage VT6 which provides signal output to the Control Down-Mixer Board. The 123.1 MHz signal is produced by 61.55 MHz crystal controlled Colpitts oscillator VT1 followed by tuned doubler stage VT2A. A 123.1 MHz output to the Signal Up-Mixer Board on the Frequency Translator Module is taken from VT2 Collector circuit. The 123.1 MHz signal is applied to the balanced modulator by amplifier VT3 and cascode pair VT4 and VT5.

1.6 Control Down-Mixer Board 1R66446

Refer to circuit diagram, Fig. 2-9.

The Control Down-Mixer Board down-mixes the output of the Control Up-Mixer Board (133.8 MHz) with the output of the high frequency phase locked loop via the V.C.O. Splitter Board (a frequency in the range 135.4 MHz to 163.79 MHz). The output frequency of the board is in the range 1.6 MHz to 29.99 MHz which is fed to the Pulse Swallower Module.

Quad diode mixer assembly MR2 is connected as a balanced modulator. The output of the Control Up-Mixer Board is applied to the modulator via a

133.8 MHz bandpass filter TR1, C11, C14 and C9 to ensure rejection of unwanted frequency components. Output from the V.C.O. Splitter Board is applied to the modulator via amplifier VT1 and cascode pair VT2 and VT3. The 135.4 MHz to 163.79 MHz component is reduced in the mixing process and the frequency components appearing at the modulator output are the sum (in the range 269.2000 MHz to 297.5900 MHz) and the difference (in the range 1.6000 MHz to 29.9900 MHz). The output of the modulator is applied to a two-stage wide-band amplifier comprising grounded base stage VT4 followed by grounded emitter stage VT5 which provides transformer coupled output to the Pulse Swallower Module. The sum frequency is virtually eliminated by the band-pass nature of the wide-band amplifier.

1.7 10.7 MHz Low Pass Filter Board 1R66467

Refer to circuit diagram, Fig. 2-9A.

The Low Pass Filter board is placed in the 10.7 MHz line to the Control Up-Mixer Board. The function is to minimise any harmonics of 10.7 MHz and any feedback of 123.1 MHz or 133.8 MHz on the cable. The circuit is passive and comprises a pi section L-C filter.

2. FREQUENCY TRANSLATOR MODULE 1J66464

Refer to interwiring diagram, Fig. 2-10 and to circuit diagram as indicated.

2.1 General

The Frequency Translator Module contains eight printed circuit boards, each contained in a screened box; interwiring between them is shown in Fig. 2-10. The eight printed circuit boards are as follows:

(a) 10.7 MHz V.C.O. Board Type 1R66438
(b) 10.45 MHz V.C.O. Board Type 1R66442
(c) 2nd I.F. Mixer Board Type 1R66443
(d) 2nd I.F. Amplifier Board 1R66444
(e) Signal Up-Mixer Board Type 1R66448
(f) Signal Down-Mixer Board Type 1R66449
(g) Wide-Band Amplifier Board 2R66450
(h) 123 MHz Filter Board Type 1R66466

The front panel of the Module is equipped with four coaxial connectors as follows:

(i) 123 MHz - Receives 123.1 MHz signal from the V.C.O. Module. Connected internally to the Signal Up-Mixer Board via the 123 MHz Filter Board.

(ii) 10.7 MHz - Provides 10.7 MHz output from the 10.7 MHz V.C.O. Board for connection to the V.C.O. Module.

(iii) V.C.O. - Receives the output of the Main V.C.O. Board in the V.C.O. Module. Connected internally to the Signal Down-Mixer Board.

(iv) R.F. OUT - The r.f. output from the exciter via the Wide-Band Amplifier Board.

2.2 10.7 MHz V.C.O. Board 1R66438

Refer to circuit diagram, Fig. 2-11.

The 10.7 MHz V.C.O. Board is the voltage controlled oscillator for the control phase locked loop which maintains the oscillator frequency at 10.7 MHz. The oscillator output provides the base frequency for the control path synthesis and duplicates the output of the 2nd I.F. Amplifier Board in the signal path.

A 10.7 MHz crystal controlled Colpitts oscillator is held at 10.7 MHz by a correction voltage applied to varactor C20 in the crystal circuit. The correction voltage is supplied by the phase comparator on the 2nd I.F. Loop Module and is applied to C20 via a differential amplifier MN1. The oscillator transistor VT1 feeds a grounded base isolation stage which provides signal output to the Control Up-Mixer via C18, and, via C14, drives grounded base amplifier VT4 which in turn provides signal output to the divider on the 2nd I.F. Loop Module via C17. The isolation stage also drives a.g.c. amplifier VT3 via C10. The a.g.c. amplifier provides a negative feedback to the base of the oscillator transistor VT1, giving a high degree of stability to the oscillator.

2.3 10.45 MHz V.C.O. Board 1R66442

Refer to circuit diagram, Fig. 2-12.

The 10.45 MHz V.C.O. Board is the voltage controlled oscillator for the low frequency phase locked loop which controls the oscillator over the range 10.4401 MHz to 10.4500 MHz. The oscillator output provides input to the 2nd I.F. Mixer Board for mixing with the modulated 250 kHz signal from the S.S.B. Generator Module.

Crystal controlled Butler oscillator VT1 and VT2 is pulled over the operating frequency range by a controlling voltage applied to two varactors C21 and C22 in the crystal circuit. The controlling voltage is supplied by the phase comparator on the 2nd I.F. Loop Module and is applied to the varactors via differential amplifier MN1. The output from the oscillator at VT2 collector is applied to F.E.T. isolation stage VT3 which, because of its low feedback capacitance, provides excellent isolation from output circuit loading. Amplifier VT3 provides a signal output to the 2nd I.F. Mixer Board via C14 and via C16 drives grounded base amplifier VT4 which provides signal output to the divider on the 2nd I.F. Loop Module via C18.

2.4 2nd I.F. Mixer Board 1R66443

Refer to circuit diagram, Fig. 2-13.

The 2nd I.F. Mixer Board up-mixes the 250 kHz modulated signal from the S.S.B. Generator Module via the Auto Attenuator Module, with the output of the 10.45 MHz V.C.O. Board (in the range 10.4401 MHz to 10.4500 MHz) to provide an output frequency in the range 10.6901 MHz to 10.7000 MHz.

Quad diode mixer assembly MR1 is connected as a balanced modulator. The modulated 250 kHz signal is applied to the modulator via TR1. Output from the 10.45 MHz V.C.O. Board is applied to amplifier VT1 which drives the modulator at the centre-tap of TR2. The 10.45 MHz component is largely cancelled in the mixing process and the frequency components appearing at the secondary of TR2 are mostly the sum (in the range 10.6901 MHz to 10.7000 MHz) and the difference (in the range 10.1901 MHz to 10.2000 MHz). Output bandpass filter C12, L3 and C13 is tuned to 10.7 MHz and provides a degree of attenuation for the difference component as well as any 10.45 MHz residual.

2.5 2nd I.F. Amplifier Board 1R66444

Refer to circuit diagram, Fig. 2-14.

The 2nd I.F. Amplifier Board follows the 2nd I.F. Mixer Board and provides amplification and filtering.

Input from the 2nd I.F. Mixer Board at 10.7 MHz is applied to the base of tuned amplifier VT1 via C1. Trap filter C8 and L4 is tuned to 10.45 MHz to ensure the elimination of the 10.45 residual from the 2nd I.F. Mixer Board. Output from VT1 collector is applied to a 10.7 MHz crystal filter which has a bandwidth of 30 kHz and ensures rejection of all unwanted frequency components. The unbalanced output of the crystal filter is balanced by L3 to satisfy the input requirements of the following Signal Up-Mixer Board.

2.6 Signal Up-Mixer Board 1R66448

Refer to circuit diagram, Fig. 2-15.

The Signal Up-Mixer Board up-mixes the output of the 2nd I.F. Mixer Board via the 2nd I.F. Amplifier Board, with the 123.1 MHz signal from the Control Up-Mixer Board in the V.C.O. Module. The output frequency of the board is in the range 133.7901 MHz to 133.8000 MHz.

Quad diode mixer assembly MR2 is connected as a balanced modulator. The 10.7 MHz signal from the 2nd I.F. Amplifier is applied directly to the modulator across C9 and C11. The 123.1 MHz signal is applied to the modulator via amplifier VT1 and cascode pair VT2 and VT3. The 123.1 MHz component is reduced by virtue of mixer balance and the frequency components appearing across C12 and C13 are mostly the residual 123.1 MHz, the sum (in the range 133.7901 MHz to 133.8000 MHz) and the difference (in the range 112.4000 MHz to 112.4099 MHz). Following the modulator there are two successive bandpass filters C14, TR1, C16 and C17, and C21, C22, TR2, C23 and C24 the former preceding and the latter following the tuned output amplifier VT4. Both filters are tuned to 133.8 MHz and together provide considerable rejection for the difference component as well as for 123.1 MHz residual.

2.7 Signal Down-Mixer Board 1R66449

Refer to circuit diagram, Fig. 2-16.

The Signal Down-Mixer Board down-mixes the output of the Signal Up-Mixer Board (in the range 133.7901 MHz to 133.8000 MHz), with the output of

the high frequency phase locked loop via the V.C.O. Splitter Board in the V.C.O. Module (a frequency in the range 135.40 MHz to 163.79 MHz). The output frequency of the board is in the range 1.6000 MHz to 29.9999 MHz which is the required output range for the exciter.

Quad diode mixer assembly MR2 is connected as a balanced modulator. The output of the Signal Up-Mixer Board is applied to amplifier VT4 via a bandpass filter L4, C24 and C23 tuned to 133.8 MHz and a notch filter L3 and C22 tuned to 123.1 MHz. The filters together ensure rejection of unwanted frequency products of the mixing process on the Signal Up-Mixer Board. Output from VT4 collector feeds the balanced modulator via a further 133.8 MHz bandpass filter C16, C17, TR1 and C14. Output from the high frequency phase locked loop is applied to the modulator via amplifier VT1 and cascode pair VT2 and VT3. The high frequency phase locked loop component is reduced by virtue of balanced mixing and the frequency components appearing at the modulator output are the above residual, the sum (in the range 269.1901 MHz to 297.5900 MHz) and the difference (in the range 1.6000 MHz to 29.9999 MHz). The output from the modulator is fed out to the following Wide-Band Amplifier Board via a low-pass filter L6, C26, L7 and C27 which has a cut-off frequency of just beyond 30 MHz and ensures rejection of the sum components and the residual components of the high frequency phase locked loop output.

2.8 Wide-Band Amplifier Board 2R66450

Refer to circuit diagram, Fig. 2-17.

The Wide-Band Amplifier Board is the output amplifier for the exciter unit: it amplifies the output of the Signal Down-Mixer and provides the required output level.

The circuit comprises a grounded emitter stage VT1, transformer coupled by TR1 to a grounded emitter state VT2. Bias filtering is provided for low noise operation. The output circuit is transformer coupled for impedance matching, (50 ohms) and is connected to front panel coaxial connector R.F. OUT.

2.9 123 MHz Filter Board 1R66466

Refer to circuit diagram, Fig. 2-18.

The 123 MHz Filter Board is placed in the 123.1 MHz input line to the Signal Up-Mixer Board. The function of the filter is to provide rejection of any 133.8 MHz component from the Control Up-Mixer Board. The circuit is passive and comprises a 2-section band-pass filter, tuned to 123 MHz.

3. 2nd I.F. LOOP MODULE 1J66451

Refer to circuit diagram, Fig. 2-19.

3.1 General

The 2nd I.F. Loop Module provides the programmable frequency divider for low frequency phase locked loop, the fixed frequency divider for the control phase locked loop, and frequency phase comparison circuits for both phase

locked loops. The programmable divider provides division ratios in the range 10.4401 to 10.4500 as determined by the kHz and Hz x 100 digits of the selected channel frequency. The fixed frequency divider provides a division ratio of 10.7.

3.2 Principles of Operation

3.2.1 Programmable Divider

A divide-by-ten circuit is made to divide by eleven for 45% of the time to provide a base division ratio of 10.4500. Under control of the kHz and Hz x 100 digits of the selected channel frequency the percentage of divides by eleven is reduced by a maximum of 0.99%, and hence the average division ratio is reduced to a minimum of 10.4401.

The 0.99% reduction is made up as follows:

(i) 0 - 0.9% as determined by the kHz digit, plus
(ii) 0 - 0.09% as determined by the Hz x 100 digit.

For the example channel frequency setting, the value of the kHz and Hz x 100 digits is 6.3 kHz. The base division ratio of 10.4500 will be reduced to 10.4437 by reducing the number of divides by eleven by 0.63% as follows:

(i) 0.6% as determined by the kHz digit (6), plus
(ii) 0.03% as determined by the Hz x 100 digit (3).

3.2.2 Fixed Divider

A divide-by-ten circuit is made to divide by eleven for 70% of the time to provide a division ratio of 10.7.

3.2.3 Frequency Phase Comparators

For the low frequency phase locked loop, the divided output is extracted from the programmable divider logic at a frequency of 100 kHz. The 1 MHz reference is divided by ten and the two 100 kHz signals applied to a phase comparator circuit. Both signals are again divided by ten and control the states of a bistable circuit. The mark-to-space ratio of the bistable output indicates the phase difference. For the control phase locked loop, the circuitry is identical except that the input frequencies are 1 MHz.

3.3 Circuit Description

3.3.1 Programmable Divider

The sinusoidal input signal from the 10.45 MHz V.C.O. Board is amplified by long-tailed pair VT4 and VT5 and squared by clipping amplifier VT6/MR2. The resulting square-wave is applied to the clock input of pre-settable binary counter MN3. The logic controlling MN3 is arranged so that at a count of 1 1 0 0, MN4 a(3)/MN4 b(6) goes to 0 and causes the data inputs to be loaded to the counter. The loaded value will be 0 0 1 1 if MN5 b(8)/MN4 c(8) is 1, or 0 0 1 0 if MN5 b(8)/MN4 c(8) is 0. The number of input pulses required to advance MN3 from the loaded values of 0 0 1 1 and 0 0 1 0 to 1 1 0 0 is 10 and 11 respectively. Thus MN3 behaves as a divide-by-ten while MN5

b(8)/MN4 c(8) is 1 and as a divide-by-eleven while MN5 b(8)/MN4 c(8) is 0.

The level at MN5 b(8)/MN4 c(8) is determined, in part, by the state of the B output of divide-by-ten circuit MN6. The input to MN6 is to the B input, the D output is connected to the A input and the stage output is taken from the A output. The stage behaves as a divide-by-ten with the A as the high order bit. During the count sequence the B output is 1 for 40% of the time and hence MN4 c(8) is 0 for 40% of the time. The division ratio of MN3 will therefore be ten for 60% and eleven for 40% of the time providing an average division ratio of 10.4. The output of MN6 is fed to decade counter MN7, which is advanced through a normal BCD count. The average division ratio is further increased by the action of MN5 b(8) which is 0 when MN6A, MN6D, MN7A and MN5 a(6) are all 1. The two states MN6A and MN6D at 1 together define one in ten division cycles of MN3; MN7A, being half the frequency of MN6A, narrows the definition to one in twenty division cycles of MN3. Thus the number of divides by eleven in MN3 is increased by a further 5% to provide an average division ratio of 10.45 which is the required base mentioned above.

The base division ratio of 10.4500 is then reduced under control of the kHz and Hz 100 digits of the selected channel frequency. NAND gate MN5 examines the "carries" out of a binary adder array during every 1 state of MN7D which defines one in 100 division cycles of MN3. Gate MN5a may detect as many as 99 carries for every 100 MN7D pulses (this represents 99 in 10,000 division cycles of MN3 or 0.99%). Each carry causes MN5a(6) to go to 0 and prevent MN5b(8) going to 0; this prevents MN5b(8) from causing a divide by eleven and effectively reduces the average division ratio.

The binary adder array comprises two adder circuits: decade counter MN8 with binary full-adder MN23, and decade counter MN9 with binary full-adder MN10. Decade counters MN8 and MN9 are connected in cascade with MN7D advancing MN8, and MN8A advancing MN9. Hence MN9 advances at one tenth the rate of MN8. The decade counter outputs are applied to the "B" inputs of the appropriate binary adders: MN8 outputs to MN23 and MN9 outputs to MN10. Appearing on the "A" inputs of the adders are control inputs representing the kHz and Hz x 100 digits of the selected channel frequency: the kHz digit is applied to MN23 and the Hz x 100 digit is applied to MN10. The code of the control inputs is an "excess six" code which represents, in binary, the selected digit plus six: the code is shown in Table 2-1.

Selected Digit	Control Inputs 8	4	2	1
0	0	1	1	0
1	0	1	1	1
2	1	0	0	0
3	1	0	0	1
4	1	0	1	0
5	1	0	1	1
6	1	1	0	0
7	1	1	0	1
8	1	1	1	0
9	1	1	1	1

TABLE 2-1

"EXCESS SIX" CODE of kHz and Hz x 100 DIGIT

CONTROL INPUTS

The two decade counters are connected with B as the low-order stage and A as the high order stage. The four stage outputs of the decade counters are considered on the adder inputs in the normal order of A B C D and the resulting count sequence is as shown in Table 2-2. The control input code and the count sequence of the decade counters are chosen to provide the required pattern of carries out of the adder array.

The adders continuously provide at their outputs the sum and carry (if present) of the control input states and the count in MN8 or MN9. Only the carry is considered by the logic. The behaviour of the adder circuits for selected digits of 0, 1, 3, 6 and 9 is summarised in Table 2-2 which applies to both adder circuits. Table 2-2 shows that the number of carries which emerge from the adder during the count sequence of the decade counter corresponds to the value of the selected digit if the input carry (Co) is 0. If there is an input carry to the adder (Co = 1) then the number of carries is one greater than the value of the selected digit. The carry out (C4) of MN10 is applied to the carry input (Co) of MN23 and if there is a carry out of MN10 it will propagate through MN23 to increase the number of carries from MN23 by one for a maximum of

nine MN8 count sequences in ten. To prevent MN10 carries from appearing simultaneously with those from MN23, the arrangement of MN8/MN9 count sequences provides separation of the carries into two groups so that the carry from MN10 always propagates through MN23 where there is no carry due to the add in MN23.

For the example channel frequency setting the selected digits are 6.3 kHz. Three carries emerge from MN10 during the count sequence of MN9 and increase the normal six carries from MN23 to seven for three out of ten count sequences of MN8. Thus a total of 63 carries emerge from MN23 for every 100 pulses from MN7D and there are 63 less divides by eleven for every 10,000 division cycles of MN3 (0.63%). The average division ratio is therefore reduced to:
10.4500 - 0.63% = 10.4437.

3.3.2 Fixed Divider

The sinusoidal input signal from the 10.7 MHz V.C.O. Board is amplified by long-tailed pair VT1 and VT2, and squared by clipping amplifier VT3/MR1. The resulting square wave is applied to the clock input of presettable binary counter MN14. Gate MN17b goes to 0 when the count in MN14 reaches 1 1 0 0 and causes the data inputs to be loaded to the counter. The loaded value will be 0 0 1 1 if MN15a (13) is 1 or 0 0 1 0 if it is 0; the number of input pulses required to advance MN14 from the loaded values of 0 0 1 0 and 0 0 1 1 to 1 1 0 0 is ten and eleven, respectively. Thus MN14 behaves as divider-by-ten while MN15a (13) is 1 and as a divide-by-eleven while MN15a (13) is 0. Flip-flop MN15aforms part of a four-stage counter circuit which is advanced by the divided out-put of MN14. The states of the counter follow the count sequence shown in Table 2-3.

The state at MN15a (13) is the inverse of that at MN15a (12) and will be at 0 for seven of the ten states of the counter. Hence, MN14 will divide by eleven for 70% of the time to provide an average division ratio of 10.7.

3.3.3 Frequency/Phase Comparators

The frequency/phase comparator circuits for the low frequency phase locked loop are identical and only the former is considered in detail.

From the programmable divider, an output is taken from MN6A where the frequency is nominally 100 kHz being one tenth the frequency at MN3D. This 100 kHz output is applied to the A input of decade counter MN18. The 1 MHz reference signal is divided by ten in decade counter MN1 and the resultant 100 kHz signal applied to the A input of decade counter MN19. The decade counters MN18 and MN19 are advanced by their inputs through normal BCD count sequences. The AND gates MN11d and MN11a produce a 1 output pulse during the count of 9 (1 0 0 1). Pulse shaping networks MN12a/MN13b/C36 and MN12f/MN13a/C37 each produce a short positive pulse whose duration is determined by the delay of MN12a or MN12f and the integrating effect of C36 or C37. This pulse appears after the trailing edge of the MN11d or MN11a pulse. The two NOR gates MN13c and MN13d are connected as a bistable

TABLE 2-2 CARRIES OUT OF ADDERS MN10 AND MN23

MN8/MN9 COUNT D	C	B	A	CONTROL INPUTS 8	4	2	1		CARRIES OUT (C_4) with $C_o = 0$	with $C_o = 1$
MN10 MN23 B_4	B_3	B_2	B_1	A_4	A_3	A_2	A_1			
0	0	0	0	0	1	1	0	)	0	0
0	0	1	0	0	1	1	0	)	0	0
0	1	0	0	0	1	1	0	)	0	0
0	1	1	0	0	1	1	0	)	0	0
1	0	0	0	0	1	1	0	)	0	0
0	0	0	1	0	1	1	0	) (0)	0	0
0	0	1	1	0	1	1	0	)	0	0
0	1	0	1	0	1	1	0	)	0	0
0	1	1	1	0	1	1	0	)	0	0
1	0	0	1	0	1	1	0	)	0	1
0	0	0	0	0	1	1	1	)	0	0
0	0	1	0	0	1	1	1	)	0	0
0	1	0	0	0	1	1	1	)	0	0
0	1	1	0	0	1	1	1	)	0	0
1	0	0	0	0	1	1	1	)	0	1
0	0	0	1	0	1	1	1	) (1)	0	0
0	0	1	1	0	1	1	1	)	0	0
0	1	0	1	0	1	1	1	)	0	0
0	1	1	1	0	1	1	1	)	0	0
1	0	0	1	0	1	1	1	)	1	1
0	0	0	0	1	0	0	1	)	0	0
0	0	1	0	1	0	0	1	)	0	0
0	1	0	0	1	0	0	1	)	0	0
0	1	1	0	1	0	0	1	)	0	1
1	0	0	0	1	0	0	1	)	1	1
0	0	0	1	1	0	0	1	) (3)	0	0
0	0	1	1	1	0	0	1	)	0	0
0	1	0	1	1	0	0	1	)	0	0
0	1	1	1	1	0	0	1	)	1	1
1	0	0	1	1	0	0	1	)	1	1
0	0	0	0	1	1	0	0	)	0	0
0	0	1	0	1	1	0	0	)	0	0
0	1	0	0	1	1	0	0	)	1	1
0	1	1	0	1	1	0	0	)	1	1
1	0	0	0	1	1	0	0	)	1	1
0	0	0	1	1	1	0	0	) (6)	0	0
0	0	1	1	1	1	0	0	)	0	1
0	1	0	1	1	1	0	0	)	1	1
0	1	1	1	1	1	0	0	)	1	1
1	0	0	1	1	1	0	0	)	1	1
0	0	0	0	1	1	1	1	)	0	1
0	0	1	0	1	1	1	1	)	1	1
0	1	0	0	1	1	1	1	)	1	1
0	1	1	0	1	1	1	1	)	1	1
1	0	0	0	1	1	1	1	)	1	1
0	0	0	1	1	1	1	1	) (9)	1	1
0	0	1	1	1	1	1	1	)	1	1
0	1	0	1	1	1	1	1	)	1	1
0	1	1	1	1	1	1	1	)	1	1
1	0	0	1	1	1	1	1	)	1	1

MN15		MN16		
a	b	a	b	
(12)	(9)	(12)	(9)	
1	1	1	0	
0	1	1	0	
1	0	1	0	
1	1	0	1	
0	1	0	1	
1	0	0	1	
1	0	1	1	
1	1	0	0	
0	1	0	0	
1	0	0	0	
1	1	1	0	NEW CYCLE

TABLE 2-3. MN15/MN16 COUNT SEQUENCE

circuit. If the bistable is in the state MN13c(1) = 1 and MN13d(13) = 0, a positive pulse appearing at MN13b(4) will cause the state of the bistable to be reversed, while a pulse appearing at MN13a(1) will have no effect. If the bistable is in the opposite state (MN13c(10) = 0 and MN13d(13) = 1), a positive pulse appearing at MN13a(1) will cause the state of the bistable to be reversed, while a pulse appearing at MN13b(4) will have no effect. Thus the bistable circuit is made to alternate between its two states by the alternate appearance of pulses at MN13b(4) and MN13a(1). The mark-to-space ratio of the resultant waveform is proportional to the phase difference between the two 100 kHz input signals. This output wave form is applied to a transistor switch VT10 and fed out to the 10.45 MHz V.C.O. Board, where an oscillator d.c. control voltage is derived.

The phase locked loop, of which the comparator is a part, does not, due to finite gain, reduce the phase difference between the reference and divider out-put signals to zero, but to a small value depending on the initial frequency of the V.C.O.; this varies over the frequency range of the loop. Thus over the required frequency range of the V.C.O., there is a corresponding range of mark-to-space ratio at the compartor output and a corresponding range of phase difference between the signals at the comparator inputs.

As the kHz and Hz x 100 digits of the selected channel frequency are varied and the division ratio of the programmable divider changed, the

comparator will cause the loop to "lock" at a point where the phase difference between the comparator input signals is such as to provide a mark-to-space ratio at the comparator output and hence an oscillator control voltage which will give the required frequency output from the V.C.O.

If the frequency of the programmable divider output is much higher than the reference frequency, MN18 will reach a count of 1 0 0 1 before a pulse appears at MN13a(1) to change the bistable state back to MN13d(13) = 0. The combination of a 1 at MN18(7) from MN13d(13) and a 1 at MN18(6) from MN11d (11) forces MN18 to a count of 1 0 0 1. This causes MN11d(11) to remain at 1 and no trailing edge pulse is produced at MN13b(4). This condition is held until a pulse does appear at MN13a(1) to reverse the state of the bistable. During the inactive period, MN13d(13) remains at 1 to provide a maximum correction signal of the required polarity to reduce the frequency of the 10.45 MHz V.C.O. until the pulses at MN13b(4) and MN13a(1) appear alternately again. If the 100 kHz reference frequency is the higher, the opposite side of the circuit will behave in the same way to provide a zero at MN13d(13) which increases the frequency of the 10.45 MHz V.C.O. In this way the comparator circuit behaves as a frequency comparator for large frequency differences to provide rapid stabilisation of oscillator frequency at switch-on by producing maximum correction of the required polarity until the frequencies are close enough for the phase comparison to be effective.

The frequency/phase comparator for the control phase locked loop is identical with that for the low frequency phase locked loop except that the input frequencies are both 1 MHz and that the output is fed to the 10.7 MHz V.C.O. Board.

A divided reference frequency output is taken from the A output of decade counter MN1 at a frequency of 500 kHz and applied to the clock input of J-K flip-flop MN2. The output at MN2(8) is 250 kHz provided the flip-flop is enabled by a 1 on the J1 input MN2(3) which is the KEY input inverted by MN12b. Thus, when there is a 0 on the KEY input, a 250 kHz reference signal is produced. This signal is amplified by VT7, VT8 and VT9, and fed to the S.S.B. Generator to provide the carrier frequency.

4. PULSE SWALLOWER MODULE 1J66452

Refer to circuit diagram, Fig. 2-20 and to logic sequence, Fig. 2-21

4.1 General

The Pulse Swallower Module is the programmable frequency divider of the high frequency phase locked loop and provides division ratios in the range 1.60 to 29.99 as determined by the MHz x 10, MHz, kHz x 10 digits of the selected channel frequency.

4.2 Principles of Operation

The divider logic is set to provide frequency division by a base number corresponding to the MHz x 10 and MHz digits of the selected channel frequency. The division ratio is increased to one more than the base number for a percentage of the time as determined by the kHz x 100 and kHz x 10 digits of the

selected channel frequency as follows:

(i) 0 - 90% as determined by the kHz 100 digit, plug
(ii) 0 - 9% as determined by the kHz x 10 digit.

For the example channel frequency setting (21.4963 MHz), the value of the MHz x 10, MHz, kHz x 100 and kHz x 10 digits is 21.49 MHz. The divider will be set to a division ratio of 21 which will be increased to 22 for 49% of the time, made up as follows:

(i) 40% as determined by the kHz x 100 digit (4), plus
(ii) 9% as determined by the kHz x 10 digit (9).

Thus, over a sequence of 100 divisions, 51 will be divisions by 21, and 49 will be divisions by 22. The average (effective) division ratio will be 21.49.

For selected channel frequencies in the range 1.6 MHz to 9.9999 MHz, the divided V.C.O. output (nominally 1 MHz) along with the 1 MHz reference signal (also processed in this module), before being applied to the Phase Comparator Module, is processed in identical circuits which perform the operation $X\frac{M1}{10}$; where M_1 is the value of the MHz digit of the selected channel frequency. This operation provides, in the above frequency range, a range of comparison frequencies at the module outputs. In this way the low frequency portion of the gain/frequency response relationship for the high frequency phase locked loop is shaped as required for optimum performance. For selected channel frequencies in the range 10.0000 MHz to 23.0000 MHz, the $X\frac{M1}{10}$ operation is bypassed.

4.3 Circuit Description

The sinusoidal input from the Control Down-Mixer Board is squared by clipping amplifier VT3/MR1. The square-wave output from VT3 collector is fed to the clock inputs of J-K flip-flops MN1a, MN1b and MN6, and constitute the input pulses to be divided.

Control inputs representing the MHz x 10 and MHz digits of the selected channel frequency appear on the inputs of a BCD to binary converter array comprising 2-bit full adder MN9, and 4-bit full adders MN10 and MN24.

The control input code for the two digits is inverse BCD (zeros are active) and the two digits are combined in MN24 to provide a five-bit inverse-binary number representing the combined value of the MHz x 10 and MHz digits (M). This is achieved by adding the three most significant bits of the MHz digit to the two bits of the MHz x 10 digit: the 10-weight line of the MHz x 10 digit is added in both the 8-weight and 2-weight positions of the B input, while the 20-weight line is added in both the 16-weight and 4-weight positions of the B input. The 8, 4 and 2-weight lines of the MHz digit are applied to the inputs of MN24 with a permanent 1 (inverse 0) applied to the 16-weight position (there is no 16-weight line for the MHz digit). The 1-weight bit of the MHz digit is considered directly as the 1-weight bit of the combined number as this bit is not

affected by any value of the MHz x 10 digit.

The inverse binary number produced by MN24 is applied to the A inputs of a 5-bit adder array comprising MN10 (providing the 1, 2, 4 and 8-weight positions) and MN9 (providing the 16-weight position). To the B inputs of MN10 and MN9 is applied either all zeros or all ones depending on the state of the flip-flop MN11 pin 5 (Q). A permanent carry is injected to the 1-weight position (+5 V at MN10 Co). The resulting output from MN10 and MN9 is a binary number representing 32-M if MN11(5) = 0, or 32-M+1 if MN11(5) = 1 (M is the combined value of the MHz x 10 and MHz digits). Refer to Table 2-4 for a summary of the BCD-binary converter operation.

The 2, 4, 8 and 16-weight bits of the converter output are applied to the data inputs (D_A, D_B, D_C and D_D) of presettable binary counters MN3 and MN5. The 1-weight bit of the converter output is applied to a network of NAND gates, MN2a, MN2b, MN2c, MN2d and MN20b. This network determines the behaviour of flip-flops MN1a and MN1b under the influence of the 1-weight bit and the outputs of flip-flop MN6. For example, if MN6(8) = 1, and MN10(9) = 1, MN2d(11) will be at 0 and hold MN1a set (Q = 1): Both MN2a(3) and MN2b(6) will be 1 and MN1b is free to toggle under the influence of VT3 collector waveform. The behaviour of MN1a and MN1b under control of MN6 and MN10(9) is summarised in Table 2-5, below.

Assuming that MN6(8) = 1, as before; MN1a is held at Q = 1 and MN1b toggles. Presettable binary counter MN5, having previously been loaded with the four most significant bits of the BCD to binary converter output, is advanced by the output of MN1b(10). While MN5 is being advanced, presettable binary counter MN3 is held at the states of the 2, 4, 8 and 16-weight bits of the BCD to binary converter output by a 0 at the STROBE input from MN6(6). When MN5 reaches the 'full' state (1 1 1 1), both MN4(12) and MN5(5) go to 1 and the 'K' input gate of MN6 is enabled during the next 1 state of MN1b(10). The next input pulse which occurs while this state prevails reverses the state of MN6. The number of input pulses which pass before MN6 changes state is twice the number required to advance MN5 to the full state (MN1b introduces division by 2), plus 1 waiting for MN1b(10) to go to 1. As MN6(8) goes to 0, MN5 is loaded with the data inputs and held at this count. As MN6(6) goes to 1, MN3 is released and commences to advance from the previously loaded count under control of MN1a(15) which begins to toggle (see Table 2-5). When MN3 reaches the full state, both MN4(8) and MN3(5) go to 1 and the 'J' input gate of MN6 is enabled during the next 1 state of MN1a(15). The next input pulse which occurs while this state prevails will reverse the state of MN6 (the inherent 1-pulse delay applies as for MN5 above); MN3 is again loaded and held, and the cycle repeats. The pulse shaping network MN7d and MN8d produces a negative pulse of constant width for each 0 to 1 transition of MN6(8). The pulse width is determined by the delay of MN7d and the time constant R9/C5. Similarly, MN7a and MN8a produce a negative pulse for each 0 to 1 transition of MN6(6). Therefore at MN20(11) there appears a positive output pulse of constant width and amplitude for every change of MN6 state so that MN6 itself introduces no further division by 2.

Pulses from MN20d(11) are applied to the $X\frac{M1}{10}$ circuit.

The 1-weight bit of the BCD to binary converter output MN10(9) determines at which state the appropriate flip-flop MN1a or MN1b is held during its inactive period (refer to Table 2-5). This, in turn determines whether MN3 or MN5 commences counting at the first input pulse following its release (MN6(6) or (8) going to 1), or is forced to wait for the second input pulse. This occurs because MN3 and MN5 count on the negative going edge of the input pulse and therefore count only 1 to 0 transitions. If the pulse train from MN1a(15) or MN1b(10) begins with a 1 and 0 transition, counting commences with the first input pulse. If MN1a(15) or MN1b(10) has been held at 0 during the inactive period the first transition will be 0 to 1 and will be ignored; counting will not commence until the second (1 to 0) transition. In this way the division ratio is increased by 1 over that determined by MN1a/MN3 or MN1b/MN5 plus the inherent one pulse delay at the end of the count.

Freq. Setting MHz x10	MHz	Control Inputs MHz x 10 20	10	MHz 8	4	2	1	(M) Binary MN22 (15) 16	(2) 8	(6) 4	(9) 2	1	Comparison Frequency (kHz)	OUTPUTS MN9 (1)	(15)	MN10 (2)	(6)	(9)	Base Division Ratio
0	1	1	1	1	1	1	0	1	1	1	1	0	100,000	1	1	1	1	1	1
0	2	1	1	1	1	0	1	1	1	1	0	1	200,000	1	1	1	1	0	2
0	3	1	1	1	1	0	0	1	1	1	0	0	300,000	1	1	1	0	1	3
0	4	1	1	1	0	1	1	1	1	0	1	1	400,000	1	1	1	0	0	4
0	5	1	1	1	0	1	0	1	1	0	1	0	500,000	1	1	0	1	1	5
0	6	1	1	1	0	0	1	1	1	0	0	1	600,000	1	1	0	1	0	6
0	7	1	1	1	0	0	0	1	1	0	0	0	700,000	1	1	0	0	1	7
0	8	1	1	0	1	1	1	1	0	1	1	1	800,000	1	1	0	0	0	8
0	9	1	1	0	1	1	0	1	0	1	1	0	900,000	1	0	1	1	1	9
1	0	1	0	1	1	1	1	1	0	1	0	1		1	0	1	1	0	10
1	1	1	0	1	1	1	0	1	0	1	0	0		1	0	1	0	1	11
1	2	1	0	1	1	0	1	1	0	0	1	1		1	0	1	0	0	12
1	3	1	0	1	1	0	0	1	0	0	1	0		1	0	0	1	1	13
1	4	1	0	1	0	1	1	1	0	0	0	1		1	0	0	1	0	14
1	5	1	0	1	0	1	0	1	0	0	0	0		1	0	0	0	1	15
1	6	1	0	1	0	0	1	0	1	1	1	1		1	0	0	0	0	16
1	7	1	0	1	0	0	0	0	1	1	1	0	1 MHz	0	1	1	1	1	17
1	8	1	0	0	1	1	1	0	1	1	0	1		0	1	1	1	0	18
1	9	1	0	0	1	1	0	0	1	1	0	0		0	1	1	0	1	19
2	0	0	1	1	1	1	1	0	1	0	1	1		0	1	1	0	0	20
*2	1	0	1	1	1	1	0	0	1	0	1	0		0	1	0	1	1	21
2	2	0	1	1	1	0	1	0	1	0	0	1		0	1	0	1	0	22
2	3	0	1	1	1	0	0	0	1	0	0	0		0	1	0	0	1	23
2	4	0	1	1	0	1	1	0	0	1	1	1		0	1	0	0	0	24
2	5	0	1	1	0	1	0	0	0	1	1	0		0	0	1	1	1	25
2	6	0	1	1	0	0	1	0	0	1	0	1		0	0	1	1	0	26
2	7	0	1	1	0	0	0	0	0	1	0	0		0	0	1	0	1	27
2	8	0	1	0	1	1	1	0	0	0	1	1		0	0	1	0	0	28
2	9	0	1	0	1	1	0	0	0	0	1	0		0	0	0	1	1	29

TABLE 2-4 PULSE SWALLOWER CIRCUIT STATES

* Example Channel Frequency Setting

MN6	MN10		MN1a	MN1b
(8)	(6)	(9)		
1	0	1	Held at Q = 1	Toggles
1	0	0	Held at Q = 0	Toggles
0	1	1	Toggles	Held at Q = 0
0	1	0	Toggles	Held at Q = 1

TABLE 2-5 BEHAVIOUR OF MN1a AND MN1b

To summarise, presetable counters MN3 and MN5 are alternately loaded with the four most significant bits of the BCD to binary converter output, and advanced from the loaded count to the full state. Flip-flop MN6 controls the alternation and provides an output pulse at each change. The four-bit binary value loaded to MN3 and MN5 is determined by the MHz x 10 and MHz digits of the selected channel frequency. For odd-numbered base division ratios, this binary value is chosen so that the number of input pulses required to advance MN3 or MN5 from the loaded binary value to the full state is one less than the required base division ratio; the ratio is increased by one by the inherent one pulse delay at the end of the MN3 or MN5 count. For even numbered base division ratios the binary value loaded to MN3 and MN5 is the same as for the next lower odd number; thus the number of input pulses required is now two less than the required base division ratio. The ratio is increased by two by the inherent one pulse delay plus an additional one pulse delay caused by the action of the 1-weight bit of the BCD to binary converter output.

Pulses from MN20d(11), as well as being fed to the $X\frac{M1}{10}$ circuit, are applied to the 'A' input of divide-by-ten circuit, MN12. When MN12 reaches a count of 1 0 0 1 (9), MN13b (4) and (5) go to 1 and the next (10th) MN20d(11) pulse passes to MN17c as well as to the STROBE input of presetable binary counter MN15 which will be loaded with its data inputs. While MN12 is counting, pulses from MN20d(11) are being passed by MN21b to the clock input MN15. Gate MN21b is enabled * because MN20b will not be energised† until a count of 1 0 0 1 (9) is reached by MN12, nor will MN14a be energised until a count of 1 1 1 1 (15) is reached by MN15. Appearing on the data inputs of MN15 are control inputs representing the kHz x 100 digit of the selected channel frequency. The control input code which is shown in Table 2-6, is an inverse BCD (zeros are active) and hence is the "fifteens complement" of the character selected. The "fifteens complement" of a binary number is that value which, when added to the original value produces a sum of 1 1 1 1 (15): for example the number 4 (0 1 0 0) in inverse BCD is 1 0 1 1 which when added to 0 1 0 0 produces a sum of 1 1 1 1 (15). The implication of this is that when the inverse BCD value is

loaded to the counter, the number of clock pulses required to advance the counter to the full state (1 1 1 1) is equal to the value of the digit selected: for the above example, four pulses are required to advance the counter from 1 0 1 1 (inverse BCD 4) to 1 1 1 1 (15).

* Enabled denotes a gate ready to pass a positive going pulse

† Energise denotes the state of a NAND gate when all its inputs are high.

Frequency Setting	Control Lines			
	8	4	2	1
0	1	1	1	1
1	1	1	1	0
2	1	1	0	1
3	1	1	0	0
4	1	0	1	1
5	1	0	1	0
6	1	0	0	1
7	1	0	0	0
8	0	1	1	1
9	0	1	1	0

TABLE 2-6.

Control Line Coding for kHz x 100
and kHz x 10 digits of Selected Channel Frequency

Pulses passed by MN21b advance MN15 from the loaded value to the full state (1 1 1 1). When the full state is reached MN14a(6) goes to 0 and inhibits further pulses from MN21b. Gate MN20b also inhibits pulses from passing MN21b while the count of MN12 is at 1 0 0 1 (9): this prevents the pulse which strobed MN15 via MN13b from prematurely advancing MN15 via MN21b. Each pulse which is passed by MN21b sets MN11 to Q = 1 via MN21c and MN17d. The setting of MN11 causes the output of the BCD to binary converter MN9, MN10, MN24 to be increased by 1 and the division ratio for the following cycle will be one greater than the base number (refer Table 2-4). The next pulse from MN20d(11) resets MN11 to Q = 0 ready for the next pulse from MN21b. Thus, for every group of ten pulses from MN20d(11) the first 'n_1' pulses are

passed by MN21b to set MN11 ('n_1' is the kHz x 100 digit of the selected channel frequency). The division ratio of the divider logic will therefore be one greater than the base number for 'n_1' x 10% of the time. In this way the setting of the kHz x 100 digit determines the first decimal place of the over-all division ratio.

Pulses MN13b(6) are at one tenth the frequency of those from MN20d(11) due to the action of MN12. These pulses are applied via an inverter, MN17c to a circuit identical to that used to handle the kHz x 100 digit. The presetable counter is MN18 and the divide-by-ten is MN16. The first 'n_2' pulses will be passed by MN21a to set MN11 ('n_2' is the kHz x 10 digits of the selected channel frequency). Each pulse passed by MN21a corresponds to the tenth pulse of the appropriate group considered above for the kHz x 100 digit. Seeing that the tenth pulse is never passed by MN21b (9 is the maximum number passed), the pulses passed by MN21a do not overlap any pulses passed by MN21b. The division ratio of the divider logic will therefore be one greater than the base number for a further 'n_2'% of the time. In this way the setting of the kHz x 10 digit determines the second decimal place of the overall division ratio.

The sinusoidal 1 MHz reference signal from the Power Supply Module is amplified by VT4 and squared by VT5. The square wave at VT5 collector is inverted by MN28b and fed out to the 2nd I.F. Loop Module to serve as the phase comparison reference in the low frequency and control phase locked loops. The square wave of VT5 collector is also inverted by MN28a and applied to the $X\frac{M1}{10}$ circuit.

Thus far, two signals have been produced in the Pulse Swallower Module:

(i) The divider output at MN20d(11) - frequency 1 MHz when main V.C.O. is on correct frequency.

(ii) Shaped 1 MHz reference pulses at MN28a(2).

Before being applied to the Phase Comparator Module, these two signals are fed to the $X\frac{M1}{10}$ circuit.

The $X\frac{M1}{10}$ circuit comprises rate multipliers MN26 (divided V.C.O. output) and MN27 (1 MHz reference), four-bit latch MN23, four-bit magnitude comparator MN22 and supporting circuitry. Divided V.C.O. pulses from MN20d(11). are applied to the input of rate multiplier MN26 and 1 MHz reference pulses from MN28a(2) are applied to the input of rate multiplier MN27. The 1, 2, 4 and 8-weight bits of the inverse binary value from the BCD to binary converter are fed to the data (D) inputs of four-bit storage MN23. The inverted outputs of MN23 represent a normal binary value and are applied to the rate inputs of MN26 and MN27 to control the action of these circuits. The effect of MN26 and MN27 will be $X\frac{M1}{10}$; where M_1 is the value of the MHz digit of the selected channel frequency. The Q outputs of MN23 (inverse binary) are applied to the B inputs of magnitude comparator MN22. To the A inputs of MN22 are applied the

1, 2, 4 and 8-weight bits of the inverse binary value from the BCD to binary converter.

The circuit is controlled by a timer circuit VT1, C11, R4, R5 and R6, which together form a monostable circuit with a duration of approximately four seconds. As long as the four least significant bits of combined MHz and MHz x 10 digits remain unchanged, the "A=B" output of MN22 is 1; VT1 is normally conducting and MN19d(13) is 0. This causes MN19d(11) to be 1, MN19a(3) to be 0 and MN28f(11) to be 1. Capacitor C11 will charge to 5 V. When any of these bits change, the A inputs of MN22 will no longer be equal to the B inputs seeing that the Q outputs of MN23 do not change until the new data levels are entered by the receipt of a clock pulse. The inequality of the inputs to MN22 cause the "A=B" output to go to 0 and MN28f(12) to go to 1. This places the charged C11 across the base-emitter junction of VT1 with negative at the base. This cuts VT1 off and the collector swings to +5 V clocking the new data levels into MN23, whereupon the "A=B" output returns to 1. Meanwhile MN19d(11) has gone to 0 and MN19a is rendered insensitive to the "A=B" output of MN22. The 1 at MN 19a(3) is applied via inverter MN25d and NAND gate MN25c to the strobe inputs of MN26 and MN27, and to the NAND gates MN19c and MN19b. If there is a zero selected for the MHz x 10 digit of the channel frequency, MN25a(3) will be 0, MN25b(6) will be 1 and MN25c will be enabled. The input pulses to pin 9 of the rate multipliers are passed via MN19c and MN19b to the UNITY CASCADE input and thence via internal logic to the Y output effectively by-passing the division logic. The circuit remains in this state until C11 has discharged sufficiently for VT1 to commence conduction again (approximately four seconds). Thus, for the duration of the timer, the $X\frac{M1}{10}$ circuit is disabled, the comparison frequencies are 1 MHz, and the loop gain is highest. This ensures rapid initial frequency stabilisation after change of channel. The four second period is chosen to exceed slightly the maximum possible stabilising time at the high gain; this occurs when a channel frequency change is made from 29.9999 MHz to 1.6000 MHz. When the timer reverts to its stable state, the loop gain is once more under control of the selected MHz digit for final locking. If there is a 1 or a 2 selected in the MHz x 10 position of the channel frequency, MN25a(3) will be 1, MN25b(6) will be 0 and MN25c(8) will be permanently 1 causing the $X\frac{M1}{10}$ circuit to be permanently bypassed regardless of the timer operation. Thus for frequencies in the range 1.6000 MHz to 9.9999 MHz the comparison frequency, and hence loop gain, is under control of the MHz digit of the selected frequency. For frequencies in the range 10.0000 MHz to 29.9999 MHz the comparison frequency is 1 MHz and the loop gain at the comparator is highest.

The outputs from MN26 and MN27 are taken to the Phase Comparator Module via pulse shaping networks similar to those used on the outputs of MN6.

4.4 Example Channel Frequency Setting

Refer to Divider Sequence Diagram Fig. 2-21.

Figure shows the divider logic sequence for the example channel frequency setting of 21.4963 MHz. Section A of Figure 2-21 covers the operation of the

main divider, Section B covers the operation of the kHz x 100 digit circuit and Section C covers the operation of the kHz x 10 circuit.

The binary value loaded to the counters MN3 and MN5 is 0 1 0 1 and 10 pulses from MN1a or b are required to advance MN3 or MN5 to the full state. These 10 pulses, along with the divide-by-two action of MN1a, or b, and the 1-pulse delay after the full state of MN3 or MN5, provide a division ratio of 21.

The least significant digit of the BCD to binary converter output is 1 and no 1-pulse delay is introduced at the commencement of MN3 or MN5 count. For the first two division cycles shown, no pulse appears to set MN11 and two divides by 21 result. At the beginning of the third division cycle shown, a pulse from MN21a(12) sets MN11. The states of MN1a and MN1b are reversed and the third division cycle is a divide by 22 due to the 1-pulse delay at the commencement of MN5 count. At the beginning of the fourth division cycle shown, a pulse from MN21b(6) sets MN11 - after a momentary resetting by MN20d(11)- and another divide by 22 results.

Section B shows how, under control of the kHz x 100 digit (4), the first four pulses of every group of ten are passed by MN21b(6) to set MN11. The 'fifteens complement' of 4 (1 0 1 1) is loaded to MN15 and four pulses are required to advance MN15 to the full state.

Section C shows how, under control of the kHz x 10 digit (9), the first nine pulses of every group of ten are passed by MN21a(12) to set MN11. Transferring the MN21a(12) waveform to the time scale of Section B shows how the pulses passed by MN21a(12) do not overlap any passed by MN21b(6).

The MHz x 10 digit is 2 and the $X\frac{M1}{10}$ circuit is bypassed; the comparison frequency is 1 MHz.

5. PHASE COMPARATOR MODULE 1J66453

Refer to circuit diagram, Fig. 2-22.

5.1 General

The Phase Comparator Module performs the frequency/phase comparison function for the high frequency phase locked loop. The module receives the divided output from the Pulse Swallower Module and the 1 MHz reference frequency via the Pulse Swallower Module. The Phase Comparator Module provides separate coarse and fine correction outputs and an adjustable d.c. bias. The coarse output from the digital to analogue (D/A) converter is inversely proportional to exciter output frequency, but the fine output is connected in the reverse sense.

5.2 Circuit Description

5.2.1 Coarse Comparator

Positive pulses from the output of the Pulse Swallower Module are applied to a pulse shaping network MN8d, C2, R127, MR1 and Mn7a. The network produces a short negative pulse of width determined by the time constant R127/C2.

The pulse is positioned after the trailing edge of the input pulse. This pulse is inverted by MN7f and the resulting positive pulse applied to MN6c(9). Negative pulses from the 1 MHz reference are inverted by MN7c and applied to a pulse shaping network MN8c, C3, R128, MR2 and MN7b which is identical with that described above and positive pulses from MN7e(10) appear at MN6d(13). Pulses from MN6c(8) are applied to the "Down count" input of Up/Down Binary Counter MN5. Similarly, pulses from MN6d(11) are applied to the "Up count" input of MN5. Depending on which of the input frequencies is the higher, MN5 will count up or down. If the reference output is higher there are more pulses appearing at the up count input to increase the count than there are at the down count input to decrease the count and the nett effect is an increase of the count at a rate equal to the frequency difference. If the divided frequency is the higher, then the opposite is the case and the count decreases. The increasing or decreasing count in MN5 will be propagated down the counter array MN5 to MN1 by carries and borrows. Carries generated by MN5 at counts of 1 1 1 1 constitute up count pulses for MN4 and so on down to MN1. Similarly, borrows generated by MN5 at counts of 0 0 0 0 constitute down count pulses for MN4 and so on down to MN1. Thus the count in the entire 20-bit array will be counting either up or down depending on which of the input frequencies is the higher. Should the array reach the maximum count (all counters at 1 1 1 1) a carry will emerge from MN1(12) and cause all counters to be loaded with 1 1 1 1: thus the array, rather than moving to all zeros, will "stall" at all ones until a down count pulse is received. Similarly, should the array reach the minimum count (all counters at 0 0 0 0) a borrow will emerge from MN1(13) and, via MN6b, clear all counters to 0 0 0 0; thus the array, rather than moving to all ones, will "stall" at all zeros until an up count pulse is received. Each of the twenty stages of the counter array controls a transistor switch which in turn controls the distribution of resistance in a resistive voltage divider network comprising R1 to R19, R20 to R39, R40 to R59, R121 and R122. Regulators MN10 and MN11 in conjunction with external series pass transistors VT23 and VT24, operate in series to provide a stable reference voltage of +15 V which is applied to the voltage divider network. When a stage of the counter array goes to 1 the associated transistor conducts, effectively connecting the collector resistor junction to earth and reducing the percentage of the +15 V reference which appears at the D - A output. The network is arranged so that the transistors associated with successively higher value binary stages have successively greater effect on the voltage at the D - A output through being spaced along the series chain R1 to R19. With the counter stalled at all ones, all transistors are conducting and the D - A output is at earth potential. With the counter stalled at all zeros, all transistors are cut off and the D - A output is near +15 V. Thus the voltage at the D - A output is representative of the count in the array, and in the locked state, the count is proportional to exciter frequency. Coincidence of the two input pulses at MN8d(12) and MN8c(9) is sensed by MN8b which provides a negative pulse corresponding to the period of coincidence. This negative pulse is applied to a monostable circuit MN6a, C1, R126 and MN7d which provides a negative pulse of approximately 400 ns determined by the time constant C1/R126. The leading edge of the monostable output pulse corresponds approx-

imately to the leading edge of the lagging input pulse. The monostable output pulse is applied to inhibit MN6c and MN6d and effectively blocks both trailing edge pulses. This feature prevents error due to confusion of pulses arriving simultaneously on up and down count inputs of MN5. Voltage regulator MN12 provides a separate 5 V supply for low noise operation of the counter logic MN6-9.

5.2.2 Fine Comparator

Input pulses from the output of the Pulse Swallower Module are applied to the clock input of flip-flop MN9b and the inverted reference input from MN7c is applied to the clock input of flip-flop MN9a. Each input pulse can set the flip-flop to Q = 1. As soon as both flip-flops are at Q = 1, MN8a(3) goes to 0 and both flip-flops will be reset to Q = 0. The pulse which arrives first sets the associated flip-flop which remains set until the other pulse arrives to set the other flip-flop at which time both flip-flops will be reset. Thus the pulse which arrives first produces at the Q output of the associated flip-flop a pulse of width proportional to the leading edge phase difference of the input pulses. The Q outputs of MN9a and MN9b are applied to the inputs of differential amplifier MN13 via integrating circuits. As long as the two input frequencies are different, the Q output pulses from MN9a and MN9b will be moving with the respect to each other and passing through a point of coincidence at a rate equal to the frequency difference. As the pulses move from one coincidence point to the next, the pulse width at the Q output associated with the higher frequency will increase until at the next coincidence point the pulse width reverts to the minimum width before beginning to increase again. The result is an increase of charge on the integrating capacitor between coincidence points, and a relatively rapid collapse as the pulse width collapses at coincidence. The output from MN13(6) will therefore be a sawtooth voltage at a frequency equal to the frequency difference. The polarity of the waveform is indicative of which input frequency is higher, a negative polarity indicating that the divided output is the higher. When the input frequencies are the same and the pulses are coincident, the sawtooth waveform at MN13(6) collapses to zero.

The 10 kHz and 100 kHz components of the output waveform are attenuated by L-C notch filters, being L3, L4, C31-36, C39.

5.2.3 System Operation

The error voltage outputs of the coarse comparator and the fine comparator are fed to the V.C.O. Control Board where they are compensated to provide control voltages for the Main V.C.O. The output of the coarse comparator is in the range 0 to +15 V and can control the main V.C.O. over its entire range: the output of the fine comparator is in the range +3 V to -3 V and can control the oscillator over a range of approximately ±50 kHz. An adjustable bias of 14 V ±1 V, provided by R125 & RV1, is fed directly to the Main V.C.O. as the positive side of the differential oscillator control voltage.

When the channel frequency setting is changed a large amount, the counter array of the coarse comparator commences to count, initially, at a

high rate (equal to the frequency difference) up or down. The D - A output voltage begins to change rapidly towards the required level. Meanwhile, the fine comparator output is a sawtooth waveform corresponding in frequency and polarity to the difference and direction of the input signals. The fine comparator output is small compared with the coarse comparator output and has little effect at this stage. As the frequencies become closer due to the effect of the changing control voltage, the counting in the coarse comparator slows down and the fine comparator output becomes meaningful in tending to increase the speed of frequency correction in the last stages of closure and reducing any tendency for the coarse comparator output to "overshoot". A point will be reached where the two input frequencies are equal and the pulses interlace where the phase locked loop assumes a steady state with the fine comparator output maintaining a fixed d.c. voltage. In practice, however, there will always be small random changes in pulse position and these will cause output pulses from the fine comparator output to correct these changes. As long as the changes are small, they will be corrected by the fine comparator. If the changes become larger, the counter of the coarse comparator will count up or down and so keep the smaller changes within the narrower effective range of the fine comparator.

6. AUTO ATTENUATOR MODULE 1J66455

Refer to circuit diagram, Fig. 2-23.

6.1 General

The Auto Attenuator Module has two main sections each with a separate circuit function, viz.,

(i) The audio section which provides amplification and gain adjustment for the audio signal applied to the S.S.B. Generator Module as well as providing test tones and facilities for selecting the audio source for amplification.

(ii) The Auto Attenuator proper which receives the 250 kHz modulated signal from the S.S.B. Generator, attenuates it according to various input conditions, and passes it on to the Frequency Translator Module.

6.2 Audio Section

The audio amplifier is a differential amplifier MN1 which is fed by a 600 Ω/600 Ω transformer TR2 via a gain control network R1 - R5 and RV1, and a "parallel H" 50 Hz notch filter R7, R8, R11 - R13 and C6 - C10 which provides rejection for unwanted noise at 50 Hz. The gain control network is arranged to present a nearly constant resistance of 600 ohms to the secondary of TR2 regardless of the setting of RV1. The input to the primary of TR2 is selected by the AUDIO INPUT switch SWA and will be one of three combinations of test tones, audio input line via R55 - R57, or a 600-ohm termination (R103).

There are two test tone oscillators: F1 (1100 Hz) and F2 (1600 Hz). Each oscillator comprises a linear differential amplifier connected as a Wien Bridge oscillator with an external a.g.c. control amplifier.

For the F2 oscillator (1600 Hz), the Wien Bridge network R34, C24, R35 and C25 is connected between output (pin 6) and one input (pin 3) of differential amplifier MN3. The network is arranged so that approximately 1% of the output amplitude is applied to input pin 3. So that the oscillator operates with minimum distortion, the amount of input signal applied to pin 2 input of MN3 should be just sufficient to maintain the circuit in oscillation. A network formed by R37, C27, R38 and the source-drain resistance of FET VT3, applies a portion of the output amplitude to input pin 2: the amount applied is controlled by the conduction of VT3. A sample of the output of the oscillator is taken by RV3 and applied to the gate of VT3 via a rectifier and filter. The resultant voltage on C28 controls the conduction of VT3 and is used, with adjustment provided by RV3, to select and maintain the optimum operating condition for the oscillator ensuring the best possible distortion figure.

At switch-on, C28 is discharged and VT3 conducts heavily providing, initially, a much smaller portion of the output at pin 2 than is normal; this ensures reliable starting of the oscillator. The oscillator frequency is determined by the total phase shift introduced by the Wien Bridge network and the amplifier. The F1 oscillator is identical with the F2 oscillator except for Wien Bridge values R20 and R21.

The differential amplifiers of both oscillators are connected directly to the -15 V supply and connected to the +15 V supply via the AUDIO INPUT switch SWA which selects the required oscillator. When both oscillators are selected, the +15 V supply is connected via isolation diodes MR14 and MR15. The oscillator outputs, via level controls RV8 (F1) and RV9 (F2) are applied to the base of test tone mixer amplifier VT1 via isolation resistors R31 and R32. The output of VT1 is available for selection as the audio source by SWA.

The AUDIO INPUT switch SWA has five positions, viz.,

(i) OFF
- Both tone oscillators off
- Audio input line disconnected
- TR2 primary disconnected and terminated in 600 ohms

(ii) LINE
- Both tone oscillators off
- Audio input line connected to audio amplifier via TR2

(iii) F1
- F1 tone oscillator on
- F2 tone oscillator off
- Output of test tone mixer connected to audio amplifier via TR2
- Audio input line disconnected

(iv) F2
- F2 tone oscillator on
- F1 tone oscillator off
- Output of test tone mixer connected to audio amplifier via TR2
- Audio input line disconnected

(v) F1/F2
- Both tone oscillators on

- Output of test tone mixer connected audio amplifier via TR2
- Audio input line disconnected

6.3 Auto Attenuator Section

The modulated 250 kHz signal from the S.S.B. Generator is applied to two amplifiers, the reference amplifier and the attenuator amplifier. The attenuator amplifier is a direct coupled pair VT5 and VT6 with heavy negative feedback provided by R52. The output circuit is transformer coupled by TR1 which has the primary tuned to 250 kHz; the secondary provides a 50-ohm balanced output to the Frequency Translator Module. The base of VT5 is capacitively fed from an attenuator network formed by R44 and the source-drain resistance of FET VT4. The gate voltage of VT4 controls the conduction of VT4 and hence the attenuation applied at the input to the amplifier.

The reference amplifier is a direct coupled pair VT11 and VT12 with heavy negative feedback provided by R86. The base of VT11 is capacitively fed and the output circuit is tuned to 250 kHz by L4 and C48. The output at C47 is rectified by MR11 and C49 is charged negatively by signal excursions to a voltage near the peak signal amplitude. The voltage at C49 is proportional to the signal amplitude. This voltage is applied via R65 to a summing junction. Also applied to the summing junction via R66 is a similarly derived but opposite polarity signal which is proportional to the transmitter r.f. output. When the two signals are of the same amplitude but of opposite polarity, the resultant or sum will be zero; any difference in voltage will produce an error voltage of the appropriate polarity. The summing junction is connected to the pin 3 input of differential amplifier MN4 which provides an output proportional to the difference voltage at the summing junction. This output is applied via switch FET (VT7) to the gate of attenuator FET (VT4) to control the attenuation at the input to the attenuator amplifier and hence the output at TR1 secondary. A negative error signal at the summing junction produces a negative control signal at the gate of FET VT4 and hence an increase in output level at TR1.

Output from the reference amplifier is also fed to the input of the trigger amplifier VT13 which controls switching network VT14, VT15, VT16 and VT17. The amplifier VT13 is a tuned stage which drives rectifier circuit MR12 and MR13 providing a negative voltage across C56 proportional to input signal level. The negative voltage holds VT14 in conduction, and hence VT15 and VT16 cut off. If the signal level should fall sufficiently, VT14 will cut off and allow VT15 and VT16 to conduct. When VT16 conducts a negative voltage is applied to the gate circuit of VT7. The negative voltage on VT7 gate is limited to a safe level by zener diode MR3. While VT7 is cut off, the voltage which existed at VT4 gate before the collapse of signal is maintained for a considerable period by the charge on C32; this is due to a long time constant provided by the high impedances of VT4 and VT7. The effect of this action is to maintain a constant system gain during breaks in traffic when operating on reduced or suppressed carrier, or when operating on keyed C.W. In all these cases, a break in traffic causes a large drop or complete disappearance of signal.

With mode switch SWB in the AUTO position, the resistive network R78, R71, R72 and RV6 applies a negative voltage offset to the pin 3 input of MN4 to provide a means of adjustment (via RV6) of the amount of attenuation produced by a given error voltage at the summing junction.

With SWB in the MANUAL position, the voltage at the wiper of RV7 is applied to the base of VT8 in the manual control switch and VT8 and VT9 will both conduct placing the junction of R78 and RV6 at earth potential and so remove the negative offset voltage from MN4 pin 3. The positive voltage at VT9 collector turns on VT10 which earths the summing junction. The removal of the offset voltage and the earthing of the summing junction together disable the automatic action of the circuit and cause VT4 to be biased under the control of RV7. As RV7 is turned clockwise, resistors R88, R89, R70 and diodes MR8 and MR9 apply an increasing positive voltage from RV7 wiper to pin 2 input of MN4, providing, as RV7 is removed, a manual control of VT4 conduction and hence of r.f. gain. Switching SWB to the AUTO position will cause an immediate reversion to automatic control regardless of the position of RV7. The trigger amplifier is effective whether in automatic or manual mode.

A facility is included to limit the 250 kHz output level at PLA25, PLA26 by applying a positive voltage to pin 3 of the control amplifier MN4 and hence increase attenuation of the signal to the base of VT5.

A sufficiently positive voltage at PLA17 will overcome the negative bias, adjustable by RV5, applied to the emitter of voltage amplifier VT17, causing VT17 to cut-off and allow a current to flow via R68, R67 and R63 to provide the required voltage at pin 3 of MN4.

This facility is used in the automatic mode to provide a constant output level to the transmitter during its coarse tuning cycle.

7. S.S.B. GENERATOR MODULE 1J66454

Refer to circuit diagram, Fig. 2-24.

7.1 General

The S.S.B. Generator Module is fed with both audio and 250 kHz r.f. inputs from which it produces a modulated output signal based on a carrier frequency of 250 kHz in one of six emission modes as selected by control input lines. The emission modes are as listed below:

(i) TUNE : Carrier only at 3 dB below rated p.e.p.

(ii) C.W. : Carrier only at rated p.e.p.

(iii) D.S.B. : Full carrier and both sidebands at rated p.e.p.

(iv) A3H : Full carrier and one sideband at rated p.e.p.

(v) A3A : Reduced carrier and one or two independent sidebands at rated p.e.p.

(vi) A3J : Suppressed carrier and one or two independent sidebands at rated p.e.p.

NOTE: For (v) and (vi) above, the S.S.B. Generator supplies only one sideband (usually the upper), the remaining sideband must be generated externally and fed to the S.S.B. Generator for addition to the signal.

The S.S.B. Generator Module comprises a number of discrete circuit elements which are utilised in various combinations as dictated by the voltages applied to the six control input lines (one for each emission mode). A voltage of +15 V is applied to the line corresponding to the emission mode required and certain of the circuit elements are energised to produce the desired emission mode. In Sub-section 7.2 below, the various circuit elements are described, and in Sub-section 7.3, the combined operation of the elements is summarised for the six emission modes.

7.2 Circuit Description

Diodes MR1, MR2, MR3 and MR4 with associated components form a balanced ring modulator which is fed with audio via a 10 dB pad R1, R2 and R3, and lowpass filter C1, L1 and C2 which prevents 250 kHz from being fed back to the audio source. The 250 kHz carrier is applied to the modulator by switching amplifier VT1, VT2 and VT3. Transistors VT1 and VT2 have a common emitter circuit: VT1 acts as a tuned amplifier and VT2 as a control switch. With no enabling voltage applied via one of the diodes MR5, MR6, MR7 or MR8, VT2 conducts heavily and VT1 is unable to operate. When enabling voltage is applied to VT1 base, the bias on VT2 is overcome and VT1 is able to operate. The output from VT1 collector drives emitter follower VT3 which switches the modulator.

The modulator output (comprising mainly upper and lower sidebands) from TR1 secondary is applied to a 250 kHz band-pass filter C17, C18, L2, C19, L3 and C21 which removes harmonics of 250 kHz produced by the switching action of the modulator.

From level control RV2 at the band-pass filter output, the signal is taken to an a.g.c. - controlled amplifier VT4, VT5 and VT6. The controlled stage VT4 is a dual gate MOSFET with signal applied to gate 1 and a.g.c. voltage applied to gate 2 to control the gain of the stage. The output from VT4 drain is capacitively coupled to tuned amplifier VT5 which feeds the d.s.b. switching amplifier VT7, s.s.b. switching amplifier VT17 (via the s.s.b. filter F1) and the a.g.c. amplifier VT6.

A.G.C. voltage is produced by VT6 which amplifies the signal output of VT5 from TR2 secondary and drives a rectifier circuit based on MR14. The network R52, RV3, R50, R51 and R49 provides a fixed bias (approximately +2 V developed across C30) for gate 2 of VT4, and a voltage delay for the a.g.c. by reverse biasing MR14 (adjusted by RV3). When the amplitude of the positive signal peaks exceeds the voltage developed across C35, MR14 conducts and charges C36 so as to produce a negative voltage which reduces the positive bias for gate 2 of VT4 and hence reduces the gain of VT4. The a.g.c. can be disabled by bridging C36 at printed circuit board pins 16 and 17 (the positive bias for gate 2 of VT4 is not affected).

The output from VT5 collector is applied to both the d.s.b. switching amplifier VT7 via level control RV11, and to the s.s.b. amplifier VT17 via the s.s.b. filter F1 and level control RV9. The s.s.b. amplifier VT17 amplifies the s.s.b. filter output (the selected sideband only - usually the upper) and drives the s.s.b. switching amplifier VT8 via a resistive hybrid combining network R113, R114, R116 and R117. The combining network enables an externally generated lower sideband applied via SKA16 and SKA18 to be added to the existing upper sideband to provide an independent sideband (i.s.b.) signal. At the input to VT7 and the s.s.b. filter a dual-polarity, biased diode level clipper is available for connection to the signal line by bridging printed circuit board pins 18 and 19. When connected, the clipper limits the maximum signal amplitude at the junction of R33, R41 and R39 to approximately 1.5 V peak-to-peak.

D.S.B. switching amplifier VT7 and s.s.b. switching amplifier VT8 share common emitter and collector circuits. The enabling voltage from SKA8 (d.s.b.) determines which of the two transistors behaves as the active element in the amplifier hence determines which input signal is amplified. When +15 V is applied to SKA8, operating bias is applied to VT7 base via R56 and R54. The current in VT7 produces an emitter voltage which exceeds VT8 base voltage and VT8 cuts off leaving VT7 free to amplify its base signal. When no +15 V is applied to SKA8, VT7 base is near ground potential and the current in VT8 due to the fixed bias produces an emitter voltage which exceeds VT7 base voltage and VT7 cuts off leaving VT8 free to amplify its base signal.

The output from TR3 secondary, whether due to the action of VT7 or VT8, feeds the module output via a resistive hybrid combining network R63, R64 and R66. The hybrid network enables local carrier from TR6 secondary to be re-inserted for emission modes requiring carrier.

Carrier signal for re-insertion is provided by amplifier VT9 and VT10 which is arranged in the same way as VT1 and VT2; VT9 is able to amplify when enabling voltage is applied to VT9 base via one of the diodes MR9, MR10, MR11, MR12 or MR13. Output from TR5 secondary is fed to the inputs of carrier re-insertion amplifiers VT11, VT12, VT13, VT14 and VT15 which share a common collector circuit, and, with VT16 share a common emitter circuit. The base circuits are separate and each provides a level control. For each of the five emission modes which require carrier re-insertion (viz. TUNE, C.W., D.S.B., A3H and A3A), one of the five amplifiers is enabled by the appropriate control line. In each case the +15 V applied to the base circuit causes VT16 to cut off as with VT2 above. Carrier output from TR6 is applied to hybrid combiner R63, R64 and R66 for re-insertion as described above. For emission mode A3J (suppressed carrier) no carrier re-insertion is required and +15 V is applied to VT16 base, causing VT16 to conduct heavily preventing the operation of the carrier re-insertion amplifiers VT11 - VT15.

From the secondary of TR3 (module output) a signal is taken to tuned amplifier VT18 which drives a level indicator meter circuit. Output from VT18 collector is rectified by MR17 and MR18 to provide a positive voltage across

filter capacitor C88. This voltage is applied to LEVEL meter M1 via range switch SWA which selects ranges of -10 dB or 0 dB. The meter indication can be adjusted using RV10 and the 0 dB range adjusted separately using RV12.

7.3 Functional Operation

Table 2-7 below summarises the combined operation of the circuit elements for the various emission modes selected.

MODE	+15 V to	CIRCUIT ELEMENT ENABLED	VIA	PURPOSE
TUNE	SKA10	VT9/VT10 VT11	MR9 R82	)Carrier only to output via)R63/R64/R66)Level set to rated p.e.p. -3 dB)by RV4
C.W.	SKA9	VT9/VT10 VT12	MR10 R87	)Carrier only to output via)R63/R64/R66)Level set to rated p.e.p. by RV5
DSB	SKA8	VT1/VT2 VT7	MR6 R56	250 kHz to modulator via VT3. Sidebands only to output via R63/R64/R66
		VT9/VT10 VT13	MR11 R92	)Carrier for re-insertion in)R63/R64/R66)Level set by RV6
A3H	SKA7	VT1/VT2 VT8	MR7 *	250 kHz to modulator via VT3. 1 sideband only via VT17 to output via R63/R64/R66
		VT9/VT10 VT14	MR12 R97	)Carrier for re-insertion in)R63/R64/R66)Level set by RV7
A3A	SKA6	VT1/VT2 VT8	MR8 *	250 kHz to modulator via VT3. 1 sideband only via VT17 to output via R63/R64/R66
		VT9/VT10 VT15	MR13 R101	)Carrier for re-insertion in)R63/R64/R66)Level set by RV8
A3J	SKA5	VT1/VT2 VT8	MR6 *	250 kHz to modulator via VT3. 1 sideband only via VT17 to output via R63/R64/R66
		VT16	R106	Disables all carrier re-insertion elements

* NOTE: VT8 enabled when no +15 V on VT7 base

TABLE 2-7 SUMMARY OF COMBINED OPERATION

8. POWER SUPPLY MODULE 1H66430

Refer to circuit diagram, Fig. 2-25

The Power Supply Module Type 1H66430 provides supply voltages for the circuits in the exciter and houses the internal 1 MHz reference oscillator.

The primary of power transformer TR1 is fed from the mains supply via suppression filters C1/L1/C2 and C3/L2/C4. The primary winding is fitted with taps to enable adjustment for different supply voltages. The secondary of TR1 comprises three separate windings each of which feeds a bridge rectifier assembly. The d.c. outputs from the rectifiers MR1, MR2 and MR3 are used to derive the various output voltages as follows:

1.	MR1 (d.c. output +15 V)	(i)	+5 V shunt regulated
2.	MR2 (d.c. output +24 V)	(i)	+24 V unregulated
		(ii)	+15 V series regulated
3.	MR3 (d.c. output -24 V)	(i)	-24 V unregulated
		(ii)	-15 V zener diode stabilised

The +5 V supply is shunt regulated by VT1 - VT4. Transistors VT1 and VT2 form a differential d.c. amplifier fed from a 8.2 V source stabilised by zener diode MR5. Changes in output voltage are sensed at VT2 base with respect to VT1 base and the output at VT1 collector controls the effective resistance of VT3/VT4. Potentiometer RV1 provides adjustment of the regulated output voltage.

The +15 V supply is series regulated by VT5-VT9. Output voltage changes are sensed at VT8 base with respect to the reference voltage provided by zener diode MR7 at VT8 emitter. Conduction of VT8 varies with output voltage and controls the conduction of series element VT7 via driver VT6. Transistor VT5 provides a constant current source. Over-current protection is provided by VT9 which commences to conduct cutting off VT6 and VT7 when increasing load current causes the voltage drop across R20 to overcome the bias provided for VT9 by R18 and R19. In this way the circuit is protected from high current and short-circuit conditions. Potentiometer RV2 provides adjustment of the regulated output voltage. Socket SKE accepts the temperature controlled 1 MHz master oscillator unit. Output from the unit is taken from pin 7 of SKE and fed via INT/EXT switch SWA to SKC which feeds the exciter circuits. Provision is made to make use of an external 1 MHz frequency standard. With SWA in the EXT (External) position, the external 1 MHz signal connected to SKD is fed out to the exciter circuitry via SKC; R6 provides a 75-ohm termination. Supply to the oscillator is from the +24 V source via SWA so that the oscillator is disabled when an external source is in use. Supply to the temperature control oven is

direct from the -24 V source so that the oscillator is maintained at operating temperature whenever the mains is connected to the exciter.

- End of Part -

PART 4

ALIGNMENT PROCEDURE

1. GENERAL

The alignment procedure described in this Part is operational and where levels quoted cannot be obtained by the controls stated, reference should be made to the relevant sub-section in Part 5, Section 6, "Tests and Adjustments" for setting of other controls on which the correct levels are interdependent.

Unless otherwise mentioned, all voltage levels are measured with a wide-band millivoltmeter e.g. H.P. 411A using the bridging measurement method with a high impedance r.f. probe.

All component circuit references are preceded by a prefix number which consists of the last two figures of the relevant unit or printed circuit board type number e.g. the input pins, 1 and 2, on p.c. board 1R66446 are described as 46(1,2). During alignment it is necessary to extend the relevant unit and remove cover/s where necessary to enable measurements to be taken and for access to preset controls.

The sequence of the alignment procedure is described as follows:

a. VHF Oscillator and Control (Section 2)

b. Signal Path (Section 3)

c. Control Path (Section 4)

2. VHF OSCILLATOR AND CONTROL

2.1 Signal Levels and Frequency Range

Refer Figures 2-3, 2-4, 2-5, 2-6 and 2-7.

(a) Set the synthesiser controls for an output frequency of 20 MHz in the A1 mode with TEST KEY down, the VHF oscillator frequency is then approximately 155 MHz.

(b) Adjust VCO level control 35RV1 on the main VCO board for a maximum level at 37(1,2) then slowly turn anti-clockwise until the level drops below maximum, typically 150 mV r.m.s.

(c) Remove the VCO cable from the VCO module front panel and replace with a 50 Ω coaxial test cable terminated with 50 Ω.

(d) Adjust 37C7, 37C8, 37C12 and 37C14 for maximum VCO splitter control output level measured at the input to the Control Down Mixer on pins 46 (1,2). Change the synthesiser frequency setting if necessary to obtain the maximum level at pins 46(1,2) at these capacitor settings and then readjust 37C8 to set this maximum to 400 mV r.m.s.

(e) Vary the synthesiser frequency over the range 1.6 MHz to 23 MHz and readjust 37C7 for a mean level of 300 mV r.m.s. at the 50 Ω termination

of the test cable, the level at pins 46(1,2) will reduce to approximately 300 mV r.m.s.

(f) Vary the frequency over the range 1.6 MHz to 23 MHz and check that the level variation at pins 46(1,2) and the 50 Ω test cable termination is less than 6 dB.

(g) Replace the original V.C.O. cable.

2.2 Coarse Control

Refer Figures 2-3, 2-4, 2-5, 2-6 and 2-22.

(a) Switch to an output frequency of 20 MHz and connect a d.c. voltmeter between 34C4 on the VHF oscillator housing and the VCO module frame.

(b) Adjust VCO bias control 33RV1 through the front panel access hole in the Phase Comparator Module 1J66453 for a reading of +14 V.

(c) Connect d.c. voltmeter to 36(1,2), set 36RV1 fully clockwise and the synthesiser to 29.99 MHz. Adjust 35C7 for a voltmeter reading of -10 V at this frequency.

(d) Set the synthesiser to 1.6 MHz and adjust 33RV1 for a voltmeter reading of +10 V.

(e) Set the synthesiser to 1 MHz and adjust the frequency limit control, 36RV1, in steps anticlockwise until the synthesiser will not reach 1 MHz but stays less than 1.1 MHz.

2.3 Fine Control

Refer Figure 2-6.

Connect a shorting lead from 36(11) to 36(2).

(a) Connect an oscilloscope, audio or better, to 36(4) and set to a.c. coupled and maximum sensitivity.

(b) Change synthesiser frequency settings and adjust offset control 36RV2 carefully for a null of the sawtooth waveform which appears in the final stage of locking.

(c) Remove the shorting lead from 36(11)/36(2) and check that the total signal swing is approximately 11 V when looking at 22-23-22 MHz and approximately 2 V when looking at 1.6-1.7-1.6 MHz during locking.

3. SIGNAL PATH

3.1 250 kHz Section

Refer Figures 2-23 and 2-24.

The 250 kHz section comprises two printed circuit boards, each mounted on a separate module frame.

(a) The s.s.b. generator module provides emission control and modulation facilities with its carrier frequency of 250 kHz locked to the 1 MHz crystal oscillator via the 2nd i.f. loop module.

(b) The auto attenuator module provides an automatic and a manual mode of system gain control with a "memory" to hold the system gain at operating level during low signal conditions. This module also contains an audio amplifier with front panel switching to interface the s.s.b. generator modulator to the system audio input line or to either or both of two test tone oscillators also on the auto attenuator board.

3.1.1 S.S.B. Generator Module 1J66454 (P.C. Board 1R66439)

Refer Part 3, Section 7 for circuit description

(a) Modulator tests

(i) Set for A3J operation.

(ii) Connect r.f. millivoltmeter to TP14 and earth.

(iii) Feed a 6 kHz audio signal at a level of -20 dBm to SKA33-32.

(iv) Tune 39L2 and 39L3 for maximum indication on millivoltmeter. Typical level is 40 mV at TP14 after adjustment as in 3.1.1(a) (vi) below.
Note: Because of the tight coupling between 39L2 and 39L3, a frequency of at least 6 kHz is required to ensure accurate and symmetrical tuning.

(v) Connect millivoltmeter to TP18 and adjust 39RV2 for approximately 500 mV r.m.s.

(vi) Remove the audio signal and adjust 39RV1 and 39C3 for minimum carrier leak output at TP18. It may be necessary to link either TP10 to TP11 or TP12 to TP13 to bring this level below 5 mV r.m.s. For more precise adjustments, a selective millivoltmeter or a spectrum analyser should be connected to the output of the s.s.b. generator.

(vii) Reconnect audio signal and check the frequency response by varying the audio frequency from 200 Hz to 3 kHz. The response should be flat within ±0.1 dB.

(b) Level Adjustment.

(i) Set for A1 operation.

(ii) Set 54SWA on the module front panel to the 0 dB position and adjust 39RV10 for 0 dB indication on front panel meter 54M1 corresponding to 200 mV r.m.s. at 39PLA13-14.

(iii) Set for A3A operation and 55SWA to OFF position.

(iv) Set 54SWA to -10 dB position and adjust 39RV12 for -6 dB indication on 54M1 corresponding to 32 mV r.m.s. at 39PLA13-14.

(c) Modulator gain

(i) Set for A3J operation.

(ii) Feed a 1.4 kHz audio signal at a level of -20 dBm to SKA33-32.

(iii) Measure the output at SKA13-17, and adjust 39RV2 for 200 mV r.m.s. output.

(d) Carrier Levels

(i) Connect r.f. millivoltmeter to SKA13-17.

(ii) Set for TUNE operation and adjust 39RV4 for 160 mV r.m.s. output (-2 dB).

(iii) Set for A1 operation and adjust 39RV5 for 200 mV output (0 dB).

(iv) Set for A3 operation and adjust 39RV6 for 100 mV output (-6 dB).

(v) Set for A3H operation and adjust 39RV7 for 100 mV output (-6 dB).

(vi) Set for A3A operation and adjust 39RV8 for 32 mV output (-16 dB).

3.1.2 Auto Attenuator Module 1J66455 (P.C. Board 1R66440)

Refer Part 3, Section 6 for circuit description.

Set the exciter for A1 operation and check that the level at PLA(33,32) is 200 mV r.m.s. at 250 kHz corresponding to 0 dB on s.s.b. generator meter 54M1.

(a) Attenuator amplifier

(i) Set 55SWB on the module front panel to MANUAL.

(ii) Measure the level at PLA(25,26) terminated with 50 Ω or at the cable to the 2nd i.f. mixer as it is correctly terminated when connected.

(iii) Adjust R.F. GAIN control 55RV7, on the module front panel, and tune 40TR1 for a maximum to obtain a 75 mV r.m.s. output.

(b) Auto attenuator preset

(i) Connect a shorting link between PLA31 and PLA34.

(ii) Set 55RV7 to obtain 75 mV r.m.s. output at PLA(25,26) with 55SWB set to MANUAL.

(iii) Adjust 40RV6 until switching MANUAL-AUTO-MANUAL does not appreciably change the level at PLA(25,26) then leave 55SWB in AUTO position.

(iv) Remove shorting link between PLA31 and PLA34.

(v) Check that the level at PLA(25,26) rises to more than 300 mV r.m.s. in the absence of a feedback signal from the transmitter to PLA(11) i.e. with the transmitter H.T. switched off.

(vi) The foregoing is an approximate setting and should be readjusted in conjunction with the ATS-1 transmitter in the automatic gain mode for a minimum hand-keyed c.w. waveform overshoot.
The transmitter output waveform may be observed by connecting an oscilloscope to the R.F. MONITOR connector, 1SKB, located in the r.f. amplifier assembly.

(c) Manual range

(i) Set 55SWB to MANUAL

(ii) Measure the level at 40PLA(25,26) terminated with 50 Ω or the cable to the 2nd i.f. mixer.

(iii) Check that the range of the R.F. GAIN control, 55RV7, is greater than 30 mV r.m.s. to 300 mV r.m.s.

(d) Reference amplifier

(i) Check that the level at 40PLA(33,32) is 200 mV r.m.s.

(ii) Tune 40L3 to obtain 3.1 V r.m.s. at 40(27).

(e) Output limit

(i) Set 55SWB to MANUAL and 55RV7 fully clockwise.

(ii) Apply 2.5 V d.c. to 40PLA17 and adjust 40RV5 for approximately 150 mV r.m.s. at 40PLA(25,26) terminated with 50 Ω or the cable to the 2nd i.f. mixer.

(iii) The foregoing is an approximate setting and should be readjusted in conjunction with the ATS-1 transmitter to limit the exciter output level, i.e. the level at 40PLA(25,26), to that giving a scale reading of 55% f.s.d. on the transmitter multimeter (4M1) in the EXCITER OUTPUT position, during the coarse tuning mode.

(f) Audio amplifier

(i) Set for A3J operation and 55SWA to LINE.

(ii) Apply the peak line level used for 1 kW transmitter output, nominally 4 dBm (600 Ω), to the audio input line 40PLA(1,2) or via 57PLA(31,32) or to the system audio input.

(iii) Set 55RV1 for a level of -20 dBm at 40 PLA(6,5) terminated with 600 Ω or the cable to the s.s.b. generator. This corresponds to a level of 0 dB on the s.s.b. generator meter 54M1.

(g) Test tone oscillators

(i) Set 55SWA to F1.

(ii) Adjust 40RV2 to obtain 5 V p-p (1.7 V r.m.s.) at 40(35).

(iii) Set 55SWA to F2.

(iv) Adjust 40RV3 to obtain 5 V p-p (1.7 V r.m.s.) at 40(36).

(v) With 55RV1 set as in 3.1.2(f) above, set 40RV8 and then 40RV9 for the required system test levels. Nominally set each tone for a -6 dB reading on the s.s.b. generator meter, 54M1, which corresponds to -26 dBm at 40PLA(6,5), then switching to F1/F2 will give the 1 kW p.e.p. level from the 250 kHz section.

3.2 10.45 MHz and 10.7 MHz Section

Refer Figures 2-12, 2-13 and 2-14.

3.2.1 Frequency Translator Module 1J66464

This section of the signal path consists of three of the eight p.c. boards mounted in the frequency translator module and they are as follows:

10.45 MHz V.C.O. Board 1R66442
2nd I.F. Mixer Board 1R66443
2nd I.F. Amplifier Board 1R66444

The 10.45 MHz VCO board provides a frequency locked injection signal to mix in the 2nd i.f. mixer with the 250 kHz signal from the auto attenuator module. The resultant 10.7 MHz product is amplified and passed through a sideband filter in the 2nd i.f. amplifier.

(a) 10.45 MHz V.C.O. Board 1R66442

Refer Part 3, Sub-section 2.3 for circuit description.

The frequency of the 10.45 MHz VCO is varied by the 1 kHz and 100 Hz digits selected in the programmed frequency and is equal to 10.45 MHz minus M.N. kHz, where M is the kHz digit selected and N the 100 Hz digit (refer to operation of the 2nd I.F. Loop Module 1J66451 in Part 3, Section 3).

The 10.45 MHz VCO board does not have any preset controls but 42L1 and 42L2 are tuned for a maximum, typical values being 900 mV r.m.s. at 42(1,2) and 2.4 V r.m.s. at 42(12,13).

(b) 2nd I.F. Mixer Board 1R66443

Refer Part 3, Sub-section 2.4 for circuit description.

This board consists of a 10.45 MHz injection amplifier, with 43L2 tuned for a maximum level at pins 43B and 43C, and a balanced modulator.

Inductor 43L3 is tuned for a maximum 10.7 MHz level at 43(7,8) and at these pins the 10.45 MHz level should be less than 7 mV r.m.s. If necessary, link A to B or A to C and adjust 43C2 for a minimum 10.45 MHz level at 43(7,8). Typical operating levels are 40 mV r.m.s. for 10.7 MHz at 43(7,8) and 80 mV r.m.s. for 250 kHz at 43(1,2) when set in the A1 mode.

(c) 2nd I.F. Amplifier Board 1R66444

Refer Part 3, Sub-section 2.5 for circuit description.

This board consists of a 10.45 MHz notch filter, a 10.7 MHz amplifier with a sideband crystal filter and an output network to give a balanced feed to the Signal Up-Mixer Board 1R66448 in the V.H.F. section.

Inductors 44L2 and 44L3 are tuned for a maximum 10.7 MHz level at 44(6,5) and 44L4 for a minimum 10.45 MHz level across 44R6 which should be at least 30 dB below the 10.7 MHz level at this test point.

With the board terminated by 50 Ω coaxial cables to the signal up-mixer board and with the 123.1 MHz injection drive connected to the mixer diodes on that board, typical operating levels are 80 mV r.m.s. for 10.7 MHz at 44(6,5) or 44(4,5) and 40 mV r.m.s. for 10.7 MHz at 44(3,2) when set in the A1 mode.

3.3 V.H.F. Section

This section of the signal path consists of the 123 MHz Filter Board 1R66466, Signal Up-Mixer Board 1R66448 and Signal Down-Mixer Board 1R66449 which are mounted in Frequency Translator Module 1J66464.

The 10.7 MHz signal is raised to the VHF i.f. frequency of 133.8 MHz by mixing it on the signal up-mixer board with the 123.1 MHz signal fed, via the 123 MHz band pass filter board, from the Control Up-Mixer Board 1R66445 in V.C.O. Module 1J66463.

The 133.8 MHz signal is then lowered to the HF output frequency range by mixing it on the signal down-mixer board with the VHF oscillator frequency in the range 135.4 MHz to 163.79 MHz.

3.3.1 123 MHz Filter Board 1R66446

Refer Part 3, Sub-section 2.9 for circuit description, and to Figure 2-18.

There is an approximate 10 dB loss in the 123 MHz filter board.

(a) Set for A1 operation, connect r.f. millivoltmeter to 66(1,2) and check for an input level of typically 1 V r.m.s.

(b) Connect r.f. millivoltmeter to 66(3,4) and adjust 66C2, 66C3 and 66C4 for maximum 123.1 MHz signal level.

3.3.2 Signal Up-Mixer Board 1R66448

Refer Part 3, Sub-section 2.6 for circuit description and to Figure 2-15.

(a) Set for A1 operation.

(b) Connect a spectrum analyser to 48(9,10) via a high impedance probe (much greater than 50 Ω) or remove the cable from 48(9,10) and feed the signal directly to the 50 Ω input of the spectrum analyser.

(c) Check that the 123.1 MHz level is typically 300 mV but is greater than 50 mV bridging at 48(1,2).

(d) Adjust 48C14, 48C16, 48C22 and 48C23 for a maximum 133.8 MHz signal level at 48(9,10) a typical level being 45 mV r.m.s. A typical level for the 10.7 MHz signal is 120 mV r.m.s. at 48(5,4) or at 48(6,4) with the 123.1 MHz cable removed from 64SKA. The 123.1 MHz level should be at least 20 dB below the 133.8 MHz level at 48(9,10).

Note: If only one of the variable capacitors in 3.3.2(d) above needs to be readjusted, or a check adjustment only is required, the correct alignment may be obtained by setting the capacitors for a peak in the H.F. output signal from the exciter, eliminating the necessity for a spectrum analyser.

3.3.3 Signal Down-Mixer Board 1R66449

Refer Part 3 Sub-section 2.7 for circuit description, and to Figure 2-16.

(a) Set for A1 operation.

(b) Connect a spectrum analyser to the junction of 49R11 and 49R12 via a high impedance probe and set to view 123.1 MHz and 133.8 MHz.

(c) Tune 49L3 for a minimum 123.1 MHz level on the analyser and 49L4 for a maximum 133.8 MHz.

(d) Check over the exciter frequency range for a typical level of 300 mV r.m.s., but greater than 50 mV r.m.s., at 49(1,2).

(e) Set the exciter frequency to 29.99 MHz and adjust 49C14, 49C16, 49L6 and 49L7 for a maximum level at 49(10,9). Tune 49L6 and 49L7 so that the level just starts to decrease.

(f) Set the exciter frequency to 23 MHz. Typical operating levels are 50 mV r.m.s. of 133.8 MHz signal measured at 49(5,6) and 30 mV r.m.s. of 23 MHz signal at 49(10,9).

3.4 H.F. Output Section

Refer Figure 2-17.

3.4.1 Wideband Amplifier Board 2R66450

Refer Part 3, Sub-section 2.8 for circuit description.

The output section of the exciter consists of the wideband amplifier board which is mounted in the Frequency Translator Module 1J66464. It has no preset adjustments or tuning requirements.

The operating level is typically 1 V r.m.s. at 50(5,6) for 30 mV r.m.s. at 50(1,2). From 1.6 MHz to 29.99 MHz the output variation should be less than 4 dB.

4. CONTROL PATH

4.1 10.7 MHz Section

Refer Figures 2-9a and 2-11.

The 10.7 MHz section of the control path consists of the following:

10.7 MHz V.C.O. Board 1R66438 (Frequency Translator Module 1J66464)
Low Pass Filter Board 1R66467 (V.C.O. Module 1J66463)

4.1.1 10.7 MHz V.C.O. Board 1R66438

Refer Part 3, Sub-section 2.2 for circuit description.

(a) Connect a d.c. voltmeter between 38(4) and frame and adjust 38C6 for approximately -8 V.

(b) Connect a frequency counter to 38(14,15) and check that the 10.7 MHz VCO is "locked".

(c) Tune 38L4 and 38L7 for maximum and check that the 10.7 MHz level at 38(6,7) is approximately 175 V r.m.s. and at 38(14,15) approximately 900 mV r.m.s.

4.1.2 Low Pass Filter Board 1R66467

Refer Part 3, Sub-section 1.7 for circuit description.

(a) Tune inductor 67L1 until the 10.7 MHz level at 67(4,3) just starts to drop from maximum. Typical 10.7 MHz loss 67(1,2) to 67(4,3) is 0.3 dB.

4.2 V.H.F. Section

Refer Figures 2-3, 2-8 and 2-9.

The V.H.F. section of the control path consists of the following boards mounted in V.C.O. Module 1J66463:

Control Up-Mixer Board 1R66445
Control Down-Mixer Board 1R66446

4.2.1 Control Up-Mixer Board 1R66445

Refer Part 3, Sub-section 1.5 for circuit description.

(a) Set the synthesiser for an output frequency of 10 MHz and check that the 123.1 MHz cable from the frequency translator module to the VCO module is connected.

(b) Measure the level at 45(2,3) and tune 45L2, 45L4 and 45C11 for a maximum, typically 1 V r.m.s.

(c) Connect a spectrum analyser to 45(9,8) via a high impedance probe and set to view 123.1 MHz and 133.8 MHz.

(d) Tune 45TR1, 45C19 and 45C28 for a maximum 133.8 MHz level, typically 200 mV r.m.s. at 45(9,8) for 300 mV r.m.s. of 10.7 MHz signal at 45 (7,6).

Note: At 45(9,8) the 123.1 MHz component is approximately 12 dB below the required 133.8 MHz and hence a spectrum analyser level reading

of 200 mV r.m.s. for 133.8 MHz would be equivalent to a 300 mV r.m.s. reading on a wideband millivoltmeter.

4.2.2 Control Down-Mixer Board 1R66446

Refer Part 3, Sub-section 1.6 for circuit description.

(a) Check that the level at 46(1,2) is typically 300 mV r.m.s.

(b) Measure the control output level at 46(11,12) and adjust 46C9 and 46C11 for a maximum reading, typically 2.4 V r.m.s. for 300 mV r.m.s. of 133.8 MHz signal at 46(6,7).

(c) Vary the synthesiser frequency from 1.6 MHz to 29.99 MHz and the level at 46(11,12) should remain greater than 0.7 V r.m.s.

4.3 Logic Section

Refer Figures 2-2, 2-20, 2-22.

The logic section of the control path consists of the following:

Pulse Swallower Module 1J66452
Phase Comparator Module 1J66453.

Refer to Part 3, Sections 4 and 5 respectively for circuit description of the modules.

As there are no preset controls or adjustments on the modules, the following checks are made to verify correct operation of major functions.

4.3.1 Coarse Control Voltage Range

Set the synthesiser to 1.6 MHz and measure the level at 18SKE(2) or 36(5) with a d.c. voltmeter. Check that the reading is approximately +15 V. Set the synthesiser to 29.99 MHz and check that the reading is approximately 0 V.

4.3.2 Programmable Divider Drive Level

Measure the level at 18SKD(31,30) and check that it is greater than 0.6 V r.m.s. at all output frequency settings of the exciter.

4.3.3 Programmable Divider Output

Set the exciter to 15 MHz and check for approximately 50 ns +ve TTL logic pulses at 18SKD19 at a "locked" frequency of 1 MHz.

Set the exciter to 5 MHz and check for the same pulses at a locked frequency of 500 kHz after approximately 5 seconds.

The reference signal at 18SKD20 should be of the same frequency as that at 18SKD19 but of 50 ns -ve pulses.

4.3.4 1 MHz Standard Reference

The signal at 18SKD21 is a TTL logic pulse representation of the exciter 1 MHz standard internal oscillator or external reference and remains locked at 1 MHz independent of the exciter frequency setting.

- End of Part -

PART 5

MAINTENANCE AND REPAIR

1. GENERAL

Maximum utilisation of the exciter can be achieved only when unserviceable elements are restored to a serviceable state with the minimum of delay. This is best achieved by having on hand a complete set of tested spare modules for immediate replacement: faulty modules can then be repaired without increasing transmitter "down-time".

A thorough understanding of solid-state devices and logic techniques is essential for effective maintenance.

The circuitry in the exciter is completely solid state: advanced design techniques ensure a high degree of stability and eliminate the need for operational adjustments. Routine maintenance is confined to keeping the unit clean and free of dust, and ensuring that nothing impedes the flow of cooling air upwards through the unit.

Access to the plug-in modules of the exciter is gained by opening the hinged cover on the transmitter immediately below the control panel. To remove a module, first detach the retaining bar from the front of the modules and then withdraw the module by grasping the knurled knob on the lower part of the front panel. All modules with the exception of the power supply can be extended clear of the transmitter cabinet using the Service Tray 1R66458 which then gives access to both sides of the extended module. The power supply module can be withdrawn without disconnection only far enough to enable access to the internal connector and to the 1 MHz master oscillator: DO NOT ATTEMPT TO WITHDRAW THE POWER SUPPLY MODULE ANY FURTHER WITHOUT DISCONNECTING THE INTERNAL CONNECTOR OR THE ASSOCIATED WIRING WILL BE DAMAGED. The power supply module can be operated on the bench by connecting mains supply to the front panel MAINS connector; the connections are as follows:

1 2	MAINS - 240 V 50 Hz
3	EARTH
4	EARTH

Before removing or replacing modules, ensure that the a.c. mains supply is disconnected from the exciter so that damage to semiconductor devices will not be caused by voltage transients.

2. REPLACEMENT OF MOSFET DEVICES

MOSFET devices, because of their insulated gate construction, have a high impedance and low capacitance in the gate area, and can easily be damaged by electrostatic charges built up during handling. The use of carbon element

soldering irons is not recommended for the servicing of any transistorised circuits as any a.c. leakage may cause permanent damage. If it becomes necessary to replace one of these devices, the following procedure should be followed to avoid damage to the replacement device.

1. Using a small solder-removing tool, remove as much solder as possible from the four leads of the original component.

2. Straighten the four leads by careful use of a low voltage soldering iron which has a sharp tip. Using a pair of miniature side-cutters trim the leads as close as possible to the board, withdraw the old transistor from the board.

3. The new transistor will normally be supplied with an eyelet or similar device connecting together the four leads. Before removing the eyelet, wrap several turns of 5 amp fuse wire around the leads as near as possible to the case.

4. Slide the eyelet from the leads and pass the leads through the spacer and the board ensuring that the leads remain connected together. Twist the ends of the leads together and remove the fuse wire.

5. Solder the leads into position and trim off the twisted ends.

3. REMOVAL OF INTEGRATED CIRCUITS

The following procedure is recommended to minimise damage to printed circuit cards during removal of integrated circuits.

a. Circuits having circular pin arrangement

1. Using a small solder-removing tool, remove as much solder as possible from the leads.

2. Straighten the leads by careful use of a low voltage soldering iron which has a sharp tip. Using a pair of miniature side cutters, trim the leads as close as possible to the board.

3. Using a soldering iron with a tip large enough to cover all leads simultaneously, apply just sufficient heat to allow the circuit to be withdrawn from the board.

4. Before inserting the new circuit, ensure that all holes are free from solder.

b. Circuits having in-line pin arrangement

1. Using a pair of miniature side cutters trim the pins <u>above</u> the board as close as possible to the body, remove the body of the circuit.

2. Clamp the board in a vice and remove each pin in turn using a small solder removing tool and gripping the cut end of the pin with a pair of long-nose pliers.

4. FERRITE BEADS

Ferrite suppression beads are used on some leads in the VCO and frequency translator modules for prevention of parasitic oscillations which may occur from spurious feedback. Care should be taken to ensure that the beads are not mislaid or damaged during servicing and that they are replaced.

5. FAULT LOCATION

To facilitate rapid location of a faulty module, a series of fault location flow charts have been included in this handbook as Figs. 2-26 and 2-27. In producing these flow charts it has been assumed that a complete set of spare tested modules is available along with the Service Tray 1R66458. A cathode-ray oscilloscope, a frequency counter and a multimeter may also be needed (refer to Chapter 1, Part 1, Section 13 for recommended types). To aid in the use of the flow charts some of the words used are defined below:

Extend: Withdraw the module concerned and place it on the service tray.

CAUTION: The service tray has no coding arrangement. Ensure that the service tray is placed in the correct sub-rack position for the module concerned.

Re-fit: Return the previously extended module to its correct sub-rack position,

OR

Replace the original module after substitution.

Faulty: The module concerned is faulty: fit a tested spare and mark the original module for repair.

Substitute: Fit a tested spare in place of the original module. Do not consider the original module to be faulty at this stage.

Was Faulty: As the result of a substitution the original module is shown to be faulty; leave the spare in position and mark the original module for repair.

In the flow charts only two basic fault conditions have been considered; those of incorrect frequency and loss of output. Faults involving the auto attenuator and s.s.b. generator modules have not been considered. For problems in the audio circuits, the auto attenuator module is quickly checked by extending, selecting test tones and checking output at pin 6. Problems in the generation of the selected emission mode, for example, excessive or insufficient carrier level, presence of unwanted sideband, spurious emission, are usually due to faults in the s.s.b. generator which is best checked by substitution.

6. TEST AND ADJUSTMENT PROCEDURE

6.1 General

A detailed description of the function and operation of each module and board is given in Part 3 of this chapter. However, a brief resume of the function of each is given as an introduction in each of the test and adjustment procedures which follow in Sections 7 to 11 below to provide a quick reference as to the purpose of the adjustments.

To facilitate fault tracing it is necessary to first check circuit voltages; for that reason a voltage analysis table comprises the second sub-section in each section below. Where external power supplies are connected for voltage analysis they should remain connected for the test and adjustment procedure which follows.

References are made to pin numbers in the text and refer to the test point pins which are located at various points on the p.c. board. The pin number is printed on the board adjacent to the pin.

The components in the following modules are set, no adjustments are necessary.

2nd I.F. Loop Module 1J66451
Pulse Swallower Module 1J66452
Phase Comparator Module 1J66453

For d.c. voltage analysis for transistors and integrated circuits refer to Figures 2-19, 2-20 and 2-22 respectively.

Figure 2-28 shows the test set-up for those modules and boards which cannot be simply described in the text.

7. POWER SUPPLY MODULE 1H66430

Refer Part 3, Section 8 for circuit description.

7.1 Power Supply Board 1R66456

7.1.1 Function

The power supply module provides the d.c. supply voltages for all modules in the exciter; it also houses the internal 1 MHz reference frequency crystal oscillator unit.

It is operated from a single phase 240 V a.c. mains supply and provides the following d.c. voltages:

+5 V	shunt regulated
+24 V	unregulated
+15 V	series regulated
-24 V	unregulated
-15 V	zener diode stabilised

During tests and adjustments on the bench the 1 MHz crystal oscillator unit should be removed from the module.

7.1.2 Preliminary voltage check

(a) Before connecting the a.c. mains supply check with a multimeter (ohms) that there is no continuity between earth and 30SKA1, 30SKA2, 30SKB1, 30SKB4, 30SKB5, 30SKB7 and 30SKB11.

(b) Connect the module to the a.c. mains supply and with the multimeter check for the following d.c. voltages with respect to earth:

+5 V at	30SKB1
+24 V at	30SKB4
+15 V at	30SKB5
-24 V at	30SKB7
-15 V at	30SKB11

Note that these voltages are approximate.

(c) Switch off the unit and reconnect to the mains supply via a variac.

7.1.3 Tests and adjustments

(a) +5 V supply

(i) Connect a 3.3 Ω 10 W test load resistor between 30SKB1 and 30SKB9.

(ii) Set the variac to 240 V and switch on the mains supply.

(iii) Turn 30RV1 fully anticlockwise and then fully clockwise and measure the voltage at 30SKB1 for each extreme. The voltages should be approximately +4 V and +6 V respectively.

(iv) Adjust 30RV1 until the voltage at 30SKB1 is +5 V.

(v) Reduce the mains voltage to 216 V and then increase to 264 V. The voltage at 30SKB1 should not change at either mains input.

(vi) Set the mains voltage to 240 V and measure the ripple at 30SKB1. It should be less than 50 mV p-p.

(vii) Switch off mains supply, remove 3.3 Ω load resistor and switch mains on again.

(viii) Measure the voltage at 30SKB1. It should not have changed from the +5 V as set in (iv) above.

(ix) Switch off mains supply.

(b) +15 V supply

(i) Connect a 33 Ω 10 W test load resistor between 30SKB5 and 30SKB9.

(ii) Set variac to 240 V and switch on the mains supply.

(iii) Turn 30RV2 fully anticlockwise and then fully clockwise and measure the voltage at 30SKB5 for each extreme. The voltages should be approximately +12.5 V and +16.5 V respectively.

(iv) Adjust 30RV2 until the voltage at 30SKB5 is +15 V.

(v) Reduce the mains voltage to 216 V and then increase to 264 V. The voltage at 30SKB5 should not change at either mains input.

(vi) Set the mains voltage to 240 V and measure the ripple at 30SKB5. It should be less than 10 mV p-p.

(vii) Switch off mains supply, remove 33 Ω load resistor and switch mains on again.

(viii) Measure the voltage at 30SKB5. It should not have changed from the +15 V as set in (iv) above.

(ix) Switch off mains supply.

(c) -15 V supply

(i) Connect a 220 Ω, 2 W or more, test load resistor between 30SKB11 and 30SKB9.

(ii) Set the variac to 240 V and switch on the mains supply.

(iii) Measure the voltage at 30SKB11. It should be approximately -15 V.

(iv) Measure the ripple at 30SKB11. It should be less than 30 mV p-p.

(v) Switch off mains supply and remove 220 Ω load resistor.

(d) ±24 V supplies

(i) Set the variac to 240 V and switch on the mains supply.

(ii) Measure the voltage at 30SKB4. It should be approximately +24 V.

(iii) Measure the ripple at 30SKB4. It should be approximately 1 V p-p.

(iv) Measure the voltage at 30SKB7. It should be approximately -24 V.

(v) Measure the ripple at 30SKB7. It should be approximately 1 V p-p.

(vi) Switch off mains supply. Disconnect variac and replace 1 MHz crystal oscillator unit in its octal socket.

7.2 1 MHz Crystal Oscillator

7.2.1 Function

The 1 MHz Crystal Oscillator, Marconi type F3125-01 is an octal based plug-in unit mounted in Power Supply Module 1H66430.

Its function is to provide the standard reference frequency for the phase comparator module and the divide by four frequency of 250 kHz for the s.s.b. generator carrier frequency.

The crystal unit and its integrated silicon transistor oscillator circuit are totally enclosed within a proportional control oven and finally fitted into a compact metal container. Frequency change from the BT cut crystal due to aging is less than +5 in 10⁸/month.

The r.f. output is taken from pin 7 of 30SKE via the INT/EXT toggle switch 30SWA to coaxial connector 30SKC.

To compensate for up to 10 years crystal aging, frequency adjustment can be made by setting of the coarse and fine trimmers accessible through two holes in the side of the oscillator case. The range of adjustment by the trimmers is:

Coarse: 48 parts in 10^7

Fine: 2 parts in 10^7

7.2.2 Voltage analysis

Voltages and connections to 30SKE are as follows:

Pin	Connection
1	+24 V d.c. oven supply
2	+24 V d.c. oscillator supply
3	-24 V d.c. oven supply
4	Oscillator d.c. negative supply and r.f. earth
5	Blank
6	Blank
7	R.F. output, typically 3 V p-p into 1 kΩ
8	Earth

7.2.3 Tests and adjustments

No adjustments should be made on the oscillator unless it has been operating for a period of not less than 3 hours and a frequency standard is available for calibration of test equipment.

(a) Frequency adjustment

(i) Set for A1 (C.W.) operation at a high frequency which is an exact multiple of 1 MHz e.g. 20 MHz to increase any observed oscillator error by a factor of 20.

(ii) Connect frequency counter to R.F. MONITOR connector 1SKB located in the main transmitter r.f. amplifier assembly and check the output frequency using a counter time base of 10 seconds or more. If necessary adjust the fine trimmer in the oscillator to obtain the exact frequency as set using a non metallic adjusting tool.

(iii) If the exact frequency cannot be obtained, i.e. it is outside the range of the fine trimmer, it will be necessary to readjust the coarse trimmer slightly and then the fine trimmer.

(iv) The short term frequency stability over a period of one second is as follows:

With constant ambient temperature and supply voltage - less than ±5 in 10^9

With temperature variation -20 °C to +55 °C and constant supply voltage - less than ±1.5 in 10^8

With constant ambient temperature and ±10% supply voltage variation - less than ±5 in 10^9

8. V.C.O. MODULE 1J66463

8.1 V.H.F. Oscillator 1R66465 and Main V.C.O. Board 2R66435

Refer Alignment Procedure Part 4, Section 2, Figures 2-4 and 2-5 and Test Set-up, Figure 2-28(D).

8.1.1 Function

The VHF oscillator and the main VCO board are part of the VCO module. Together they provide a voltage controlled oscillator operating in the frequency range 130 MHz to 165 MHz and consists of the following:

(a) VHF oscillator proper

(b) Input compensating network

(c) Output amplifier and

(d) +15 V regulated power supply

The VHF oscillator is the complete board and housing. The frequency varies proportionally with the differential voltage at pins 1 and 2 (positive) on the board.

8.1.2 Voltage analysis

(a) Two power supplies are required, 10 V and 20 V, connected as shown in Figure 2-28(D).

(b) Connect the multimeter to the case earth pin as negative reference.

(i) Check that the voltage at pin 6 of 35MN1 is +15 V ±0.4 V.

(ii) Typical transistor terminal voltages are as follows:

	c	b	e
35VT1	+11 V	+1.8 V	+1.2 V
35VT2	+15 V	+1.7 V	+1 V

Note: The voltages for oscillator 35VT1 depend on the oscillatory state and hence will vary from those given above which are typical for a maximum output setting of 35RV1.

8.1.3 Tests and adjustments

Connect power supplies, frequency counter via BNC "T" adaptor and resistors as shown in Figure 2-28(D).

Note: When checking levels disconnect the frequency counter from the BNC "T" adaptor to obtain accurate readings.

(a) Frequency and output level

(i) Set 35C7, RVY and RVZ to mid-range and connect millivoltmeter across the 50 Ω termination at the BNC "T" adaptor.

(ii) Adjust 35RV1 for a maximum millivoltmeter reading and then turn slowly anticlockwise until the reading just starts to decrease, typically 200 mV r.m.s.

(b) Coarse control check

(i) Connect multimeter between pins 4 and 1 (negative) and set RVY for a reading of 24 V.

(ii) Adjust 35C7 for an output frequency of 164 MHz. 35C7 should be at least two complete turns from the top.

(iii) Set RVY for an output frequency of 135.4 MHz, check that the multimeter reads 4 V ±1 V.

(iv) Turn RVY through its range and check that the output level and frequency vary smoothly with approximately a 6 dB drop from 135.4 MHz to 164 MHz.

(c) Fine control check

(i) Set RVY for an output frequency of approximately 135 MHz.

(ii) Adjust RVZ over its full range and check that the output frequency varies smoothly with a maximum value when RVZ is fully clockwise. The total frequency change should be 100 kHz ±10 kHz.

(iii) Disconnect all test equipment.

8.2 V.C.O. Control Board 1R66436

Refer Circuit Description Part 3, Sub-section 1.3, Figure 2-6 and Test Set-up, Figure 2-28(E).

8.2.1 Function

The VCO control board is part of the VCO module and contains the gain compensating amplifiers for the coarse and fine control loops of the VHF oscillator. It also contains +15 V and -15 V voltage regulators to supply the amplifiers.

The coarse amplifier, 36MN3, is a d.c. amplifier with non-linear feedback to reduce the gain with its increasing positive output.

The fine amplifier, 36MN4, has a multiplying function to give an output which is level dependent on the fine input signal at one input and on the d.c. voltage from the coarse amplifier output on its other input.

8.2.2 Voltage analysis

Connect the two 24 V power supplies as in Figure 2-28(E).

(a) D.C. voltages from regulator

(i) Check that voltages at 36MN3 pin 7, 36MN4 pin 15 and board pin 6 are all +15 V ±0.4 V referred to earth.

(ii) Check that voltages at 36MN3 pin 4, 36MN4 pin 5 and board pin 9 are all -15 V ±0.4 V referred to earth.

(iii) Vary the +24 V and -24 V power supplies by ±4 V and check that the +15 V measured at pin 6 and the -15 V at pin 9 do not change.

8.2.3 Tests and adjustments

(a) Coarse control range

Refer Alignment Procedure Part 4, Sub-section 2.2.

In the following tests all d.c. voltages are measured with respect to pin 2 (earth).

(i) Connect the 10 kΩ, 1/4 W linear potentiometer (RVA) to pins 6 and 2, refer Figure 2-28(E), but do not connect the moving arm to pin 5 at this stage.

(ii) Measure the voltage at pin 1, typically -13 V.

(iii) Connect RVA moving arm to pin 5 and check that the voltage measured at pin 1 is approximately +10 V when the voltage at pin 5 is +14 V (set by RVA).

(iv) Vary 36RV1 through its range and check that the voltage measured at pin 1 varies approximately 0.5 V about the +10 V position.

(v) By adjusting RVA in small steps, check that the incremental gain about the +10 V point at pin 1 is approximately six times less than that about the -10 V point at pin 1.

$$\text{i.e. Incremental Gain} = \frac{\text{Pin 1 reading 1 - Pin 1 reading 2}}{\text{Pin 5 reading 1 - Pin 5 reading 2}}$$

(b) Fine gain control

Refer Alignment Procedure Part 4, Sub-section 2.3.

In the following tests all d.c. voltages are measured with respect to pin 2 (earth).

(i) Disconnect RVA and check that the voltage measured at pin 11 is approximately -14 V.

(ii) Connect c.r.o. to pins 4 and 2 (common) and set a.c. input sensitivity to maximum.

(iii) Connect A/F signal generator to pins 3 and 2(common) and a shorting link between pins 11 and 2.

(iv) Set audio generator for a 1 kHz output at a level of 1 V r.m.s. measured at pin 3.

(v) Adjust 36RV2 for a null in the output waveform, typically less than 10 mV p-p. Remove shorting link from pins 11-2 and check that the output rises to approximately 9.5 V p-p (3.4 V r.m.s.).

(vi) Reconnect RVA, refer Figure 2-28(E), and set for +10 V measured at pin 1. The voltage measured at pin 11 should be approximately -2 V and the output at pin 4 should be approximately 1.5 V p-p.

(vii) Disconnect RVA and all test equipment.

8.3 V.C.O. Splitter Board 1R66437

Refer Figure 2-7.

8.3.1 Function

The VCO splitter board is part of the VCO module and consists of three 135 MHz - 165 MHz amplifiers to provide two outputs, isolated from each other, from the one input, which is the signal from V.H.F. Oscillator 1R66465.

8.3.2 Voltage analysis

(a) Connect the +15 V power supply to the board, positive to pins 3 and 6 and negative to pin 5 (common).

(b) Using the multimeter measure the transistor terminal voltages, referred to pin 5. Typical readings are:

	c	b	e
37VT1	+15 V	+4.8 V	+4.1 V
	d	s	g
37VT2(FET)	+15 V	+0.5 V	0 V
37VT3(FET)	+15 V	+0.5 V	0V

8.3.3 Tests and adjustments

(a) Gain and frequency response

(i) Connect a 50 Ω, 1/4 W resistor between pins 4 and 5 (common) and another between pins 7 and 8 (common).

(ii) Connect signal generator output to pins 1 and 2 (common) via a 50 Ω cable and set the frequency to approximately 155 MHz at a level of 150 mV r.m.s. measured at pins 1 and 2.

(iii) Connect the r.f. millivoltmeter to pins 7 and 8 and adjust 37C14, 37C12, 37C8 and 37C7, in that order, for a maximum reading. Readjust 37C8 to reduce this level to 300 mV r.m.s.

(iv) Connect the millivoltmeter to pins 4 and 5 and readjust 37C7 so that the level measured at pins 4 and 5 is 300 mV r.m.s. average for

input frequencies in the range 135 MHz to 165 MHz.

(v) Check that the output variation at pins 4-5 and at 7-8 is less than 6 dB over the input frequency range 135 MHz - 165 MHz.

Note: 1. Capacitors 37C7, 37C8, 37C12 and 37C14 may have to be re-adjusted when replaced and operating in the VCO module to take into account a possible non-constant input level versus frequency from the VHF oscillator and changes in stray capacitances.

8.4 Control Up-Mixer Board 1R66445

Refer Alignment Procedure Part 4, Sub-section 4.2.1 and Figure 2-8.

8.4.1 Function

The control up-mixer board is part of the VCO module and is a 10.7 MHz to 133.8 MHz up frequency mixer. It consists of the following:

(a) A 61.55 MHz crystal oscillator and doubler stage

(b) A 123.1 MHz injection amplifier to drive the mixer diodes

(c) A 133.8 MHz bandpass filter after the mixer diodes and

(d) A tuned 10.7 MHz input transformer.

8.4.2 Voltage analysis

(a) Connect the +15 V power supply to the board, positive to pins 5 and 10 and negative to pin 3 (common).

(b) Using the multimeter measure the transistor terminal voltages, referred to pin 3. Typical readings are:

	c	b	e
45VT1	+15 V	*	+4.8 V
45VT2	+15 V	*	+4.1 V
45VT3	+15 V	+9.3 V	+8.6 V
45VT4	+13 V	+3.7 V	+3.0 V
45VT5	+3 V	+0.7 V	0 V
45VT6	+15 V	+4.8 V	+4.1 V

* dependent upon oscillatory condition

8.4.3 Tests and adjustments

(a) Gain 123.1 MHz

(i) Connect a 50 Ω, 1/4 W resistor between pins 2 and 3 and another between pins 9 and 8.

(ii) Connect the r.f. millivoltmeter to pins 2 and 3 and tune 45L2, 45L4 and 45C11 for a maximum reading, typically 1 V r.m.s.

(b) Gain 133.8 MHz

(i) With the two 50 Ω resistors connected as in the previous adjustment, connect the signal generator output to pins 7 and 6 via a 50 Ω cable and set the frequency to 10.7 MHz at a level of 200 mV r.m.s. measured at pins 7 and 6.

(ii) Connect a spectrum analyser to pins 9 and 8 via a high impedance probe and set to view 123.1 MHz and 133.8 MHz (calibrated at 100 mV with VHF signal generator).

(iii) Tune 45TR1, 45C28 and 45C29 for a maximum 133.8 MHz level. Reset level at pins 7 and 6 for 300 mV r.m.s. then the 133.8 MHz level is typically 200 mV r.m.s. with the 123.1 MHz level approximately 12 dB lower.

Note: 1. Inductors 45L2, 45L4 and 45L5 and capacitor 45C11 may be re-adjusted after the board has been replaced and operating in the module to obtain a maximum 133.8 MHz output.

8.5 Control Down-Mixer Board 1R66446

Refer Alignment Procedure Part 4, Sub-section 4.2.2 and Figure 2-9.

8.5.1 Function

The control down-mixer board is a 133.8 MHz to h.f. down frequency mixer and is part of the VCO module. It consists of the following:

(a) A 135 MHz - 165 MHz injection amplifier to drive the mixer diodes

(b) A 133.8 MHz bandpass filter before the mixer diodes and

(c) A 1.6 MHz - 30 MHz amplifier to the output.

8.5.2 Voltage analysis

(a) Connect the +15 V power supply to the board, positive to pins 4 and 9 and negative to pin 3 (common).

(b) Using the multimeter measure the transistor terminal voltages, referred to earth. Typical readings are:

	c	b	e
46VT1	+15 V	+9.3 V	+8.6 V
46VT2	+13 V	+3.9 V	+3.2 V
46VT3	+3 V	+0.7 V	0 V
46VT4	+15 V	+1.1 V	+0.4 V
46VT5	+15 V	+3.7 V	+3 V

8.5.3 Tests and adjustments

(a) Gain

(i) Connect a 50 Ω, 1/4 W resistor between pins 11 and 12.

(ii) Connect signal generator No. 1 output to pins 1 and 2 (common) via a 50 Ω cable and set the frequency to 145 MHz at a level of 300 mV r.m.s. measured at pins 1 and 2.

(iii) Connect signal generator No. 2 output to pins 6 and 7 (common) via a 50 Ω cable and set the frequency to 133.8 MHz at a level of 300 mV r.m.s. measured at pins 6 and 7.

(iv) Connect the r.f. millivoltmeter to pins 11 and 12 and adjust 46C11 and 46C9 for a maximum reading.

(v) Reconnect the millivoltmeter to pins 6 and 7 and readjust signal generator No. 2 output level to read 200 mV r.m.s.

(vi) Reconnect the millivoltmeter to pins 11 and 12 and check for a typical output level reading greater than 2 V r.m.s.

(vii) Vary the frequency of signal generator No. 1 connected to pins 1 and 2 from 135 MHz to 164 MHz and check that the level measured at pins 11 and 12 does not drop below 0.7 V r.m.s. over the frequency range.

9. FREQUENCY TRANSLATOR MODULE 1J66464

9.1 10.7 MHz V.C.O. Board 1R66438

Refer Alignment Procedure Part 4, Sub-section 4.1.1, and Figure 2-11.

9.1.1 Function

The 10.7 MHz VCO board is part of the frequency translator module and consists of a 10.7 MHz crystal oscillator with provision for frequency locking via an integrating amplifier 38MN1, varactor diode 38C20 used as a trimmer on the crystal and an external frequency error detector (phase comparator in 2nd i.f. loop module).

9.1.2 Voltage analysis

(a) Two 15 V power supplies are required.

(i) Connect a jumper lead between pins 2 and 11.

(ii) Connect the positive of power supply No. 1 to pin 11 and the negative to pin 7 and the positive of power supply No. 2.

(iii) Connect the positive of power supply No. 2 to pin 5 and the negative to pin 3.

(iv) Connect a 10 kΩ, 1/4 W resistor to the positive of power supply No. 1. The other end of the resistor is connected in series with a 1 kΩ, 1/4 W linear potentiometer, the other end of which is connected to the negative of the power supply. The potentiometer moving arm is connected to pin 1 on the board.

(b) Using the multimeter measure the transistor terminal voltages, referred to earth. Typical readings are:

	c	b	e
38VT1	+8.8 V	*	*
38VT2	+15 V	+9.5 V	+8.85 V
38VT3	*	*	0 V
38VT4	+15 V	+1 V	+0.35 V

* no meaningful reading

9.1.3 Tests and adjustments

(a) Frequency adjustment

(i) Connect a 50 Ω, 1/4 W resistor between pins 6 and 7 and another between pins 14 and 15.

(ii) Connect a jumper clip/lead from pin 4 to the junction of 38R3 and 38C2.

(iii) Connect a multimeter (low volts scale) to pins 4 (-ve) and 7 (+ve). Set the 1 kΩ test potentiometer for a multimeter reading of approximately 8 V.

(iv) Connect frequency counter to pins 14 and 15 (common) and adjust 38C6 to display 10.7000 MHz. A swing of frequency greater than ±1 kHz should be possible by adjustment of 38C6.

(b) Tuning of 38L4 and 38L7

(i) Adjust 38C6 for a display of 10.7 MHz as above.

(ii) Disconnect the frequency counter and connect the r.f. millivoltmeter to pins 6 and 7 (common).

(iii) Tune 38L4 for a maximum millivoltmeter reading, typically 175 mV r.m.s.

(iv) Connect the millivoltmeter to pins 14 and 15 (common) and tune 38L7 for a maximum reading, typically 900 mV r.m.s.

(v) Recheck the tuning of 38L4 at pins 6 and 7 and then 38L7 at pins 14 and 15.

(vi) Disconnect test equipment and jumper leads between pins 1 and 11 also from pin 4 to junction of 38R3 and 38C2.

9.2 10.45 MHz V.C.O. Board 1R66442

Refer Alignment Procedure Part 4, Sub-section 3.2.1, Figure 2-12.

9.2.1 Function

The 10.45 MHz VCO board is part of the frequency translator module and consists of a 10.45 MHz crystal oscillator the frequency of which is variable by a d.c. voltage supplied from an external error detector (2nd i.f. loop module) via 42MN1 to varactor diodes 42C21 and 42C22.

9.2.2 Voltage analysis

(a) Two 15 V power supplies are required.

(i) Connect jumper leads between pins 5 and 9 and pins 9 and 11 on the board.

(ii) Connect the positive of power supply No. 1 to pin 11 and the negative to board earth and the positive of power supply No. 2.

(iii) Connect the positive of power supply No. 2 to pin 7 and the negative to pin 8.

(iv) Connect a 10 kΩ, 1/4 W resistor to the positive of power supply No. 1. The other end of the resistor is connected in series with a 1 kΩ 1/4 W linear potentiometer, the other end of which is connected to the negative of the power supply. The potentiometer moving arm is connected to pin 6 on the board.

(b) Using the multimeter measure the transistor terminal voltages, referred to earth. Typical readings are

	c	b	e
42VT1	+6.8 V	+1.75 V	*
42VT2	+11 V	+6.8 V	*
42VT4	+15 V	+1.75 V	+0.45 V
	d	s	g
42VT3(FET)	+15 V	+0.3 V	0 V

* No meaningful reading

9.2.3 Tests and adjustments

(a) Frequency adjustment

(i) Connect a 50 Ω, 1/4 W resistor between pins 1 and 2 and another between pins 12 and 13.

(ii) Connect frequency counter to pins 12 and 13 (common).

(iii) Connect multimeter (low volts scale) to pins 10 (-ve) and 13 (+ve).

(iv) Check that by adjustment of the 1 kΩ test potentiometer, the oscillator frequency can be varied between 10.440 MHz and 10.450 MHz: typical multimeter readings for these frequency limits are 2 V and 10 V respectively.

(b) Tuning of 42L1 and 42L2.

(i) Set the 1 kΩ test potentiometer to display 10.445 MHz on the frequency counter.

(ii) Disconnect the frequency counter from pins 12 and 13 and connect the r.f. millivoltmeter in lieu.

(iii) Tune 42L1 and 42L2 for a maximum millivoltmeter reading, typically 2.4 V r.m.s.

(iv) Connect the millivoltmeter to pins 1 and 2 and check for a typical reading of 900 mV r.m.s.

(v) Disconnect test equipment and jumper leads between pins 5-9 and 9-11.

9.3 2nd I.F. Mixer Board 1R66443

Refer Alignment Procedure Part 4, Sub-section 3.2(b) and Figure 2-13.

9.3.1 Function

The 2nd i.f. mixer board is part of the frequency translator module. The function of the board is to additively combine the 250 kHz output of the s.s.b. generator module, via the auto attenuator module, with the output of the 10.45 MHz VCO to produce an i.f. of 10.7 MHz.

9.3.2 Voltage analysis

(a) Connect the +15 V power supply to the board, positive to pin 3 and negative to pin 8.

(b) Using the multimeter measure the terminal voltages on 43VT1. Typical readings are:

c	+15 V
b	+3.3 V ±10%
e	+2.75 V ±10%

The above voltages are referred to the negative of the supply. Variation of the "b" and "e" voltages of up to 10% is not necessarily an indication of a fault.

9.3.3 Tests and adjustments

(a) Tuning of 43L2

(i) Connect signal generator No. 1 output to pins 5 and 6 (common) and set the frequency to 10.45 MHz ±100 Hz using the internal crystal calibrator. Using the r.f. millivoltmeter, set the output level for 500 mV at pins 5 and 6.

(ii) Connect the r.f. millivoltmeter to test point "B" and earth at pin 2.

(iii) Tune 43L2 for maximum output which should be in the range 500 mV to 700 mV.

(b) Tuning of 43L3 and overall gain measurement

(i) Connect signal generator No. 2 output to pins 1 and 2 (common) and set the frequency to 250 kHz ±100 Hz. Using the r.f. millivoltmeter, set the output level for 100 mV at pins 1 and 2.

(ii) Connect the r.f. millivoltmeter to pins 7 and 8 (common) terminated with a 50 Ω, 1/4 W resistor.

(iii) Tune 43L3 for maximum output which should be approximately 40 mV, after 9.3.3 (c).

(c) Carrier balance

(i) Disconnect signal generator No. 1 from pins 5 and 6 and check that the output at pins 7 and 8 drops to less than 7 mV.

(ii) If the output is 7 mV or greater, connect test point "A" to test point "B" or "C" (whichever gives a reduction in output) and adjust 43C2 for minimum output.

Notes: 1. In noisy conditions it may be necessary to screen the board to permit correct carrier balance measurements. However this test may be postponed until the board is installed in the exciter.

2. 43VT1 may oscillate without sufficient drive which is normal because of the very low damping of the 43L2 circuit with a low level signal.

9.4 2nd I.F. Amplifier Board 1R66444

Refer Alignment Procedure Part 4, Sub-section 3.2 (c) and Figure 2-14.

9.4.1 Function

The 2nd i.f. amplifier board is part of the frequency translator module. The function of the board is to amplify and filter the 10.7 MHz output from the 2nd i.f. mixer board using a crystal bandpass filter.

9.4.2 Voltage analysis

(a) Connect the +15 V power supply to the board, positive to pin 1 and negative to pin 2.

(b) Using the multimeter measure the terminal voltages on 44VT1, referred to earth. Typical readings are:

c	+15 V
b	+3.5 V ±10%
e	+2.9 V ±10%

9.4.3 Tests and adjustments

(a) Gain

(i) Connect pin 6 to pin 5.

(ii) Connect a 1200 pF ±5%, 500 VDCW, metallised mica, style CM06 capacitor between pins 4 and 5.

(iii) Connect a 50 Ω ±2%, 1/2 W, metal oxide, style RFG5-E resistor between pins 4 and 5 i.e. the 1200 pF capacitor and 50 Ω resistor are connected in parallel between pins 4 and 5.

(iv) Connect the signal generator output to pins 3 and 2 (common) and set the frequency to 10.7 MHz at a level of 50 mV r.m.s. measured

at pins 3 and 2.

(v) Connect the r.f. millivoltmeter to pins 4 and 5 (common).

(vi) Tune 44L4, 44L2 and 44L3, in that order, for a maximum reading on the millivoltmeter which should be approximately 80 mV r.m.s.

(vii) Remove test equipment and connection between pins 6 and 5.

Notes: 1. Inductors 44L2 and 44L3 may require readjustment when replaced in the frequency translator module.

2. The overall gain as indicated by the above figures corresponds to an output termination of 50 Ω. When the board is replaced in the frequency translator module the output termination is 200 Ω and the gain will be 6 dB greater.

9.5 Signal Up-Mixer Board 1R66448

Refer Alignment Procedure Part 4, Sub-section 3.3.1, Figure 2-15 and Test Transformer, Figure 2-28(F).

9.5.1 Function

The signal up-mixer board is a 10.7 MHz to 133.8 MHz up frequency mixer and is part of the frequency translator module. It consists of the following:

(a) A 123.1 MHz injection amplifier to drive the mixer diodes

(b) A 133.8 MHz amplifier and

(c) Two 133.8 MHz bandpass filters to select the required mixing product.

9.5.2 Voltage analysis

(a) Connect the +15 V power supply to the board, positive to pins 3 and 7 and negative to pin 4 (common).

(b) Using the multimeter measure the transistor terminal voltages, referred to earth. Typical readings are:

	c	b	e
48VT1	+15 V	+9.3 V	+8.6 V
48VT2	+2.8 V	+0.7 V	0 V
48VT3	+3 V	+3.7 V	+3 V
48VT4	+14.5 V	+4.4 V	+3.7 V

9.5.3 Tests and adjustments

Refer to Figure 2-28(F) for connections to Test Transformer type 403V57998.

(a) Gain

(i) Connect signal generator output to pins 1 and 2. Set to 123.1 MHz at a level of approximately 300 mV r.m.s. measured at pins 1 and 2.

(ii) Connect a 50 Ω, 1/4 W resistor between pins 9 and 10.

(iii) Connect Test Transformer 403V57998 and 470 pF capacitor to pins 5 and 6, refer Figure 2-28(F).

(iv) Connect the test transformer to the h.f. signal generator via a 50Ω cable. Set the signal generator to 10.7 MHz at a level to give 60 mV r.m.s. as measured with the spectrum analyser connected to pins 5 and 4. (Calibrate spectrum analyser and probe with the h.f. signal generator.)

(v) Connect the spectrum analyser to pins 9 and 10, via the probe, and set to view 123.1 MHz and 133.8 MHz.

(vi) Adjust 48C23, 48C22, 48C16 and 48C14 for a maximum 133.8 MHz level on the spectrum analyser, a typical level being 45 mV r.m.s. with the 123.1 MHz level more than 20 dB lower. (Calibrate the spectrum analyser and probe with the v.h.f. signal generator.)

(vii) Disconnect the test equipment and test transformer.

Note: Capacitors 48C23, 48C22, 48C16 and 48C14 may be readjusted slightly when the board is replaced in the module and the exciter is operative.

9.6 Signal Down-Mixer Board 1R66449

Refer Alignment Procedure Part 4, Sub-section 3.3.1 (b) and Figure 2-16.

9.6.1 Function

The signal down-mixer board is a 133.8 MHz to h.f. down frequency mixer and is part of the frequency translator module. It consists of the following

(a) A 135 MHz - 165 MHz injection amplifier to drive the mixer diodes

(b) A 133.8 MHz amplifier and bandpass filter before the mixer diodes and

(c) A 30 MHz low-pass filter to the output.

9.6.2 Voltage analysis

(a) Connect the +15 V power supply to the board, positive to pins 3 and 4 and negative to pin 9 (common).

(b) Using the multimeter measure the transistor terminal voltages, referred to earth. Typical readings are:

	c	b	e
49VT1	+15 V	+9.3 V	+8.6 V
49VT2	+2.8 V	+0.7 V	0 V
49VT3	+11.5 V	+3.7 V	+3.0 V
49VT4	+14.5 V	+4.7 V	+3.7 V

9.6.3 Tests and adjustments

(a) Gain

(i) Connect signal generator No. 1 output to pins 1 and 2. Set to 165 MHz at a level of approximately 300 mV r.m.s. measured at pins 1 and 2.

(ii) Connect signal generator No. 2 output to pins 5 and 6. Set to 133.8 MHz at a level of 50 mV r.m.s. measured at pins 5 and 6.

(iii) Connect the r.f. millivoltmeter to pins 10 and 9 (common) terminated with a 50 Ω, 1/4 W resistor.

(iv) Tune 49C14, 49C16, 49L4, 49L6 and 49L7 for a maximum reading on the millivoltmeter. Retune 49L6 and 49L7 so that the level at pins 10 and 9 just starts to decrease.

(v) Connect spectrum analyser probe to the junction of 49R11 and 49R12 and set to view 123.1 MHz and 133.8 MHz.

(vi) Retune 49L4 for a maximum at 133.8 MHz and tune 49L3 for a minimum at 123.1 MHz. Reset the output of signal generator No. 2 for a level of 50 mV r.m.s. measured at pins 5 and 6, then a typical output level at 30 MHz measured at pins 10 and 9 is 32 mV r.m.s.

(vii) Change frequency of signal generator No. 1 connected to pins 1 and 2 from 165 MHz to 135 MHz, the level measured at pins 10 and 9 should vary less than 2 dB.

Note: Capacitors 49C14, 49C16 may be readjusted slightly when the board is replaced in the module and the exciter is operative.

9.7 Wideband Amplifier Board 2R66450

Refer Alignment Procedure Part 4, Sub-section 3.4.1 and Figure 2-17.

9.7.1 Function

The wideband amplifier board is a 1.6 MHz to 30 MHz amplifier with bias filtering and is part of the frequency translator module. It is used to raise the signal level from the mixer circuits to a level suitable to drive the ATS-1 transmitter, i.e. 20 mW into 50 Ω.

9.7.2 Voltage analysis

(a) Connect the +15 V power supply to the board, positive to pin 3 and negative to pin 6 (common).

(b) Using the multimeter measure the transistor terminal voltages, referred to pin 6. Typical readings are:

	c	b	e
50VT1	+15 V	+0.9 V	+0.25 V
50VT2	+15 V	+2.7 V	+2 V

9.7.3 Tests

(a) Frequency response

(i) Connect signal generator output to pins 1 and 2 (common) and signal receiver to pins 5 and 6 (common) and set for 50 Ω termination.

(ii) Set input level to 32 mV r.m.s. at approximately 8 MHz. A typical output level is 1 V r.m.s. corresponding to a 30 dB gain.

(iii) Vary the input frequency to 1.6 MHz and to 30 MHz. The output level should not drop more than 3 dB below the peak at 8 MHz.

10. S.S.B. GENERATOR MODULE 1J66454

10.1 S.S.B. Generator Board 1R66439

Refer Alignment Procedure Part 4, Sub-sections 3.1 (a) and 3.1.1, Figure 2-24 and Test Set-up Figures 2-28(A) and (B).

10.1.1 General

During tests and adjustments on the s.s.b. generator, unless otherwise specified, the clipper is disconnected and the a.g.c. is OFF i.e. pins 16 and 17 are to be linked and check that there is no link between pins 18 and 19.

For sensitivity measurements all figures quoted are true levels as measured with an accurate VTVM, such as the H.P. 411A listed in the test equipment, and are not signal generator open circuit voltages, unless otherwise specified.

10.1.2 Function

The s.s.b. generator board is used in the exciter to provide a modulated 250 kHz i.f. signal which is translated by other units of the exciter to the frequency and level required by the ATS-1 transmitter.

It is mounted on the s.s.b. generator module frame and functions in conjunction with a front panel meter and the toggle switch. For this reason tests and adjustments are performed on the complete module.

10.1.3 Voltage analysis

(a) Connect the 15 V power supply to SKA(12,30), refer Figure 2-28(A).

(b) Using the multimeter measure the transistor terminal voltages, referred to earth. A variation of ±10% is considered normal. Typical readings are as follows:

	c/d	b/gl	e/s	Notes:
39VT1	+8.7 V	+6.2 V	+5.4 V	1.
39VT2	+8.7 V	+2.75 V	+5.4 V	1.
39VT3	+8.7 V	+4.4 V	+4.1 V	1.
39VT4(FET)	+9.7 V	0 V	+0.5 V	2.
39VT5	+14 V	+4.1	+3.5 V	

10.1.3 Voltage analysis (continued)

	c/d	b/gl	e/s	Notes:
39VT6	+14 V	+4.2 V	+3.6 V	
39VT7	+13.7 V	0 V/+6.2 V	+3.6 V	3.
39VT8	+13.7 V	0 V/+4.2 V	+3.6 V	3.
39VT9	+11 V	0 V/+6.9 V	+3.2 V/+6.2 V	4.
39VT10	+11 V	+3.5 V	+3.2 V/+6.2 V	4.
39VT11	+14.5 V	+5.4 V	+4.8 V	5.
39VT12	+14.5 V	+5.4 V	+4.8 V	5.
39VT13	+14.5 V	+5.4 V	+4.8 V	5.
39VT14	+14.5 V	+5.4 V	+4.8 V	5.
39VT15	+14.5 V	+5.4 V	+4.8 V	5.
39VT16	+14.5 V	+5.4 V	+4.8 V	5.
39VT17	+12.5 V	+4.5 V	+3.8 V	
39VT18	+12 V	+5.3 V	+4.7 V	

Notes: 1. A3J operation.

2. Dual gate F.E.T. g2 = +2.5 V

3. The higher base voltage for A3 (a.m.) operation.

4. The higher emitter voltage for 39VT9 switched ON.

5. Base of switched on transistor = +5.4 V. All others at 0 V.

10.1.4 Tests and adjustments

Refer to Figure 2-28(A) for connections to 15 V power supply, audio and 250 kHz signal inputs and six position rotary switch for mode selection via SKA (ISEP 33-way connector socket).

(a) 39VT1 sensitivity

(i) Set for A3J operation and feed 250 kHz at a level of 0.1 V r.m.s. to SKA(1,2).

(ii) Connect r.f. millivoltmeter to pin 3 and tune 39L6 for maximum output; it should be approximately 1 V r.m.s.

(iii) Increase the 250 kHz input level to 0.5 V r.m.s., the output level should increase to approximately 2 V r.m.s.

(b) 39VT9 sensitivity

(i) Set for A1 operation and feed 250 kHz at a level of 0.1 V r.m.s. to SKA(1,2).

(ii) Connect r.f. millivoltmeter to pin 1 and earth and tune 39TR5 for a maximum output, it should be approximately 0.5 V r.m.s.

(iii) Increase the 250 kHz input level to 0.5 V r.m.s., the output level should increase to approximately 1 V r.m.s.

(c) 39VT8 sensitivity

(i) Set for A3J operation and feed 250 kHz at a level of 50 mV r.m.s. to the junction of 39R113 and 39R114.

(ii) Connect r.f. millivoltmeter to SKA(13,17) and terminate with a 50 Ω, 1/4 W resistor.

(iii) Tune 39TR3 for a maximum millivoltmeter reading, typically 200 mV r.m.s.

(d) 39VT7 sensitivity

(i) Set for A3 operation. Turn 39RV11 fully clockwise and feed 250 kHz at a level of 50 mV r.m.s. to the junction of 39R41 and 39RV11.

(ii) Connect r.f. millivoltmeter to SKA(13,17) and measure the output level, typically 200 mV r.m.s.

(e) 39VT11 - 39VT15 sensitivity

(i) Feed 250 kHz at a level of 1 V r.m.s. to pin 1 and earth (signal generator disconnected from SKA(1,2)).

(ii) Connect r.f. millivoltmeter to SKA(13,17) terminated with a 50 Ω resistor and adjust 39RV4, 39RV5, 39RV6, 39RV7 and 39RV8 for maximum output.

(iii) Set for A1 operation and tune 39TR6 for maximum output measured on the millivoltmeter.

(iv) Check the output for typical levels as below:

Operation	Output Level
TUNE	190 mV r.m.s.
A1	250 mV r.m.s.
A3	140 mV r.m.s.
A3H	140 mV r.m.s.
A3A	36 mV r.m.s.

(f) 39VT17 and VT8 overall sensitivity

(i) Set for A3J operation. Connect r.f. millivoltmeter to SKA(13-17) terminated with a 50 Ω resistor and set 39RV9 fully clockwise.

(ii) Feed 250 kHz to pin 20 and earth and tune 39TR4 for maximum. Measure the input level required for 200 mV r.m.s. output, typically 10 mV r.m.s.

(g) 39VT4, 39VT5 and 39VT6 overall sensitivity and stage levels

(i) Connect r.f. millivoltmeter to pin 9 and earth. Set 39RV2 and 39RV3 fully clockwise.

(ii) Feed 250 kHz in turn to pin 8, pin 15 and pin 14 and tune 39TR2 and 39L4 for maximum.

(iii) Measure the input levels required for a 3 V r.m.s. output level at pin 9. Typical levels are shown below:

Test Points	Input Levels	Output at Pin 9
Pin 8	330 mV r.m.s.	3 V r.m.s.
Pin 15 *	60 mV r.m.s.	3 V r.m.s.
Pin 14	15 mV r.m.s.	3 V r.m.s.

* Feed via fixed capacitor.

(h) 39VT4 to 39VT8 sensitivity and stage levels

(i) Set for A3J operation. Connect r.f. millivoltmeter to SKA(13-17) terminated with a 50 Ω resistor and set 39RV2 and 39RV9 fully clockwise (see Note 1).

(ii) Feed a 248.6 kHz signal in turn to pin 20, pin 18, 39C66, pin 15 and pin 14 and measure the input levels required to obtain a 200 mV r.m.s. output level at SKA(13-17). Typical levels are shown below:

Test Points	Input Levels
Pin 20	10 mV r.m.s.
Pin 18	0.22 V r.m.s.
39C66	0.125 V r.m.s. (for Collins filter)
Pin 15	17 mV r.m.s.
Pin 14	4 mV r.m.s. (This level subject variation due to 3N159(FET) variation.)

Note: 1. 39RV2 and 39RV9 will be finally set at a later stage.

(j) Modulator tests

(i) Set for A3J operation and feed 250 kHz to SKA(1,2) at a level of approximately 0.5 V r.m.s.

(ii) Connect r.f. millivoltmeter to pin 14 and earth.

(iii) Feed a 6 kHz audio signal to SKA(33-32) at a level of -20 dBm.

(iv) Tune 39L2 and 39L3 for a maximum on the millivoltmeter, typically 40 mV r.m.s. at pin 14 after adjustment as in (vi) below.

Note: Because of the tight coupling between 39L2 and 39L3 a frequency of at least 6 kHz is necessary to ensure accurate and symmetrical tuning.

(v) Connect r.f. millivoltmeter to pin 18 and earth and adjust 39RV2 for a reading of approximately 500 mV r.m.s.

(vi) Remove the audio signal and link pin 10 to pin 11 or pin 12 to pin 13 and adjust 39RV1 and 39C3 for a minimum output measured at SKA (13,17). For more precise adjustments, a selective millivoltmeter or a spectrum analyser should be connected to the s.s.b. generator output.

(vii) Re-connect the audio signal generator to SKA(33,32) and check the frequency response by varying the frequency from 200 Hz to 3 kHz. The response should be flat within ±0.1 dB.

(k) 39VT18 sensitivity

(i) Feed 250 kHz at a level of 50 mV r.m.s. to SKA(13,17) i.e. to s.s.b. generator output and set 39RV10 fully clockwise.

(ii) Connect a d.c. VTVM to pin 4 and earth and tune 39L5 for a maximum.

(iii) Increase the signal generator input level until +20 V is measured on the VTVM. A typical input level is 80 mV r.m.s.

(l) Level adjustment - calibration of 54M1

(i) Feed 250 kHz at a level of 200 mV r.m.s. to SKA(13,17) i.e. to s.s.b. generator output.

(ii) Set front panel toggle switch 54SWA to the 0 dB position and adjust 39RV10 for a 0 dB indication on front panel meter 54M1.

(iii) Reduce the signal input level by 10 dB (to 64 mV r.m.s.) and set 54SWA to the -10 dB position. Adjust 39RV12 for a -10 dB indication on the bottom scale of 54M1.

(m) 39RV9 adjustment

(i) Set for A3J operation and feed 248.6 kHz at a level of 0.5 V r.m.s. to pin 18 and earth.

(ii) Connect r.f. millivoltmeter to SKA(13,17) and adjust 39RV9 for a 200 mV r.m.s. output.

(n) 39RV11 adjustment

(i) Set for A3 operation and feed 248.6 kHz at a level of 0.5 V r.m.s. to pin 18 and earth.

(ii) Connect r.f. millivoltmeter to SKA(13,17) and adjust 39RV11 for a 100 mV r.m.s. output.

(o) Modulation gain - 39RV2 adjustment

(i) Set for A3J operation and feed 250 kHz at a level of 0.5 V r.m.s. approximately to SKA(1,2).

(ii) Connect r.f. millivoltmeter to SKA(13,17) terminated with a 50 Ω resistor and feed a 1.4 kHz audio signal at a level of -20 dBm to SKA(33,32).

(iii) Adjust 39RV2 for an output reading of 200 mV r.m.s. on the millivoltmeter.

(p) Carrier level adjustments - all modes

(i) Connect r.f. millivoltmeter to SKA(13,17) terminated with a 50 Ω resistor and feed 250 kHz at a level of 0.5 V r.m.s. to SKA(1,2).

(ii) Set for TUNE operation and adjust 39RV4 for a 160 mV r.m.s. output (-2 dB).

(iii) Set for A1 operation and adjust 39RV5 for a 200 mV r.m.s. output (0 dB).

(iv) Set for A3 operation and adjust 39RV6 for a 100 mV r.m.s. output (-6 dB).

(v) Set for A3H operation and adjust 39RV7 for a 100 mV r.m.s. output (-6 dB).

(vi) Set for A3A operation and adjust 39RV8 for a 32 mV r.m.s. output (-16 dB).

(q) A3 (d.s.b.) carrier phasing adjustment

(i) Set for A3 operation and feed 250 kHz at a level of 0.5 V r.m.s. to SKA(1,2).

(ii) Connect c.r.o. to SKA(13,17) terminated with a 50 Ω resistor.

(iii) Check the setting of 39RV6 to ensure a level of 100 mV r.m.s. at SKA(13,17).

(iv) Feed audio signal of 1.5 kHz at a level of -20 dBm (600 Ω) to SKA (33,32).

(v) Adjust the slug of 39L6, and if necessary 39TR3, for minimum envelope distortion. If necessary advance 39RV11 for 100% modulation.

(vi) Set for A3J operation and readjust 39RV9 for a level of 200 mV r.m.s. at SKA(13,17).

(r) A.G.C. operation

The a.g.c. function is optional

(i) For a.g.c. operation disconnect the link previously connected between pins 16 and 17.

(ii) Feed a single tone audio signal at a level of -20 dBm (600 Ω) to SKA(33,32) and set 39RV2 for a level of 220 mV r.m.s. at SKA (13,17) terminated with a 50 Ω resistor.

(iii) Set for A3J operation and feed 250 kHz at a level of 0.5 V r.m.s. to SKA(1,2) with 39RV3 turned fully clockwise.

(iv) Increase the audio input level by 10 dB to -10 dBm and readjust 39RV3 for 170 mV p.e.p. output.

(v) Change the audio input to two tones each at a level of -20 dBm and note the output level.

(vi) Increase the audio input by 10 dB to -10 dBm per tone. The output level should not increase by more than 3.5 dB.

(vii) The intermodulation products, test detailed in (s) below, should not be worse than -40 dB.

(viii) Replace link between pins 16 and 17 and reset 39RV2 as in "(o) Modulated gain - 39RV2 adjustment" above.

(s) Intermodulation and carrier rejection

Refer Figure 2-28(B) for test set-up.

(i) Set for A3J operation and feed 250 kHz at a level of 0.5 V r.m.s. to SKA(1,2).

(ii) Feed two audio tones, 1 kHz and 1.6 kHz, at a level of -20 dBm each to SKA(33,32) via a level measuring attenuator.

(iii) Connect spectrum analyser to s.s.b. generator output SKA(13,17) and measure the intermodulation products. They should be better than -40 dB below each tone.

(iv) Similarly check for carrier rejection and optimise the settings of 39RV1 and 39C3.

Note: It should be possible to obtain at least 60 dB carrier rejection below each tone. However, unless 39MR1 to 39MR4 are matched, carrier rejection may be affected by temperature variation.

Carrier rejection of 40 dB below each tone should be considered as minimum performance in the 0 ^{o}C to 50 ^{o}C temperature range.

11. AUTO ATTENUATOR MODULE 1J66455

Refer Alignment Procedure Part 4, Sub-section 3.1.2, Figure 2-23 and Test Set-up, Figure 2-28(C).

11.1 Auto Attenuator Board 1R66440

11.1.1 Function

The auto attenuator module is used in the exciter to facilitate adjustment of the r.f. and audio levels in the ATS-1 exciter/transmitter system. It contains Auto Attenuator Board 1R66440 and other components which are mounted on the

module frame. For this reason, tests and adjustments are performed on the complete module.

It consists of two main sections as follows:

(a) 250 kHz section

This section consists of an amplifier and a 20 dB variable gain attenuator with control circuits. It is used between the s.s.b. generator module, with fixed frequency and peak value levels, and the frequency changing and output sections, combined with the transmitter proper, which require variable output levels.

The attenuator control circuits accept signals for output level limiting, either AUTO operation or MANUAL R.F. GAIN control, and include a facility to hold the current attenuation level should the 250 kHz signal drop below a predetermined threshold.

(b) Audio section

This section consists of two test-tone oscillators, an amplifier with front panel gain control and switching to perform the following:

(i) To connect the amplifier input to the equipment audio input line or

(ii) To switch on either or both test-tone oscillators or to an off state, terminated in 600 Ω.

11.1.2 Voltage analysis

(a) Two 15 V power supplies are required. Refer Figure 2-28(C) for connections to 40PLA via SKA.

(b) Using the multimeter measure the transistor terminal voltages, referred to earth.

(i) The following are typical readings with no 250 kHz input to SKA(33, 32) and the module set for MANUAL control.

	c	b	e
40VT1	+11.4 V	+3.85 V	+3.2 V
40VT5	+5.5 V	+2.8 V	+2.1 V
40VT6	+15 V	+5.5 V	+4.8 V
40VT8	+0.1 V	+0.7 V	0 V
40VT9	+14.5 V	+13.9 V	+14.5 V
40VT10	0 V	+0.7 V	0 V
40VT11	+4.5 V	+1.6 V	+0.9 V
40VT12	+15 V	+4.5 V	+3.8 V
40VT13	+14.6 V	+1.2 V	+0.5 V
40VT14	-10.4 V	0 V	0 V
40VT15	-0.1 V	-0.7 V	0 V
40VT16	-14.6 V	-14.1 V	-14.8 V

	c	b	e
40VT17	-0.6 V	0 V	-0.6 V

(ii) The following are typical readings for the field effect transistors when measured under the following conditions:

250 kHz fed to SKA(33,32) at a level of 200 mV r.m.s.
Module set to MANUAL control.
R.F.GAIN set to maximum and
Test tones F1/F2 switched on.

	d	s	g
40VT2	0 V	0 V	-1.5 V
40VT3	0 V	0 V	-1.5 V
40VT4	+14.5 V	0 V	-1.5 V
40VT7	-3 V	-3 V	-2.3 V

11.1.3 Tests and adjustments

In all of the following tests and adjustments the +15 V and -15 V power supplies are connected to SKA as shown in Figure 2-28(C).

In tests and adjustments a, b, c, d and e below the 250 kHz signal generator output is connected to SKA33 and SKA32 (common) via a 50 Ω cable with the output level set to 200 mV r.m.s. unless stated otherwise. The 250 kHz output at SKA25 and SKA26 (balanced), is terminated with a 50 Ω, 1/4 W resistor.

(a) Tuning of 40TR1 and 40L3

(i) Set 55SWB to MANUAL control and the R.F. GAIN control (55RV7) to mid-range.

(ii) Tune 40TR1 for a maximum output level measured at SKA(25,26).

(iii) Tune 40L3 for a level of 3.1 V r.m.s. measured at pin 27 to common.

(b) Manual attenuator control

(i) Set 55SWB to MANUAL control, connect millivoltmeter to SKA (25,26) and measure the level.

(ii) Adjust R.F. GAIN control (55RV7) over its full range and check that the output level range at SKA(25,26) includes the limits 30 mV r.m.s. to 300 mV r.m.s.

(c) Auto attenuator control

(i) Connect a shorting link between pins 31 and 34.

(ii) Set 55SWB to AUTO control and adjust 40RV6 to measure approximately 150 mV r.m.s. at SKA(25,26). Remove the shorting link

from pins 31 and 34 and check that the measured level increases to more than 300 mV r.m.s.

(iii) Connect a 4.7 kΩ resistor and 1 kΩ potentiometer (RVA) across the +15 V power supply with the multimeter connected as shown in Figure 2-28(C). Connect the moving arm of RVA to SKA(11) via a 47 kΩ resistor.

(iv) Adjust RVA to measure approximately 150 mV r.m.s. at SKA(25, 26). The reading on the multimeter is typically 2.3 V.

(v) Vary RVA by a ±0.02 V multimeter reading and check that the level measured at SKA(25,26) changes by more than ±6 dB.

(vi) Set 55SWB to MANUAL control and the R.F. GAIN control (55RV7) to measure approximately 150 mV r.m.s. at SKA(25,26).

(vii) Adjust RVA over its full range and check that the level measured at SKA(25,26) varies less than 0.5 dB. This test checks the operation of 40VT10.

(viii) Remove the connection from the moving arm of RVA to SKA(11).

(d) Attenuator amplifier output limit

(i) Set RVA fully anticlockwise i.e. 0 V reading on the multimeter, refer Figure 2-28(C)

(ii) Set 55SWB to MANUAL control and adjust R.F. GAIN control (55RV7) to measure approximately 300 mV r.m.s. at SKA(25,26).

(iii) Connect moving arm of RVA to SKA(17) and set it for a reading of 2.5 V on the multimeter.

(iv) Adjust 40RV5 and check for a switching action of the level at SKA (25,26) to a reading less than 100 mV r.m.s.

Note: The adjustment of 40RV5 is finally set in conjunction with the ATS-1 Transmitter to limit the exciter output level, via the level at 40PLA(SKA) (25,26), to that giving a 55% f.s.d. reading on the transmitter multimeter (4M1), set to EXCITER OUTPUT, during the coarse tuning stage.

(v) Disconnect the moving arm of RVA from SKA(17).

(e) Trigger amplifier and gain hold

(i) Connect multimeter to pins 30 and 34 (common), check for a reading of approximately +13 V.

(ii) Set 55SWB to MANUAL control and the R.F. GAIN control (55RV7) to measure approximately 300 mV r.m.s. at SKA(25,26).

(iii) Slowly decrease the 250 kHz input level to SKA(33,32) until the voltage on the multimeter, connected to pins 30 and 34, switches to approximately -15 V. The input level at SKA(33,32) is then

typically 20 mV r.m.s.

(iv) Observe the output level at SKA(25,26) and check that it is not affected by switching 55SWB and that the level has not visibly dropped after a period of 10 minutes from the d.c. voltage switching as in (iii) above.

Note: On a long term basis the level at SKA(25,26) should not drop by more than 2 dB in 5 hours.

(v) Disconnect the 250 kHz signal generator.

(f) Audio amplifier

(i) Connect audio distortion and noise meter to SKA(6,5) and set to measure level for a 600 Ω termination.

(ii) Set 55SWA to LINE and feed a 1000 Hz signal at a level of +4 dBm (600 Ω) balanced to SKA(1,2).

(iii) Vary the amplifier gain from minimum to maximum by varying 55RV1 from fully anti-clockwise to fully clockwise and check that the level measured at SKA(6,5) varies over an 18 dB range, typically -32 dBm to -14 dBm.

(iv) Set 55RV1 for a -20 dBm level at SKA(6,5) and check that the distortion at this level and frequency is less than 0.2%.

(v) Vary the input frequency over the range 350 Hz to 2.7 kHz and check that the level at SKA(6,5) varies less than ±0.5 dB.

(vi) Set the input frequency to 50 Hz by watching for a dip in the level at SKA(6,5), check that this level is more than 25 dB below the level at 1 kHz.

(g) Test Tone Oscillator F1 (1100 Hz)

(i) Connect audio distortion and noise meter to SKA(6,5) and set to measure level for a 600 Ω unbalanced termination.

(ii) Connect frequency counter to SKA(6,5) and set 55SWA to F1.

(iii) Set 55RV1 as in (f) above and both 40RV2 and 55RV8 to mid-range.
Note: The value of resistor 40R21 has been selected from 2.7 kΩ, 3.0 kΩ or 3.3 kΩ to provide an oscillator frequency of 1100 Hz ±5%.

(iv) Set 40RV2 for a level of 1.7 V r.m.s. measured at pin 35 and 55RV8 for -20 dBm at SKA(6,5).

(v) Check that the distortion at SKA(6,5) is less than 1% then reset 55RV8 for a level of -26 dBm at SKA(6,5).

(h) Test Tone Oscillator F2 (1600 Hz)

(i) Connect audio distortion and noise meter to SKA(6,5) and set to measure level for a 600 Ω unbalanced termination.

(ii) Connect frequency counter to SKA(6,5) and set 55SWA to Fs.

(iii) Set 55RV1 as in (f) above and both 40RV3 and 55RV9 to mid-range.
Note: The value of resistor 40R35 has been selected from 1.8 kΩ, 2.0 kΩ or 2.2 kΩ to provide an oscillator frequency of 1600 Hz ±5%.

(iv) Set 40RV3 for a level of 1.7 V r.m.s. measured at pin 35 and 55RV9 for -20 dBm at SKA(6,5).

(v) Check that the distortion at SKA(6,5) is less than 1% then reset 55RV9 for a level of -26 dBm at SKA(6,5).

- End of Part -