LESSON PRECIS NO: 22

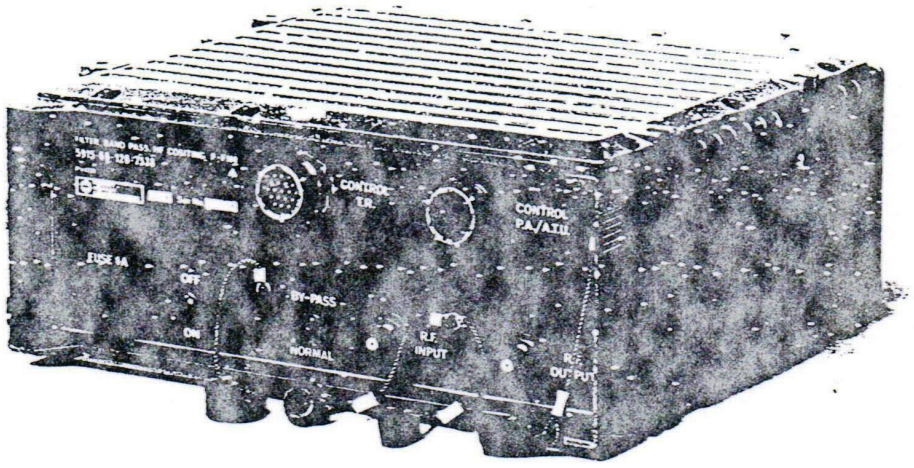
issue 1 July 89

FILTER BAND-PASS HF COSITING (F-F100)

Contents:

TCH 004/3/g (8 Pages)
TCH 004/3/e
TCH 004/3/h

Further information available in
EMEI TELS, T062



FILTER, BAND PASS, HF COSITING,
(DD - F301)

COSITE FILTER
PRINCIPLES OF OPERATION

INTRODUCTION

1. The Filter, Band Pass, HF Cositing F-F100 (CSF) is a microprocessor-controlled switchable bandpass filter for use where radio stations have to operate in close proximity with one another, ie. where more than one station is operating in the same vehicle (cositing), or when two or more vehicles are in close proximity with each other (co-located).

2. When the CSF is connected between a HF R/T and either a PA, or an ATU, the transmitter output from the HF R/T is switched through an automatically tuned bandpass filter to reduce mutual interference with other radio systems. The CSF front panel controls and their functions are shown in EMEI TELS T062 Table 1.

PURPOSE

3. Refer to Figure 1. Without cositing filters the noise produced by Radio 1's transmit signal swamps the received signal of Radio 2. The received signal of Radio 2 is also affected by a strong unwanted signal close to its operating frequency.

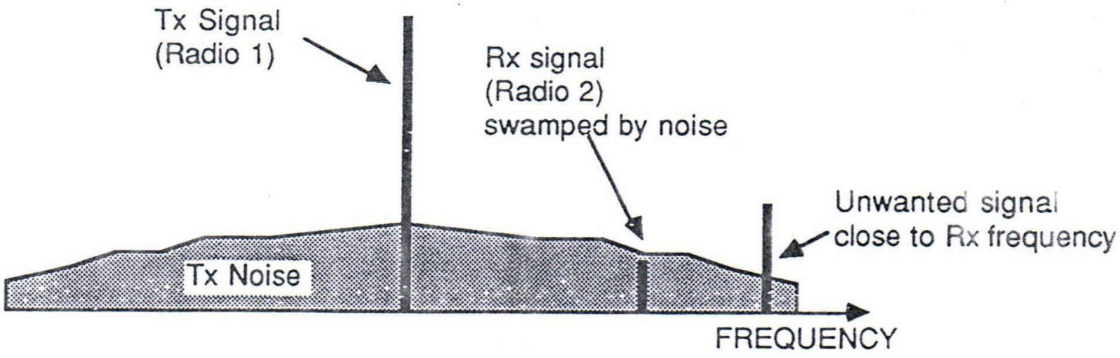


Fig. 1 OPERATING WITHOUT COSITING FILTERS

4. Refer to Fig. 2. With both radios using a cositing filter the transmit signal produced by Radio 1 is now restricted to the bandwidth of its associated cositing filter, and therefore no longer effects the received signal of Radio 2. The efect of Radio 2's associated cositing filter is to improve the selectivity of the receive signal to the extent that the unwanted signal close to its operating frequency is now excluded by the cositing filter's bandwidth.

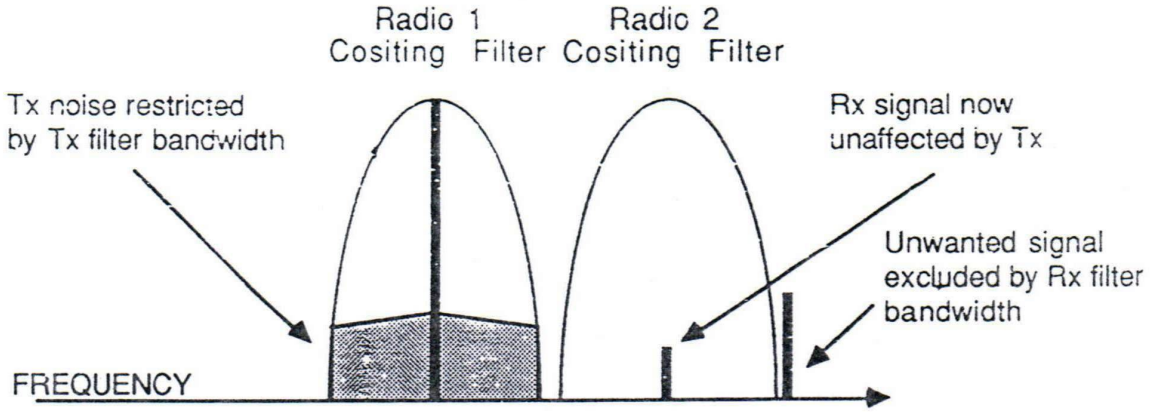


Fig. 2. OPERATING WITH COSITING FILTERS

FILTER ARRANGEMENT

5. Refer to Fig. 3. The frequency range of the CSF (2 - 30MHz) is split into 135 frequency bands, each band covered by a bandpass filter configured from tuned circuits with switchable capacitors. After sampling the transmitter rf, the microprocessor control circuits generate switching signals to configure a bandpass filter whose centre frequency is nearest the HF R/T's transmit frequency.

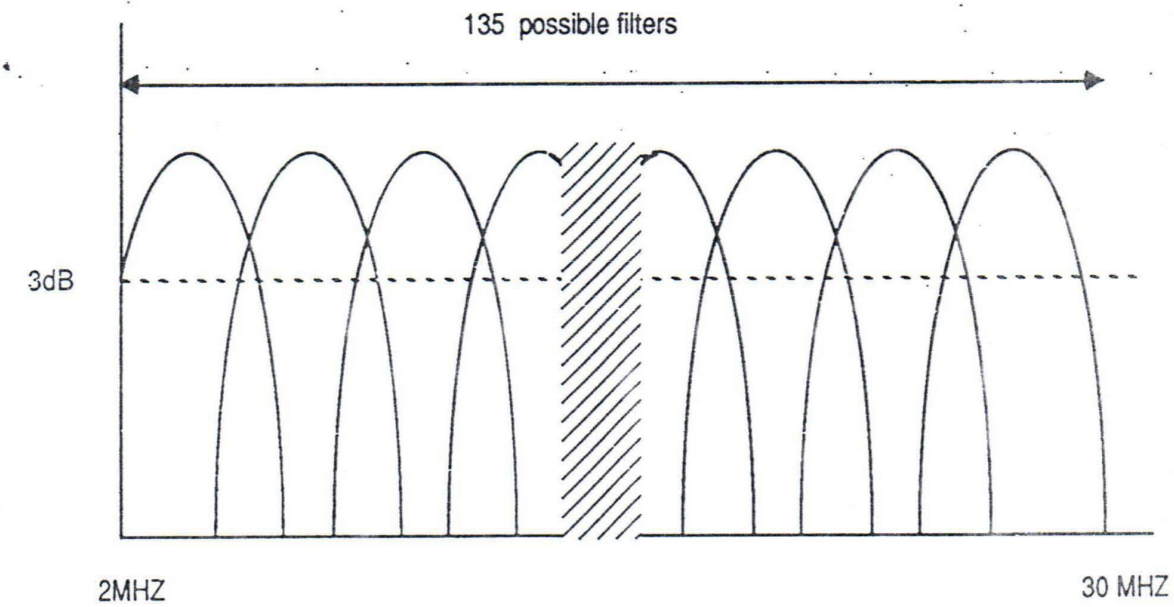


Fig. 3. BANDPASS FILTER OVERLAP

6. The 135 individually selectable bandpass filters have centre frequencies ranging from 2.020MHz to 29.702MHz. By slightly overlapping each adjacent filters frequency response, these 135 filters provide the CSF with an operating range of 2 to 30MHz. The passband of a configured filter is proportional to the transmitter frequency.

BYPASS PATH

7. Refer to Fig. 4. The operation of relays RLA and RLC decides whether the RF output is routed through the filter or straight through the unit via the bypass path. The bypass is selected when the unit is switched off, when the BYPASS switch position is selected and in the preliminary stage of a new tuning sequence. It is also selected during receive in the 2FS mode.

TUNING SEQUENCE

8. Refer to Fig. 4. When the CSF is first powered up a tuning sequence is initiated which results in the switching circuits being set to 'bypass' and the READY line, to the R/T, being set low. The READY line will remain low until the tuning process has been successfully completed. A tuning sequence will also be initiated by a RESET signal which is issued by the R/T whenever the operating frequency is changed. This causes all external units in the output path to prepare for new parameters .

9. When the R/T goes to transmit, it informs the CSF microprocessor of the fact by setting the line 'Tx/Rx' to a low and produces a 5W CW tuning signal at the operating frequency. The CSF control circuits direct the tuning signal, via RLA and RLB, to power and frequency measuring circuits where it is terminated in a 50 ohm load. RLC switches to disconnect the bypass path from the RF output path. If the power of the tuning signal is less than 1W or greater than 7W the bypass route is selected and the FAULT signal sent to the RT.

10. The required passband is calculated from the frequency measurement and the filter configuration relays are used to select the arrangement of components necessary to achieve it. The signal is then routed through the filter, via RLA, and the signal power measured, via the alternative contact of RLB, at the filter output. This enables the loss incurred by the insertion of the filter to be measured. If the loss is acceptable the READY line to the R/T is set high, and, assuming the NORMAL/BYPASS switch is set to NORMAL, the filter output is directed through RLC to the RF OUTPUT line. Otherwise the READY line is held low and the FAULT line is set high (its active state) and the bypass path selected.

OPERATION WITH ATU/PA.

11. If an ATU or a PA, or both, are in use they require access to the tuning signal in order to tune themselves. During the first measurement the tuning signal is therefore terminated by the 'last in line' external unit instead of the CSF 50 Ohm load.

12. The CSF suspends its tuning sequence after calculating the filter required, and before filter output power measurement, to allow the other units to tune. This condition lasts for one second or until the other units indicate a successful tune or an inability to tune by EU READY or EU FAULT respectively. If neither signal occurs within one second the CSF microprocessor assumes a fault and reacts as if EU FAULT had occurred. It therefore holds the READY line low and sets FAULT high. In all cases it then checks the insertion loss.

DETAILED FUNCTIONAL ANALYSIS

MODULES (Refer to Fig. 5)

13. **Module 1.** Module 1 contains a microprocessor which controls the overall operation of the CSF. The memory associated with the microprocessor contains the program of operations plus data to enable the required bandpass for any given frequency to be ascertained.

14. **Module 2.** Module 2 contains the RF routeing relays and the power and frequency measuring circuits.

15. **Module 3.** Module 3 contains the power supply regulator, which produce the 0, 5 and 20 volt supplies for the equipment, control signal level changers, which convert the 0 and 5 volt internal logic levels to the 0 and 10 volt convention used between equipments, and control signal switching relays.

16. **Module 4.** Module 4 includes the CONTROL PA/ATU front panel connector. It provides decoupling of all signal lines except EARTH lines.

17. **Module 5.** Module 5 includes the CONTROL TR front panel connector. It provides decoupling of all signal lines except EARTH lines.

18. **Module 6.** Module 6 contains the bandpass filter components and configuration relays.

NOTE:

THE FOLLOWING DESCRIPTION REFERS TO EMEI TELS TO62 FIG 1001.
All signals that are active LOW are shown in *italics.*

POWER OFF.

19. With the CSF switched off the switching relays on Module 3 are in the position shown in Fig. 6. CSF PRESENT is low, indicating the situation to the R/T. EU PRESENT, EU FAULT and EU READY are passed on to the R/T as EXT. UNIT PRESENT, FAULT and READY respectively.

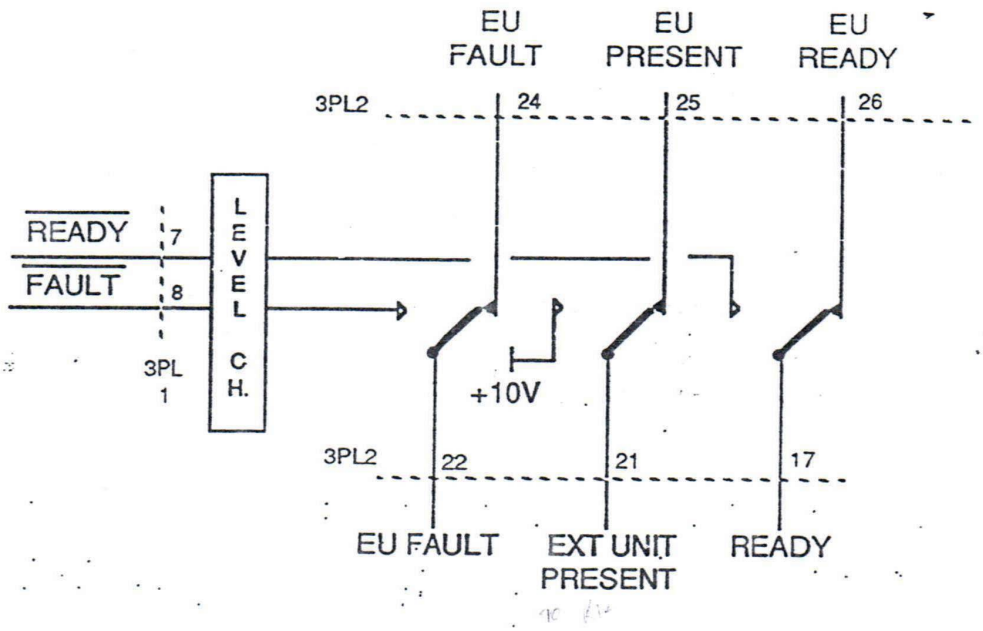


Fig. 6 Switching Relays.

POWER ON.

20. An unswitched 28V supply is provided by the R/T to 5PL1/N, (Module 5, PL1, pin N), decoupled and passed via 5PL3/19 and 20 to 3PL2/19 and 20. It exits on 3PL4/4, to the front panel ON/OFF switch and, with the switch made, returns through FS1 and 3PL4/6 where it is applied to the regulator circuits. The operation of the regulator is controlled by an enabling input, SYSTEM ON, which is produced by the R/T at power on and is applied to the regulator via 5PL1/L, 5PL3/11 and 3PL2/11. With SYSTEM ON high and 28V applied the regulator produces CSF PRESENT at a high. This signal is passed to the R/T, via 3PL2/1, 5PL3/1 and 5PL1/K, to indicate the active presence of the CSF. The switching relays are energised thereby disconnecting EU READY (3PL2/26), EU PRESENT (3PL2/25) and EU FAULT (3PL2/24) from READY (3PL2/17), EXT.UNIT PRESENT (3PL2/21) and EU FAULT (3PL2/22) respectively. EXT.UNIT PRESENT is set high, EU READY and EU FAULT are monitored by the microprocessor which considers their condition and the conditions within the CSF to decide the state of ***READY*** and ***FAULT.*** These are now connected through to the R/T via EU FAULT and READY.

POWER UP RESET

21. When power is initially applied to the microprocessor a BITE routine is initiated to perform basic checks on modules 1 and 2. If a fault is detected the I/O device RAM TIMER 3 is instructed to set *FAULT* low. This is passed via 1PL3/8 and 3PL1/8 to the level changers. The active condition of the signal is inverted and passed via the switching relays to 3PL2/22. It becomes EU FAULT which is sent to 5PL3/22 and then 5PL1/B to emerge as FAULT to the R/T. The appropriate fault LED is lit on Module 1. RAM TIMER 3 sends control signals via 1PL4/23 and 24 to Module 2 RF routeing relays, RLA and RLC, to connect RF INPUT (SK2, 2PL3) to RF OUTPUT (2PL5, SK4). The RF path therefore bypasses the filter. RAM TIMER 3 also produces the signal STOP CLOCK which, as implied, stops the clock to the microprocessor. Under these fault conditions the microprocessor will not respond to other than a power up reset.

22. If no fault is detected the bypass path is selected on Module 2, FAULT remains low and RAM TIMER 2 sends RESET RELAY GROUP via 1PL1/20 and 6PL1/20 to reset the configuration relays on Module 6. The clock is then stopped as already described. The microprocessor is now in what is referred to as its 'sleep' mode, awaiting the initiation of a tuning sequence.

TX FOLLOWING RESET

23. On the next pressel operation Tx/Rx goes to '0' indicating the transmit condition. (Note that even if the pressel is released the R/T will hold Tx/Rx to '0' until the tuning cycle is complete). It arrives as a '1' at 1PL3/2 via 5PL1/F, 5PL3/15, 3PL2/15 and 3PL1/2. It is applied to the clock start circuit and the microprocessor resumes operation. RAM TIMER 2 sends RESET RELAY GROUP to reset the configuration relays on Module 6 (The reason for this apparent 'repeat' operation will be explained in Para 34).

24. The presence of an external unit is checked by examining EU PRESENT, (4PL1/D, 5PL3/25, 3PL2/25, 3PL1/6, 1PL3/6). If EU PRESENT is 'O', indicating no external units fitted, RAM TIMER 3 outputs control signals A, B and C (1PL4/23, 24 & 25) which instruct the RF routeing relays on module 2 to connect the RF INPUT to the power and frequency measuring circuits, via RLA and RLB, isolate RF OUTPUT with RLC, and terminate the RF signal in a 50 ohm load, via RLD. The operation of RLD is decided by decoding control lines B & C. With an external unit present RLD remains open and the RF signal is forwarded through RLC and terminated in the last in line unit.

Power/Frequency Measurement

25. To ensure the readings are both stable and valid, two readings of power and three of frequency are made. The microprocessor uses RAM TIMER 1 to control the operation of the power and frequency measurement circuits. The control lines COUNTER RESET, COUNTER ENABLE, COUNT/ *POWER*, ADC CLOCK and *ADC RESET* provide the control signals to operate the circuits, with the COUNT/POWER and COUNT lines returning values of frequency and power. If the power reading is not in the range 1W to 7W, RAM TIMER 3 sets *FAULT* to '0' and instructs the RF Routeing relays on Module 2 to select the bypass path. The '0' on *FAULT*, forwarded to the R/T as '1' on FAULT, produces a 300Hz 'pips'warning tone in the headset. When the pressel is released the CSF microprocessor enters the "sleep' mode until a further RESET occurs.

26. Providing the power level is correct the frequency count is returned to the microprocessor via the 13 COUNT lines. If two out of the three readings taken are identical the result is considered valid. An invalid reading is processed the same as an invalid power measurement. With a valid frequency reading, the microprocessor proceeds to determine the required filter configuration on Module 6. The frequency value is compared with 135 pairs of upper and lower band limits in memory to obtain a frequency band value for the R.F signal. Filter configuration data for this frequency band are obtained from memory and sent to Module 6 via the SET RELAY and SELECT GROUP outputs from RAM TIMER 2.

27. When the filter is tuned the microprocessor waits for the occurence of EU READY (4SK1/A), EU FAULT (4SK1/B) or the end of a one second delay period before the insertion loss across the filter is checked.

28. If EU FAULT occurs or the one second delay period elapses then an external unit fault is assumed and FAULT (5PL1/B) is set high and READY (5PL1/A) remains low.

29. In any case the microprocessor, via RAM TIMER 3, instructs RLA, RLB and RLD to route RF INPUT to 2PL4, then as NON FILTERED RF to 6 PL2, through the bandpass filter and 6PL3 to become FILTERED RF which goes through 2PL2 to the power and frequency measuring circuits and internal 50 ohm load. RLC is instructed to isolate the RF signal from RF OUTPUT. A power measurement is made and the result compared to the original, pre-filter, value in order to calculate the loss incurred by inserting the filter.

30. If the insertion loss is not between 1dB and 4dB the 'Module 6' fault LED is illuminated on Module 1, READY is held low, FAULT goes to a '1' and the bypass path is selected on Module 2 and the sequence terminated. If the loss is acceptable, i.e. between 1dB and 4dB, the READY line is set to '1'. This indicates to the R/T that the CSF is tuned.

Bypass/Normal

31. The condition of ACTIVE BYPASS is now checked. This signal is controlled by the BY-PASS/NORMAL switch and arrives at 1PL3/9 via 3PL4/3 and 3PL1/9. With the switch set to BYPASS it is at a '1'. The microprocessor instructs the routeing relays to select the bypass path but the filter remains tuned. With NORMAL selected, RLC on Module 2 connects the output of the filter, FILTERED RF, to RF OUTPUT and via SK4 to the antenna or the next in line external unit. (Note that while the CSF is in use any transition on ACTIVE BYPASS will start the clock and the microprocessor will take the appropriate action).

32. If the pressel has been released, Tx/Rx will be set high and the clock will be stopped. This ensures that microprocessor activity does not generate noise during receive. On subsequent transmissions the clock will be switched on to enable external unit inputs to be checked.

RESET FROM R/T.

33. The R/T produces a RESET pulse when a change is required in the filtration of the outgoing RF. The occasions of this are : at R/T power up, at each frequency change and at each Tx/Rx transition during 2FS operation. The RESET pulse arrives as a '0' at 5PL1/G, is decoupled and passes via 5PL3/5 and 3PL2/5, through the level changers to emerge as a '1'. This is applied to the microprocessor interrupt and clock start circuits via 3PL1/1 and 1PL3/1. The clock starts and the interrupt causes the tuning program to begin.

34. The microprocessor instructs RAM TIMER 3 to output a '1' on the ***FAULT*** line (1PL3/8), and a '1' on the ***READY*** line (1PL3/7). These are inverted on module 3 giving FAULT and READY both at '0'. This indicates to the R/T that the CSF requires a tuning signal from which to tune its filter. The bypass path is selected on module 2 and the microprocessor clock is stopped pending a Tx flag from the R/T. The CSF is now ready for the tuning sequence which will begin on the next operation of the pressel and which, during the initial phase, causes the configuration relays to be reset. (Refer to Para 23).

2FS

34. If, on a channel change at the R/T, a 2FS channel is selected, the R/T does not set the 2FS flag immediately. A RESET is produced as usual and the normal tuning sequence is followed. After the first pressel operation has caused the CSF to tune, 2FS goes to '0', its active state. When another RESET occurs as a result of the next transmission, (remember in 2FS RESET occurs at each Tx/Rx transition), both 2FS and Tx/Rx are found to be '0', therefore the microprocessor identifies a '2FS, already tuned, transmit' condition and switches in the already selected filter. When the transmission ends and another RESET occurs, accompanied by Tx/Rx going high, a '2FS Rx' condition is identified and the bypass path is selected. At this point the microprocessor clock will be stopped.

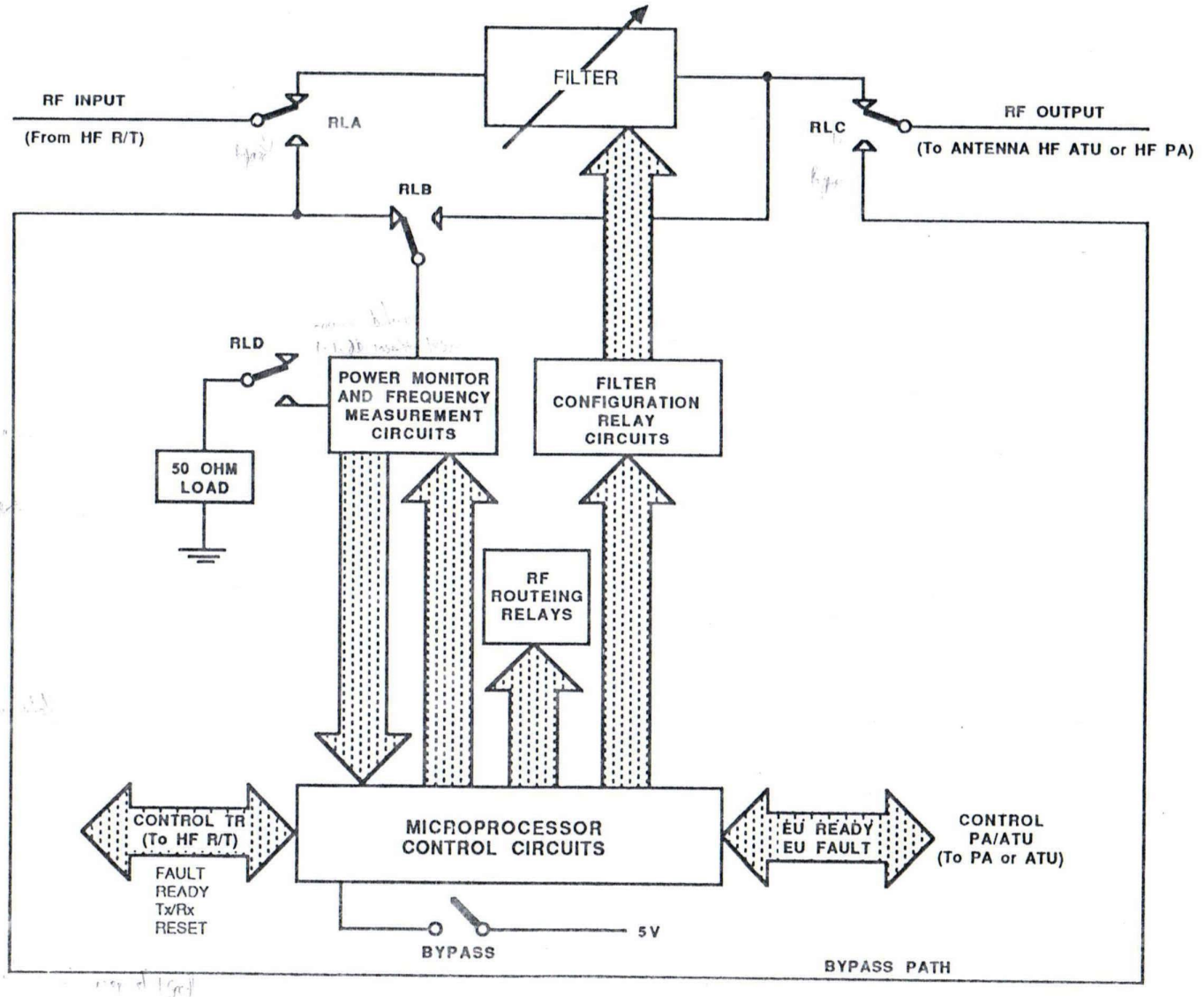


Fig 4 FUNCTIONAL BLOCK DIAGRAM

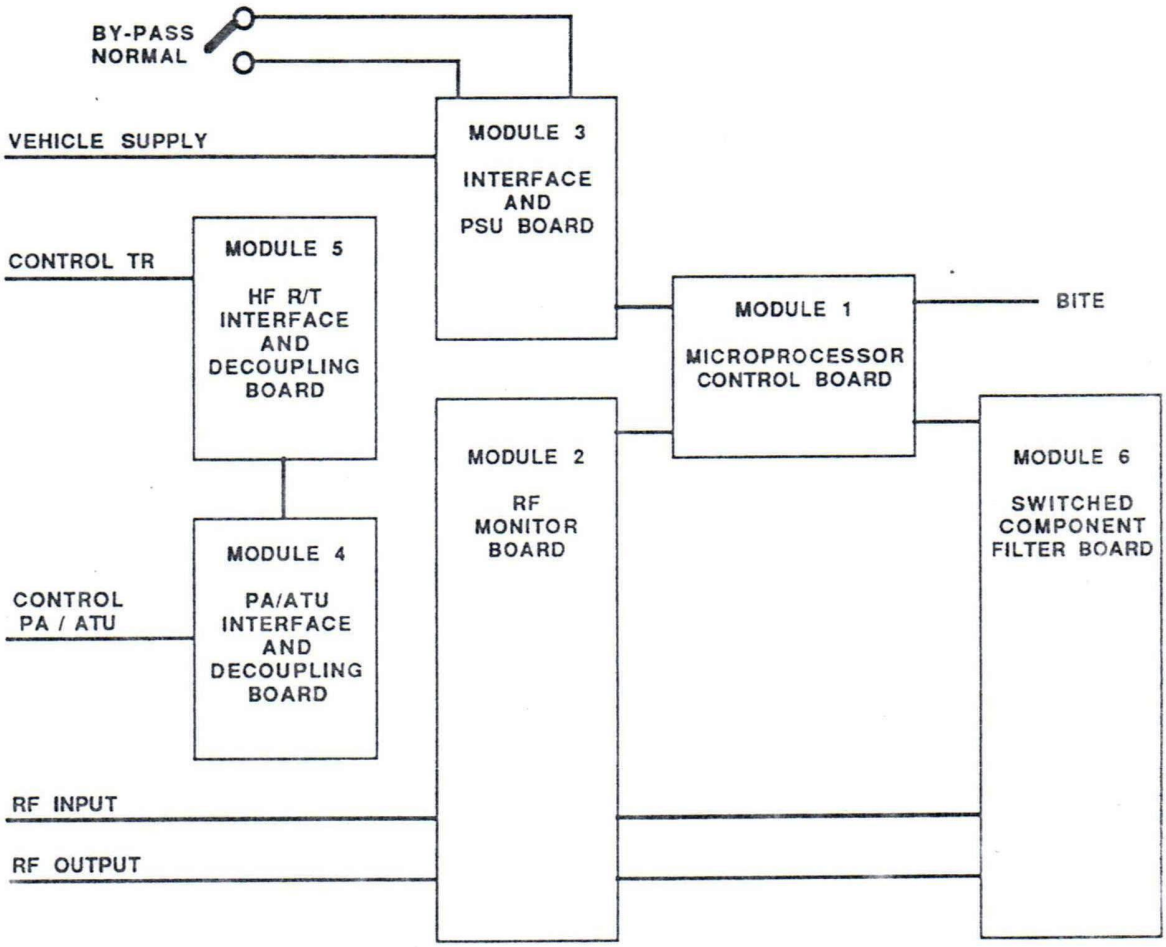


Fig. 5 EQUIPMENT BLOCK DIAGRAM

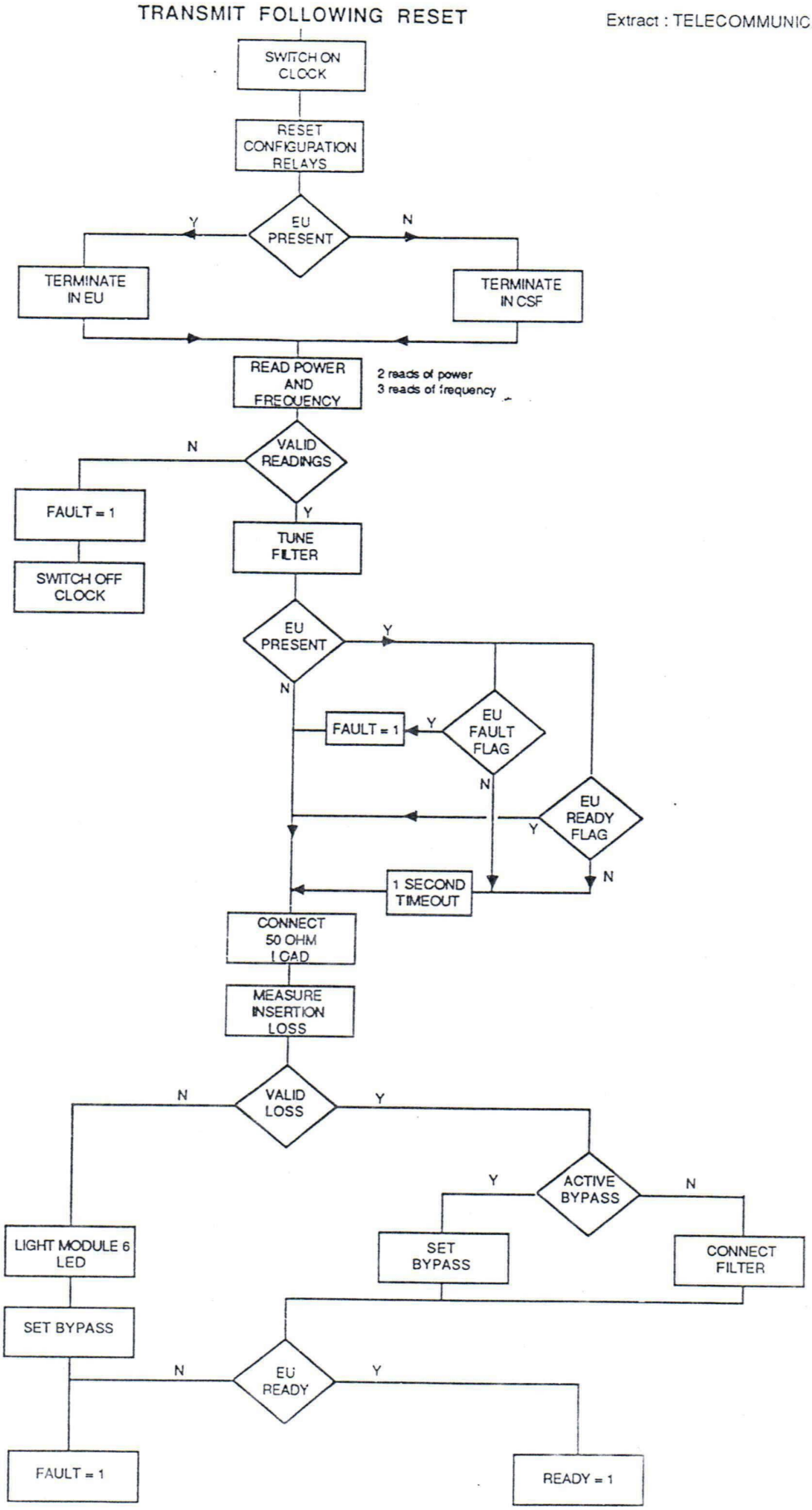
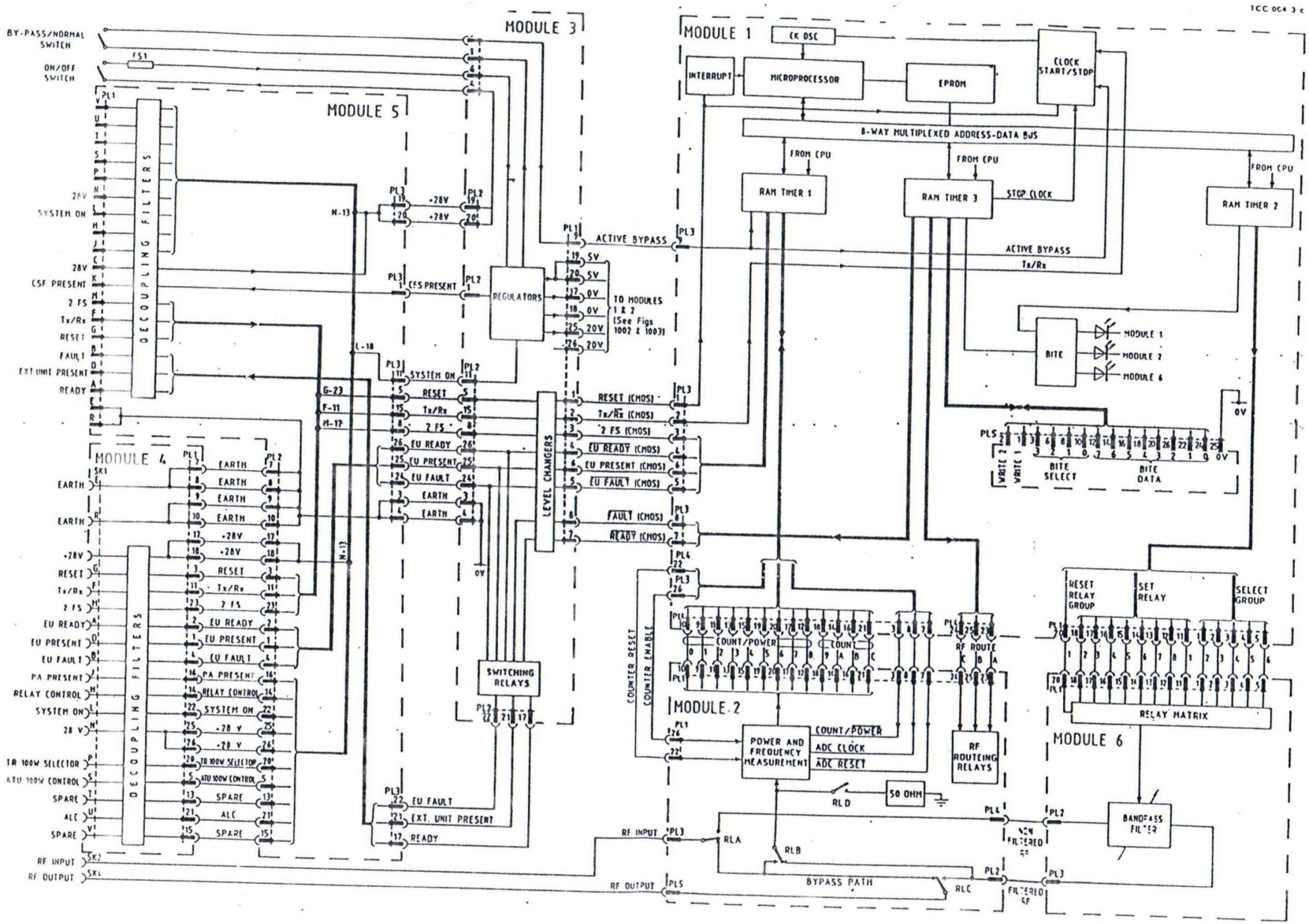

TRANSMIT FOLLOWING RESET
SWITCH ON CLOCK
RESET CONFIGURATION RELAYS
EU PRESENT
Y
N
TERMINATE IN EU
TERMINATE IN CSF
READ POWER AND FREQUENCY
2 reads of power
3 reads of frequency
VALID READINGS
N
Y
FAULT = 1
SWITCH OFF CLOCK
TUNE FILTER
EU PRESENT
Y
N
FAULT = 1
Y
EU FAULT FLAG
N
EU READY FLAG
Y
N
1 SECOND TIMEOUT
CONNECT 50 OHM LOAD
MEASURE INSERTION LOSS
VALID LOSS
N
Y
ACTIVE BYPASS
Y
N
SET BYPASS
CONNECT FILTER
LIGHT MODULE 6 LED
SET BYPASS
EU READY
N
Y
FAULT = 1
READY = 1

Figure. 13



HF CSF (F-F100)
EQUIPMENT FUNCTIONAL BLOCK DIAGRAM

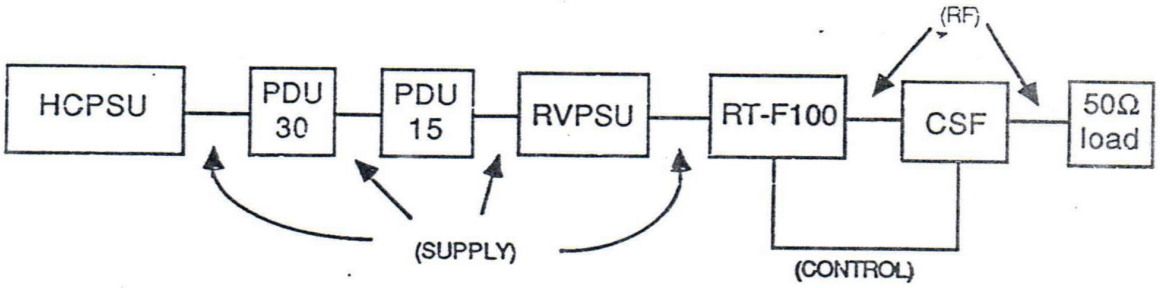
CSF PRACTICAL PROJECT

Section A

1. Remove top and bottom covers from the CSF.

2. Carry out UNIT LEVEL TEST.

3. Connect up Low Power Station as shown below.



4. **Power up the system and check the 'On-Board' BITE Indicators.** Ensure that the three GREEN supply indicators are illuminated and that the three RED Module fault indicators remain off.

Section B

[Note : A CRO is to be used to check the levels during this project.]

1. Set the CRO to measure 2V/Divn, with the timebase at 2mV/Divn. Set to monitor a DC level.

2. Connect (x1) probe to 5PL1/G. Switch on the R/T and CSF. Set the CSF to NORMAL.

3. Activate the Pressel to tune the CSF. In the event that any Audio or visual warnings indicating the presence of a fault should occur, call the instructor.

4. Whilst observing the CRO select an alternative channel at the R/T. Note the Transition that occurred below by entering HIGH/LOW as applicable.

RESET IS A LOGIC PULSE WHICH GOES FROM THE_____TO THE ____STATE.

5. Remove the CRO probe from 5PL1/G.

6. Set the R/T and CSF to the modes shown in Table 1 and Monitor 5PL1 on the CSF as defined in the table.

MODE		5PL1/A (READY)	5PL1/B (FAULT)	5PL1/M (2FS)
NORMAL	EX RESET (PRE-PRESSEL)			
	TUNED (EX-PRESSEL)			
BYPASS	EX RESET (PRE-PRESSEL)			
	TUNED (EX-PRESSEL)			
2FS	EX RESET (PRE-PRESSEL)			
	INITIAL PRESSEL			
	TUNED (EX-PRESSEL)			
FAULT (See note)				

Table 1

Note : Simulate fault by removing 6PL3 and monitor the FAULT and READY lines, Warning Tone/Pips and Module 6 LED. Remove RF I/P and RF O/P connectors. Check that the CSF, with a fault condition apparent, has reverted to the By-Pass Mode.