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ITT Mackay Marine

A DIVISION OF
INTERNATIONAL TELEPHONE AND TELEGRAPH CORPORATION

OPERATION—MAINTENANCE MANUAL
FOR
MARINE RADIO RECEIVER
MACKAY TYPE 3020A
(690001—000—001)

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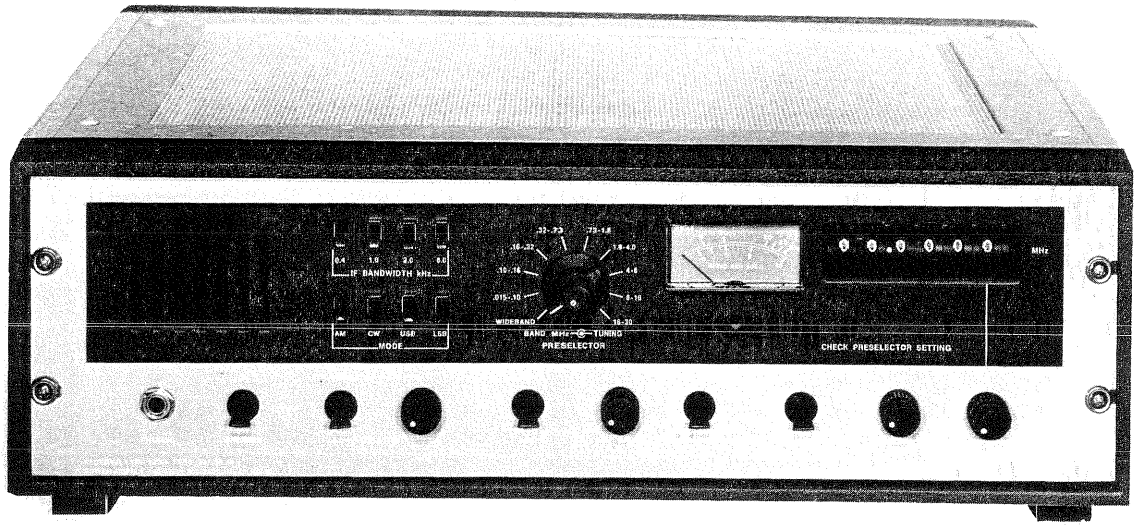


3020A Receiver.

OPERATION-MAINTENANCE MANUAL
for
MARINE RADIO RECEIVER
MACKAY TYPE 3020A
(690001-000-001)

CONTENTS

CONTENTS (Cont)

SECTION 1

GENERAL DESCRIPTION

1.1 INTRODUCTION

The ITT Mackay Marine Model 3020A Radio Receiver is a solid-state dual-conversion superheterodyne receiver providing continuous frequency coverage from 15 KHz to 29.9999 MHz.

This section generally describes the 3020A Receiver and lists the major components and corresponding part numbers. Included are electrical considerations and characteristics applicable to the 3020A.

NOTE

Wiring and schematic diagrams and assembly drawings are contained in Section 7 herein.

1.2 DESCRIPTION

a. Mechanical

The 3020A Receiver is basically packaged as a rack mounted unit 5-1/4 inches high x 19 inches wide x 17 inches deep. The receiver also is available in an optional cabinet.

The receiver consists of a front panel, rear panel, and main chassis, and connection (PC) facilities for the synthesizer and signal path plug-in printed circuit cards.

The main chassis contains the power transformer, power supply filter capacitors, PC connectors for both the synthesizer and signal path, and interconnecting wiring.

The front panel assembly contains all the front panel controls as well as the variable frequency crystal BFO and the RF Preselector subassemblies.

The rear panel assembly contains the power supply rectifier bridges, series pass transistors and associated heat sinks for heat dissipation. The power suppy regulator PC board also is attached to the rear panel assembly.

The following controls are located on the front panel:

Frequency selector switch
METER DISPLAY RF INPUT/AUDIO OUTPUT
AUDIO GAIN POWER OFF switch
SPEAKER ON/OFF switch
RF GAIN/AGC ON
PRESELECTOR BAND MHz TUNING control
ANT. ATTEN. IN/OUT switch
PULL FOR FINE TUNE control
MODE selector switches
IF BANDWIDTH kHz selector switches
AGC FAST/SLOW switch
CW PITCH FIXED/VARIABLE

The antenna input connector, 8 MHz IF monitor output, 3Ω and 600Ω audio output terminals, fuses and AC power cord are located on the rear panel assembly.

b. Major Components

Item	Part Number
Chassis Assembly	600349-705
Rear Panel Assembly	600035-539
Front Panel Assembly	600034-539
Synthesizer Plug-in Units	
Decoder	600582-536
Major Loop VCO Buffer	600583-536
Major Loop Analog and Acquisition	600580-536
Major Loop Variable Divider	600584-536
Loop Translator	600585-536
VHF Reference	600586-536
Low-frequency Reference	600587-536
Minor Loop Analog	600579-536
Minor Loop Variable Divider	600588-536
Signal Path Plug-in Units	
RF Section	600589-536
2nd Mixer	600590-536
IF Amplifier	600591-536
Information Filters	600592-536
AM and Product Detectors	600539-536
AGC Amplifier	600594-536
Audio Amplifier	600595-536
Regulator (Power Supply)	600581-536
Variable BFO	600578-536
Preselector	600125-537

c. Electrical

ITT Mackay Marine 3020A Receiver is a synthesized double-conversion superheterodyne receiver capable of a variety of modes of operation in the frequency range of 15 kHz to 30 MHz. The unit is designed for both high performance and ease of maintenance, heretofore unequalled.

The synthesizer is a VHF digital synthesizer covering the range from 92.0000 MHz to 121.9999 MHz in 100-Hz steps. All output frequencies are phase-locked to a temperature-stabilized crystal oscillator operating at 8 MHz.

The receiver achieves excellent immunity to strong off-frequency signals by careful attention to gain distribution and ultra linear active elements in the front-end, and by up-conversion to a high (92 MHz) first IF frequency to maximize image rejection and minimize effect of harmonic production of front-end stages.

IF Bandwidth can be chosen by the operator for rejection of interfering signals. Bandwidths from 8 kHz to 400 Hz are available through front panel switched crystal filters operating at the 2nd IF (8MHz). Front panel selection of AM, CW, USB and LSB modes is also provided.

1.3 ELECTRICAL CHARACTERISTICS

Frequency Range	15 KHz to 29.9999 MHz. Full sensitivity specifications from 100 KHz to 29.9999 MHz. Sensitivity is reduced uniformly between 100 KHz and 15 KHz by approximately 10 dB at 15 KHz.
Modes of Operation	Upper sideband (USB), lower sideband (LSB), amplitude modulation (AM), continuous wave (CW), radio teletype (RTTY)* and facsimile (FAX).*
Frequency Selection	Digital, 299,850 channels in 100 Hz steps. Fine tune between 100 Hz steps.
Frequency Stability	Frequency drift does not exceed 1 Hz per MHz of tuned frequency over a temperature range of 0° to 50° C., and 1 Hz per MHz of tuned frequency per year after calibration of internal frequency standard.

Sensitivity

IF Band Width	Max. Applied Input for 10 dB $\frac{S+N}{N}$ SSB/CW
8 kHz	0.8 microvolt
2 kHz	0.4 microvolt
1 kHz	0.3 microvolt
0.4 kHz	0.3 microvolt
SSB	0.4 microvolt

Image Rejection	>70 dB
IF Rejection	>70 dB
Sideband Suppression	≥50 dB at 500 Hz into the unwanted sideband.

*With optional external signal processing equipment.

Cross Modulation	With a wanted signal of 500 microvolts, an unwanted signal of 10 millivolts 30%, 400 Hz modulation and separated 10 kHz or more, produces an output at least 30 dB below output level due to the wanted signal.
Blocking	The receiver output due to a wanted signal of 500 microvolts changes less than 3 dB when an unwanted signal of 50 millivolts at least 10 kHz removed is applied.

IF Bandwidth Switch Position	6 dB down	60 dB down
8 KHz	8 KHz min.	20 KHz max.
2 KHz	2 KHz min.	12 KHz max.
1 KHz	1 KHz min.	6 KHz max.
0. 4 KHz	0. 4 KHz max.	4 KHz max.
USB	+350 Hz to +2700 Hz*	≤-500 Hz and ≤+3800 Hz *
LSB	-350 Hz to -2700 Hz*	≤+500 Hz and ≤-3800 Hz *

Automatic Gain Control	Output rise 3 dB max. for input from 3 microvolts to 100, 000 microvolts. Output rises 11 dB max. for input from 1 microvolt to 100, 000 microvolt.

AGC	Slow	Fast
Attack Time	≤ 10 milliseconds	≤ 10 milliseconds
Release Time	2 seconds (nominal)	150 ms (nominal)

Input Impedance		
	. 015 to 29. 9999 MHz	50Ω with preselector in wideband position.
	100 KHz to 4 MHz	Preselector matches receiver input to typical electrically short antennas.
	4 to 30 MHz	50Ω with preselector in tuned positions.
Audio Output	3. 2Ω	1 Watt at 5% max. distortion (internal or external speaker).
	600Ω	10 dBm max.

Primary Power	115/230 ±15% single phase 50/60 Hz
Power Requirements	80 watts at full audio output level.
Temperature, Operational	0 to 50° C (meets GPO specs. requiring operation at -15° C)
Humidity	to 95%
Size	5-1/4" H x 19" W x 17" D
Weight	30 pounds

*Referenced to carrier.

1.4 WARRANTY

Warranty Policy

ITT Mackay Marine, hereinafter referred to as Mackay, warrants that at the time of shipment the products manufactured by Mackay Marine and sold hereunder will be free from defects in material and workmanship and will conform to the specifications furnished by and/or approved by Mackay.

Warranty Adjustment

If any defect within this warranty appears, Purchaser shall notify Mackay immediately. Mackay agrees to repair or furnish a replacement for, but not install, any product, except fuses (see Exclusions), vacuum tubes and transistors, which within eighteen months from date of shipment by Mackay, or, within twelve months from date of acceptance by Purchaser, whichever date first expires, shall upon test and examination by Mackay prove defective within the above warranty. For vacuum tubes and transistors warranty is limited to ninety (90) days from date of shipment by Mackay.

No product will be accepted for return or replacement without the written authorization and in accordance with instructions by Mackay. The product will be returned to Mackay's Raleigh, North Carolina Plant, shipping charges prepaid by the Purchaser. Replacement made under this warranty will be shipped prepaid. Equipment manufactured or supplied by others, sold by Mackay hereunder, and not incorporated in the Equipment manufactured and sold by Mackay hereunder, shall bear only the warranty given Mackay by the manufacturer or supplier of that equipment. Such warranties given Mackay shall be transferred and assigned to the Purchaser on completion of the work and upon final payment to Mackay hereunder.

Exclusions from Warranty - The foregoing warranty is in lieu of and excludes all other expressed or implied warranties of merchantability of fitness or otherwise.

Mackay will not be liable for any special or consequential damages or for loss, damages or expense directly or indirectly arising from the use of the products or any inability to use them, either separately or in combination with any other equipment or material or from any other cause.

The warranty does not extend to any product manufactured by Mackay which has been subjected to misuse, neglect, accident, improper installation or to use in violation of instructions furnished by Mackay.

The warranty does not extend or apply to any unit which has been installed repaired or altered at any place, other than the appropriate Mackay factory, by persons not expressly approved by Mackay, nor to any unit the serial numbers and/or month and year of original date of shipment from Mackay have been removed, defaced, or changed.

The warranty does not extend to fuses that may be used with Mackay products.

ITT MACKAY MARINE
COMPARISON OF SYNTHESIZED RECEIVERS USED TO PROVIDE CONTINUOUS FREQUENCY
COVERAGE FROM 15kHz to 29.9999 MHz

	3020A (690001-000-001)	DEBEG 7200 (690001-000-003)	3026 (690001-000-004)	3028 (690001-000-005)
WIDEBAND	2d Mixer with 8 kHz bandpass 600590-536-001 Filter = 600035-529-001	2d mixer with 6kHz Bandpass 600590-536-002 (Fltr = 600044-529-001	2d mixer with 6kHz Bandpass (600590-536-002 Fltr = 600044-529-001	2d Mixer with 8 kHz bandpass 600590-536-001 Filter=600035-529-001
OUTPUT	600-ohm standard	600-ohm standard	Audio xmfr for bal 600-ohm output (635160-501-001	Audio xmfr for bal 600-ohm output 636160-501-001
PRIMARY POWER	115/230 VAC (2A fuse)	Rear panel with stripped lead pwr cord (230 VAC) (600035-539-002) (Cord = 600059-102-001) 1A Fuse	Rear panel with stripped lead pwr cord (230VAC) (600035-539-004) (Cord = 600059-102-001 1A Fuse	Rear panel with stripped lead pwr cord (230 VAC) (600035-539-003) (Cord=600059-102-001) 1A Fuse
FRONT PANEL	Front Panel = 600034-539-001	Front Panel=600034-539-002 + Handles	Front Panel + Handles 600034-539-003	Front Panel + Handles 600034-539-003
MOUNTING	Desk top console or 19" rack	Desk top console or 19" rack	Desk top console or 19" rack	Desk top console or 19" rack
NAMEPLATE	3020A Nameplate 600207-626-001 on Rear Panel	Nameplate=Debeg 7200 600210-626-001 on Front Panel	EB-3026 nameplate (600208-626-001 on Rear Panel	EB-3028 Nameplate (600209-626-001 on Rear Panel

SECTION 2

INSTALLATION

2.1 CABINET/RACK INSTALLATION

The 3020A Receiver will mount in a standard 19 inch rack, occupying 5 1/4 inches of panel height and 17 inches of depth. "Pem" nuts are provided in side panels for installation of slides.

NOTE

If slides are not used, do not attempt to support the receiver drawer only by the front panel. Provide braces in the cabinet or rack to support the rear of the drawer.

2.2 POWER CONNECTIONS

The input AC power to the 3020A Receiver is 115/230V, 50-60 Hz. A grounded Standard US plug is provided.

CAUTION

Verify that the power transformer is strapped for the correct AC input voltage.

For 115 volt operation, transformer primary windings must be connected in parallel (terminals 1 and 3 must be connected together and terminals 2 and 4 must be connected together). 115V applied to terminals 1 and 4.

For 230 volt operation, transformer primary windings must be connected in series (only terminals 2 and 3 must be connected together). 230V applied to terminals 1 and 4.

Transformer strapping is located on the underside of the receiver chassis and access is gained by removal of the underside rear cover plate.

2.3 OTHER REAR PANEL CONNECTIONS

A terminal block (TB1) is provided on the receiver rear panel for other connections as indicated in table 2.1.

The 600Ω audio output terminals (terminal 1 and ground) and the 3Ω speaker output terminals are provided on terminal block TB1, on the rear panel.

For connection to the 3Ω speaker terminal, disconnect the jumper on the terminal block and connect the external 3Ω speaker between terminal 3 and ground (terminal 2).

NOTE

Removing the jumper disconnects the front panel speaker.

Two spare terminals (5 and 6) are provided on the terminal block.

TABLE 2.1

Terminal Block Pin No.	Available Connection
1	600Ω audio output
2	Chassis ground
3*	3Ω external speaker
4*	3Ω line to front panel speaker
5	Spare
6	Spare

* Terminals 3 and 4 are normally jumpered.

2.4 FUSES

Three fuses (F1, F2, and F3) are utilized in the 3020A Receiver. Fuses F2 and F3 are located on the rear panel. F1 is located on the Regulator PC Card, attached to the inside of the rear panel. Table 2.2 lists the fuses, the ratings and functions.

TABLE 2.2

Designation	Rating (Amp)	Function
F1	1.5	DC fuse following the rectifier bridge and filter for the +28 VDC and +24 VDC circuitry.
F2	1/10*	DC short circuit protection for the +28 VDC and +24 VDC circuitry.
F3	**	Primary AC fuse.

* Slo-Blo.

** 2-amp fuse for 115 VAC operation; 1-amp fuse for 230 VAC operation.

SECTION 3

OPERATING INSTRUCTIONS

3.1 CONTROLS

All controls required for the operation of the 3020A Receiver are counted on the front panel. The function of each is described in the following paragraphs.

Control	Function
Frequency selector switch	Selects receiver tuned frequency in MHz. Consists of six lever-controlled decades, each decade having the digits 0 thru 9, except the most significant decade, which contains only the digits 0, 1, and 2. In all cases, the dialed frequency should correspond to the exact listed frequency of the station being received.
METER DISPLAY RF INPUT/ AUDIO OUTPUT	Toggle switch selects either audio or RF signal strength indication on the front panel meter. The audio display is derived from the rectified audio output, while the RF level indicator is derived from the AGC DC control voltage.
AUDIO GAIN/POWER OFF	Potentiometer controls audio volume and switches AC power on/off.
SPEAKER ON/OFF	Toggle switch used to silence speaker.
RF GAIN/AGC ON	Potentiometer manually adjusts the 92 MHz amplifier gain and the 8 MHz IF amplifiers gain. Also switches the AGC on when the knob is fully counter-clockwise (switched).
PRESELECTOR BAND MHz TUNING	The outer control is a 10-position switch that selects the appropriate tuned frequency range. The inner, variable control provides preselector tuning and is used in conjunction with the RF meter to peak the received input signal. Frequency of tune increases as knob is rotated in clockwise direction.

ANT. ATTEN. IN/OUT	Toggle switch connects an (approximate) 20 dB pad in receiver front end.
PULL FOR FINE TUNE	Potentiometer varies tuning approximately ±100 Hz about dialed frequency when knob is pulled outward.
MODE	Four interlocking pushbutton switches select AM, CW, USB, or LSB. In AM position, the AM detector circuitry is enabled, while the product detector circuitry and the product detector injection are disabled. In the CW, USB, or LBS position, the reverse is the case.
IF BANDWIDTH kHz	Four interlocking pushbutton switches select IF bandwidth of 8 kHz, 2 kHz, 1 kHz, 0.4 kHz. These switches are automatically disabled when USB or LSB is selected.
AGC FAST/SLOW	Toggle switch selects fast or slow AGC release time. Normally, fast AGC is utilized for CW signals and slow AGC for SSB and AM signals.
CW PITCH FIXED/VARIABLE	Toggle switch selects either fixed or variable frequency product detector injection. For CW operation the variable frequency crystal oscillator is utilized for operator pitch control by the associated variable knob. The tuning range is approximately 1 kHz. In the fixed position the product detector injection is provided by the frequency standard and produces zero beat when the incoming CW signal is precisely at the frequency of the frequency select switch.
PHONES	The PHONES jack connects to the 3Ω audio output.

3.2 SSB OPERATION

The 3020A receiver normally is used with the AGC enabled for all modes. The AGC has a large dynamic operating range over which the output is held very constant. Further, the attack time is rapid, allowing for good transient response in SSB and CW modes of reception.

For SSB reception, select USB or LSB. The USB button is normally depressed for Marine SSB service with the CW PITCH switch set to FIXED. In this condition the frequency indicated by the frequency select switches on the front panel is that (of the suppressed carrier) of the station being received.

The frequency of the desired station generally is known and is merely dialed up. In the case where a station frequency is not explicitly known, the band may be scanned with the 1-kHz position of the digit switch, with the receiver in CW mode and the 8-kHz bandwidth button depressed. When a station is found, the receiver may be returned to the normal SSB operating condition by merely depressing the USB button.

Above 4 MHz, the Preselector Range switch is normally left in the WIDEBAND position, as the receiver meets all its sensitivity, image, cross modulation, and spurious response specifications in this mode. For frequencies below approximately 4 MHz, where compromise electrically short antenna systems are most likely to be encountered, some benefit may be obtained by use of the Preselector as a form of impedance matching network to obtain optimum sensitivity. In addition, the preselector is effective in reducing interference from very strong off-frequency signals. The preselector in conjunction with the Antenna Attenuator can cleanup an otherwise unreadable signal.

The AGC switch is usually set to SLOW for SSB reception. This keeps the receiver from "pumping-up" between voice syllables.

3. 3 CW OPERATION

The excellent selectivity characteristics of the 3020A may be more fully exploited in CW operation than in voice types of operation where information bandwidths must be relatively wide.

With CW PITCH control set to FIXED, the frequency select switches again indicate the frequency of the carrier being received when audio output is zero beat. In CW reception the CW PITCH is generally set to VARIABLE position and adjusted for the desired audio pitch by the operator. Note that the 0. 4, 1, 2, or 8 kHz filters are centered on 8 MHz while the USB and LBS filters are set up so that 8 MHz is on the skirts of the filters, typically 20 dB down. For CW operation where the desired station frequency is known explicitly, the frequency select switches are set to that frequency and the 0. 4, 1, 2, or 8 kHz selectivity button depressed. The variable CW PITCH control is then adjusted for the desired pitch.

The USB or LSB filters can be used, of course, for CW reception but in order for the signal to be in the passband of the filter, the frequency select switches must be offset from the exact frequency of the station being received. This is inconvenient from the viewpoint of merely dialing in a desired frequency and normally the sideband filters are not used for CW reception.

3. 4 AM OPERATION

The AM button is depressed in this mode of operation and usually the 8-kHz-wide bandwidth is selected. The frequency select switches are set to the frequency of the desired signal. Reception of fading AM signals is generally enhanced by using either USB or LSB modes, with the CW PITCH control in the FIXED position.

SECTION 4

TECHNICAL DESCRIPTION

4. 1 SIGNAL PATH

a. Block Diagram Analysis

In the following discussion, refer to figure 4. 1.

A signal in the range 15 kHz - 30 MHz enters the preselector, where it passes through an overload protection circuit. At the operator's discretion the signal can pass through either a single-tuned RF circuit tuned to the desired frequency or can be bypassed around this circuit (in the wideband position). The signal then goes through a 40-MHz low-pass filter at the preselector output.

The signal then is fed through a wideband RF amplifier into the 1st mixer, where it is up-converted by the operator-selected synthesizer output to the 92-MHz first IF. The signal from the 1st Mixer is passed through a 20-kHz wide 4-pole crystal bandpass filter centered at 92 MHz and then to the 92 MHz IF amplifier, where it is amplified and passed through another bandpass filter. Delayed AGC voltage is applied to this dual gate FET amplifier. The output of the 2nd 92-MHz filter goes into the diode quad 2nd Mixer, where it is mixed with the 84-MHz second injection signal to produce an 8-MHz signal.

The 8 MHz signal leaves the 2nd Mixer and enters an 8-kHz-wide crystal bandpass filter. (This filter is the narrowest filter in the signal path when the 8 kHz bandwidth is selected by the operator).

The output from this 8-kHz-wide filter is amplified by an 8 MHz IF amplifier, to which IF AGC voltage is applied. The output from the amplifier is routed through an operator selected Information Filter (USB, LSB, 2 kHz, 1 kHz, or 400 Hz) and then applied to the 2nd 8-MHz IF amplifier to be further amplified.

The output from this 2nd 8-MHz IF amplifier stage then is applied to three different detector chains: AM Detector chain, product detector chain, and the AGC chain.

The AM chain consists of an 8-MHz preamplifier and a voltage doubler diode AM detector. These circuits are enabled only when AM operation is selected.

The product detector chain consists of an 8-MHz amplifier/buffer that feeds the product detector. This chain is enabled for all modes of operation other than AM.

The audio outputs from both the AM and Product Detector chains are fed through isolating resistors to a common line feeding the audio preamplifier and thence the audio power amplifier.

The AGC chain consists of an 8-MHz AGC amplifier, a full-wave diode AGC detector, DC amplifiers, and AGC delay circuitry.

b. Preselector

The preselector consists of four parts: Input overload protection circuit; tunable RF circuits; a 40-MHz low-pass filter; and switchable (20 dB) attenuator.

The input overload protection circuit is a diode clipper set to symmetrically clip on peaks greater than approximately 3V. This clipper protects the input of the RF amplifier from destruction by energy from nearby transmitters.

A low-pass filter is incorporated for the range 15-100 kHz. The RF coils tune in 8 ranges from 100 kHz to 30 MHz by means of a front panel adjusted variable capacitor. Below 4 MHz the tuned circuits are top-capacity-input coupled to provide a high impedance input for the type of antennas normally encountered in this frequency range. Above 4 MHz the tuned circuits are designed for 50-ohm antennas.

The 40 MHz low-pass filter provides attenuation for input signals above the 30 MHz top frequency limit of the receiver. A parallel-tuned trap at 92 MHz attenuates energy that might otherwise be able to feed into the first IF of the receiver.

The relay-controlled 20-dB attenuator, switched in at the front-panel of the receiver, minimizes desensitization and cross-modulation caused by strong off-channel undesired signals.

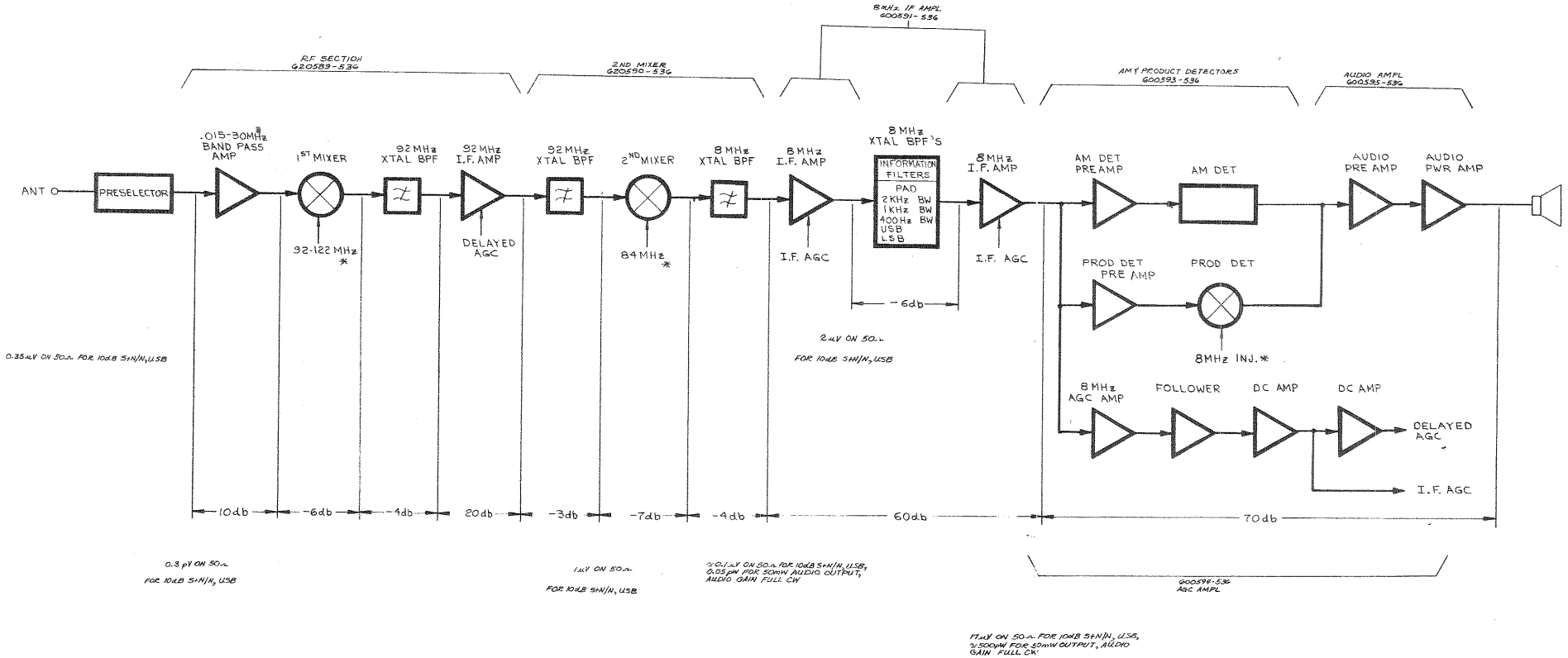
c. RF Section

The RF section card consists of four parts: Wideband RF amplifier; 1st Mixer and local oscillator buffer; 4-pole 92-MHz bandpass crystal filter; and 92-MHz amplifier.

Wideband RF amplifier Q1 is a frequency-compensated power FET operated in the common-gate mode. The low input impedance of the amplifier is transformed to approximately 50 ohms by a broadband input transformer. Output load impedance presented to this stage is set by a second broadband transformer through a peaking network set up to compensate for the output capacitance of the active device. The dynamic range of the RF amplifier from sensitivity to the 1-dB-departure-from-linearity point is in excess of 120 dB.

The 1st Mixer (A1) receives signals from both the RF amplifier and from the synthesizer through the local oscillator common base buffer (Q3). This mixer is a double-balanced (quad) mixer that has a dynamic range of greater than 120 dB. The local oscillator is balanced and the combined signal fed to the crystal buffer.

The combination of the RF amplifier and the doubled-balanced quad has a



* FROM SYNTHESIZER.

0895D529

ITT Mackay Marine
133 TERMINAL AVE. CLARK N.J. U.S.A.

TITLE: BLOCK DIAGRAM (SIGNAL PATH)

SCALE: NONE | 690001 | REV A
APP'D: RD | CHK'D: RD | 028-001

Figure 4.1

dynamic signal-handling capability of about 120 dB.

The 4-pole 92-MHz bandpass crystal filter (FL1) has a 6 dB bandwidth of approximately 20 kHz. It provides protection to the 92-MHz IF amplifier (Q2) by rejecting signals removed 10 kHz or more from the desired signal. Thus, even though a strong signal more than 10 kHz removed from the desired signal can be amplified by the broadband RF amplifier and be up converted in the 1st Mixer, it will be rejected by the 92-MHz filter.

The 92-MHz filter feeds the 92-MHz amplifier (Q2) which is a two-gate FET. This device is a low noise-figure amplifier (3 dB) with delayed AGC voltage applied to the second gate. It is operated in the grounded-source configuration to provide a high input impedance to the 92-MHz filter. The 92-MHz amplifier drives a single Pi-section filter, which matches the amplifier output to the input of the 2nd Mixer card.

d. 2nd Mixer

The 2nd Mixer card consists of three parts: A 2-pole 92-MHz crystal filter; a double-balanced second mixer and local oscillator buffer combination; and an 8-pole 8-kHz-wide crystal filter.

The 2-pole 92-MHz crystal filter (FL2) provides further attenuation of undersired signals ±10 kHz removed from the desired signal.

The 2nd Mixer is a double-balanced mixer that is fed by a local oscillator at 84 MHz through common-base buffer-amplifier Q1.

Output of the 2nd Mixer at 8 MHz is fed to the 8-pole 8-kHz wide crystal filter (FL1). This filter is the only information filter that is used when the receiver is placed in the 8-kHz BW position. The output of the 2nd Mixer is transformed up to the impedance seen by the filter by an L-section (L2 and C2) and the filter looks into the correct output impedance by means of L-section L3 and C3.

e. 8 MHz IF Amplifier

The 8 MHz IF amplifier consists of three parts: Two IC IF amplifiers, and an emitter-follower buffer amplifier.

The first IF amplifier (IC1) receives and amplifies the signal from the 2nd Mixer. The output goes to the Information Filters card where the desired bandwidth filter is selected. The output from the Information Filters reenters the 8 MHz IF amplifier and is amplified by the second amplifier (IC2). Both of these amplifiers have AGC applied to them. The AGC is of the enhancement variety, i. e., the signal-handling capability of the amplifier increases for increasing AGC gain cut.
The output from the second amplifier is fed to the detectors card and to an emitter-follower buffer on the 8 MHz IF amplifier card. This buffer output is available on the rear panel of the receiver.

f. Information Filters

Each filter on the Information Filters card is selected by means of a diode

gate by applying 24 volts to that gate. The filters not selected are automatically shorted out by the diode gates associated with them.

When the 8-kHz button is depressed, a pad rather than a filter, is connected into the circuit, with the amount of attenuation in the pad equal to that found in one of the sideband filters. The total signal path gain is therefore equal for AM or sideband operation.

g. AM and Product Detectors

The AM and Product Detectors card consists of four parts: Product detector preamplifier; product detector; AM detector preamplifier; and AM detector.

The product detector and AM detector preamplifier; (IC1 and IC3) are fed 8-MHz signals in parallel. Only one preamplifier; however, is used at any one time. The appropriate preamplifier is selected by ungrounding either the CW and SSB or the AM command bus. The product detector preamplifier feeds the product detector (IC2) which is an IC balanced mixer. The 8-MHz BFO injection is prevented from feeding back to the 8 MHz IF strip from the product detector by the reverse attenuation of the preamplifier. This prevents the BFO energy from activating the AGC detector.

The AM preamplifier is similar to the product detector preamplifier but has an input level adjustment control (R13) to equalize the audio level between AM and CW/SSB modes.

The output from the AM preamplifier feeds a voltage doubler diode detector (CR1 and CR2) whose output is combined, through an isolating resistor, with the output of the product detector and fed through a common output line to the audio amplifier card.

h. Audio Amplifier

The Audio Amplifier card consists of three parts: Audio preamplifier; audio power amplifier; and meter detector circuit.

Preamplifier Q1 provides audio drive to power amplifier IC1, a power IC with negative feedback to reduce distortion. It operates into output transformer T1 included to match the amplifier to a 3-ohm speaker load. A 560 ohm resistor (R16) provides a 600-ohm output impedance to operate telephone lines.

The meter detector is a full-wave bridge rectifier set up so that one milli-watt into a 600-ohm load indicates 0 dBm on the audio meter.

i. AGC Amplifier

The AGC amplifier consists of six parts: An 8-MHz AGC amplifier; voltage doubler AGC rectifier; emitter follower; IF AGC DC amplifiers; delayed AGC active level shifter; and delayed AGC DC amplifiers.

AGC amplifier IC1 is another IC amplifier, like those used in the 8 MHz IF amplifiers, the AM preamplifier, and the product detector preamplifier. It

provides gain to the voltage doubler AGC detector diodes (CR3 and CR4). The detector is followed by emitter follower Q1, which serves as a low impedance driving source for the 22-μf AGC decay capacitor (C9). Various resistors shunted across the decay capacitor allow variable decay times while the emitter follower driver allows fast attack-time charging of the 22-μf capacitor.

The decay capacitor is followed by complementary-symmetry DC amplifier Q2-Q3, whose output drives the IF AGC line to the 8-MHz IF amplifier.

The IF AGC line drives active level shifter Q4-Q5 with adjustable threshold adjust. This level shifter drives another DC amplifier pair (Q6 and Q7) and provides the delayed AGC voltage to the second gate of the 92-MHz IF amplifier in the RF Section card. The adjustable threshold serves to determine the AGC voltage point at which the 92-MHz IF amplifier begins to cut gain. This delaying of AGC voltage to the 92-MHz IF amplifier is necessary to ensure that the signal-to-noise ratio is not degraded with AGC action at medium input signal levels, where noise figure degradation in the front end must be avoided. AGC action to the 92-MHz IF amplifier acts in a reverse direction from the 8-MHz IF amplifier in that gain is decreased as the AGC voltage falls below 8.2 volts.

j. Variable BFO

The variable BFO consists of an 8-MHz Pierce crystal oscillator (Q1) followed by an emitter follower buffer stage (Q2). A switch built into the BFO RF-tight (shielded) compartment switches between the output of this variable BFO and the output of the fixed 8-MHz BFO (derived from the 8-MHz standard) and passes the signal on to the product detector.

In the AM mode Vcc to the variable BFO is disabled. The crystal oscillator frequency is pulled by means of variable capacitor C4 in the BFO compartment.

k. Regulator

The regulator consists of six parts: Transformer; bridge rectifiers (14 and 55 volts) and filter capacitors; 38V pre regulator system; 38V pre regulator current overload protection system; +28V regulator system; +24V regulator system; and +5.6V regulator system.

Transformer T1 supplies power to both the +55V (CR1) and +14V (CR2) bridge rectifiers and their associated filter capacitors.

The IC regulators for the +28V (IC1) and +24V (IC2) power systems can operate with a maximum input voltage of +40V. It is desirable to provide a degree of pre-regulation to these high current medium-voltage supply systems as well as to lower their input voltage. Thus, the pre-regulator system of Q3, Q4, CR4 and associated circuitry is used. This pre-regulator circuit uses a simple Darlington-connected series-pass regulator with a base voltage set by zener CR4.

In the event of a current overload on either the +24V or +28V line, transistors

Q1 and Q7 begin conducting (the voltage drops across R1 and R15, cause them to conduct) in turn, causing Q6 to conduct. Q6 bleeds the base drive from the Q3-Q4 pair and prevents damage. This action starts for currents on either line exceeding approximately 1 ampere. Transistor Q6 puts a heavy current through slow-blow fuse F2 and if the overload lasts for longer than approximately 20 seconds the fuse will blow.

4. 2 SYNTHESIZER

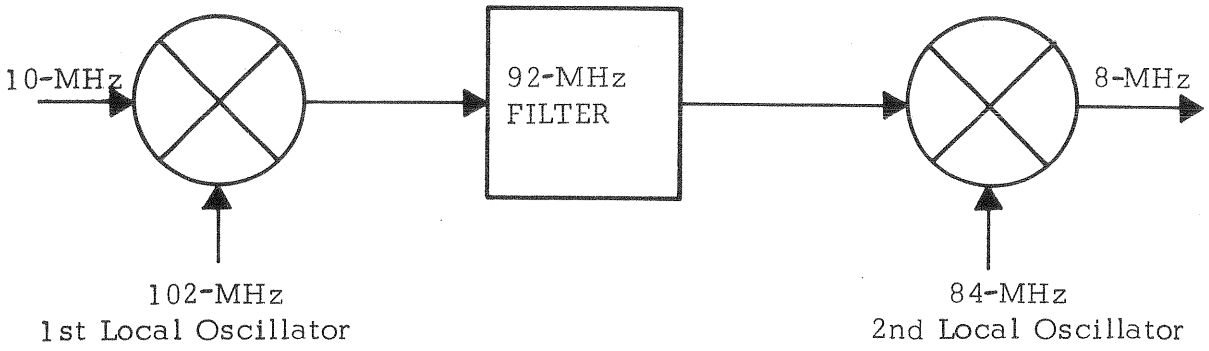
a. Block Diagram Analysis

In the following discussion, refer to figure 4. 2.

The synthesizer in the ITT Mackay Marine 3020A receiver consists of two programmable phase-locked loops. One loop, the Minor Loop, is controlled by the 100-Hz 1-kHz and 10-kHz positions of the front-panel frequency-select switches. The other loop, the Major Loop, is controlled by both the output of the first loop and the settings of the 100-kHz 1-MHz and 10-MHz frequency-select switches.

Both the minor and major loops are phase-locked to a 8-MHz temperature compensated crystal oscillator standard, although in the interface between the two loops a conversion oscillator (84 MHz) is used that is not phase locked to the standard. Since this 84 MHz provides the injection to the 2nd Mixer in the receiver signal path, and since the output of the synthesizer provides the injection to the 1st Mixer in the signal path, the over-all receiver becomes drift cancelled; that is, any shift in the 84-MHz oscillator away from exactly 84 MHz is compensated for in the system on a cycle-for-cycle basis.

For example, assume that a signal of 10 MHz is to be received. The first local oscillator frequency should be 102 MHz, the second local oscillator frequency should be 84 MHz and the final output IF frequency will be 8 MHz as indicated in the following illustration.



3020A Mixer Scheme.

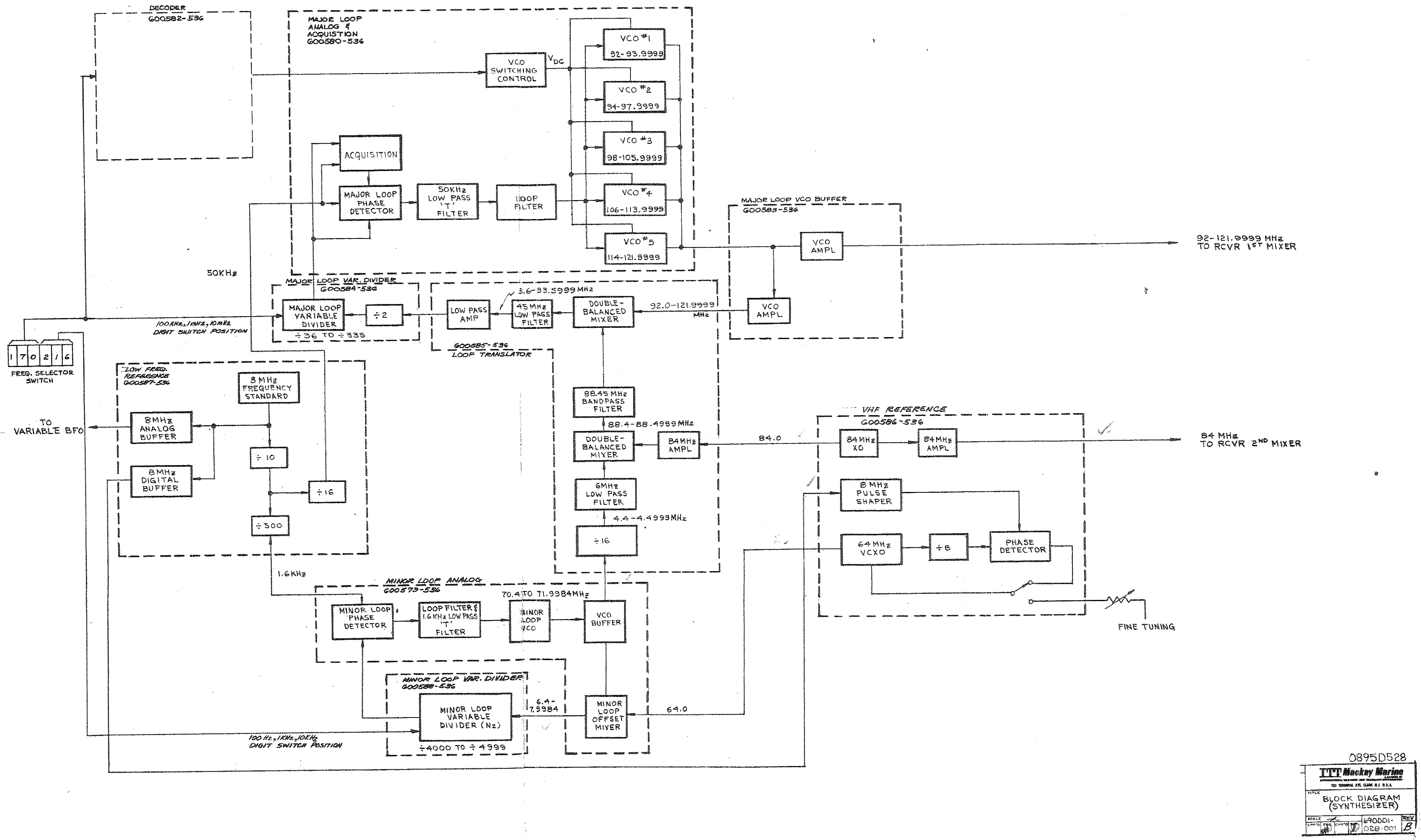

DECODER
G00582-536
MAJOR LOOP
ANALOG &
ACQUISTION
G00580-536
VCO SWITCHING CONTROL
V_{DC}
VCO #1
92-93.9999
VCO #2
94-97.9999
VCO #3
98-105.9999
VCO #4
106-113.9999
VCO #5
114-121.9999
ACQUISITION
MAJOR LOOP PHASE DETECTOR
50KHz LOW PASS 'T' FILTER
LOOP FILTER
MAJOR LOOP VCO BUFFER
G00583-536
VCO AMPL
VCO AMPL
92-121.9999 MHz
TO RCVR 1ST MIXER
50KHz
MAJOR LOOP VAR. DIVIDER
G00584-536
MAJOR LOOP VARIABLE DIVIDER
÷36 TO ÷335
÷2
LOW PASS AMP
3.6-33.5999 MHz
45 MHz LOW PASS FILTER
DOUBLE-BALANCED MIXER
92.0-121.9999 MHz
G00585-536
LOOP TRANSLATOR
100KHz, 1MHz, 10MHz
DIGIT SWITCH POSITION
1 7 0 2 1 6
FREQ. SELECTOR SWITCH
LOW FREQ. REFERENCE
G00587-536
8 MHz FREQUENCY STANDARD
8MHz ANALOG BUFFER
8MHz DIGITAL BUFFER
TO VARIABLE BFO
÷10
÷16
÷500
88.45 MHz BANDPASS FILTER
88.4-88.4999 MHz
DOUBLE-BALANCED MIXER
84MHz AMPL
84.0
6MHz LOW PASS FILTER
4.4-4.4999MHz
÷16
VHF REFERENCE
G00586-536
84MHz XO
84MHz AMPL
84 MHz
TO RCVR 2ND MIXER
8 MHz PULSE SHAPER
64MHz VCXO
÷8
PHASE DETECTOR
FINE TUNING
1.6KHz
MINOR LOOP ANALOG
G00579-536
MINOR LOOP PHASE DETECTOR
LOOP FILTER & 1.6KHz LOW PASS 'T' FILTER
70.4 TO 71.9984MHz
MINOR LOOP VCO
VCO BUFFER
MINOR LOOP VAR. DIVIDER
G00588-536
MINOR LOOP VARIABLE DIVIDER (Nz)
÷4000 TO ÷4999
6.4-7.9984
MINOR LOOP OFFSET MIXER
64.0
100Hz, 1KHz, 10KHz
DIGIT SWITCH POSITION
0895D528
ITT Mackay Marine
BLOCK DIAGRAM (SYNTHESIZER)
690001-028-001
REV B

Figure 4. 2

If the second local oscillator frequency happens to be 84.002 MHz, the first local oscillator becomes 102.002 MHz.

The conversion then becomes 10.0 MHz to 92.002 MHz, and 92.002 MHz back to 8.000 MHz. The receiver has thus compensated for the slight change in the 84 MHz frequency and will do so as long as the signal remains within the ±10 kHz passband of the 92 MHz first IF filters.

The minor loop produces 999 steps from 70.4000 to 71.9984 MHz at its output. The output frequency is mixed with a 64-MHz signal phase-locked to the 8-MHz crystal standard to yield a range from 6.4000 to 7.9984 MHz. (The 64-MHz crystal oscillator may be taken out of phase-lock mode and allowed to run free. The frequency can be pulled to provide fine tuning.) This output is divided by a divisor ratio between 4000 - 4999 to yield a 1.6 kHz output. This 1.6 kHz is compared in a phase detector to 1.6 kHz derived from the 8 MHz crystal standard. If a difference occurs between the output from the variable divider and the 1.6-kHz reference the loop adjusts the frequency until no error occurs. For example, suppose a dial setting of the frequency-select switches is chosen and the divisor ratio is 4100. The VCO will adjust itself until

$$\frac{(x - 64\ \text{MHz})}{4100} = 1.6\ \text{kHz}, \quad \text{or } x = 70.560\ \text{MHz}.$$

The major loop produces, for any particular minor loop output frequency, 30 steps in its output. The output of the major loop varies from 92.0000 to 121.9999 MHz (with a 92.0000 MHz first IF this yields a receiver frequency range from 0 - 29.9999 MHz).

The major loop takes the 70.4 to 71.9984 MHz output from the minor loop and first divides it by 16 to yield a range from 4.4 to 4.4999 MHz. This range of frequencies then is mixed with the output of an 84-MHz crystal oscillator (as already discussed) to yield a range from 88.4 to 88.4999 MHz. This range then is used to mix with the output range of the major loop, thus producing a range from 3.6 to 33.500 MHz.

This frequency range then is fed to a variable divider, which divides by 2 and then by 36 to 335. If the loop is at the right output frequency, the final result of all these manipulations is an output from the variable divider at 50 kHz, the sampling frequency of the major loop. The output of the variable divider is compared to a 50-kHz pulse train derived from the 8-MHz crystal standard.

For example, if the minor loop output frequency is 70.560 MHz, as in the previous example, this divided by 16 yields: 70.560/16 = 4.410 MHz. This is mixed with 84.0 MHz to yield 88.410 MHz. If the variable divider is programmed to divide by 100 ($\div 2$, $\div 50$), then the output frequency will be

$$\frac{x - 88.410}{100} = 50\ \text{kHz}, \quad x = 93.410\ \text{MHz}.$$

(This means: 93.410 - 92.000 MHz IF = 1.410 desired reception frequency.)

b. Low Frequency Reference

The purpose of the Low-Frequency Reference is to provide 1.6 kHz, 50 kHz, and 8 MHz reference pulses for the minor loop, major loop, and the VHF Reference, respectively. 8-MHz energy also is provided for the fixed BFO output.

The output from temperature-compensated crystal-standard Y1 is buffered in Q1 and fed to the 8-MHz fixed BFO. It is also buffered by Q2 and Q3 and fed into a digital buffer (the inverters in ICA) at TTL level to feed the VHF Reference card.

IC1 and IC2 divide 8 MHz by 10 and then by 16 to yield a 50-kHz output. A 1.25-μsec-wide pulse at a 50-kHz rate is provided from gate B decoding from IC2. A positive rising and negative falling output pulse is provided for the major loop phase detector at 50 kHz.

The 800-kHz output from IC1 is fed to IC3, then IC4, and IC5, which form a divide-by-500. This yields a 1.6-kHz output frequency. Gates C and A decode the various dividers to produce a 1.25-μsec-wide output pulse at a rate of 1.6 kHz. A positive rising and negative falling output pulse are provided to the minor loop phase detector at 1.6 kHz.

c. VHF Reference Card

The purpose of the VHF Reference card is to provide an 84-MHz output signal for the Loop Translator card and for the signal path 2nd Mixer and to provide a 64-MHz output that is phase-locked to the 8-MHz standard for the minor loop analog card.

The VHF Reference card contains five parts: An 84 MHz crystal oscillator and buffer; a 64 MHz crystal oscillator; an analog-to-ECL (emitter coupled logic) level 64 MHz buffer; an ECL divide-by-8; and a phase detector/DC control system for the 64-MHz phase-locked loop.

The 84-MHz oscillator (Q2) is a modified Colpitts crystal oscillator fed into a FET buffer (Q1) and then to the signal path.

The 64-MHz oscillator (Q3) is another modified Colpitts crystal oscillator, but one whose frequency is pullable by means of varactor CR1. The 64-MHz oscillator can be phase-locked to the 8-MHz standard, or can be allowed to run free. Voltage applied to CR1 can be used to fine tune the receiver over the range ±100 Hz, approximately.

In the phase-lock mode the 64-MHz oscillator is followed by buffer Q4-Q5, which converts the analog 64 MHz signals to emitter-coupled logic (ECL) levels to drive the ECL high speed divide-by-8 counter comprised of IC4 and IC5. This divide-by-8 produces 8 MHz pulses that are fed to low-pass filter C40, L8, and C41.

The filtered 8 MHz is then fed to the phase-detector/DC control system, IC3, which is a cascode mixer type of phase-detector. 8 MHz energy from the Low-Frequency Reference is also fed to IC3. The DC output from IC3 goes to the varactor CR1 through the fine-tune enable relay to complete the loop.

d. Minor Loop Analog

The Minor Loop Analog card consists of four parts: The minor loop offset mixer and 64 MHz buffer, the 70.4 - 71.9984 MHz VCO (voltage controlled oscillator) and buffer; the minor loop sample-and-hold phase detector; and the loop filter/1.6 kHz T-notch filter.

The minor loop offset mixer is an IC cascode mixer, IC2, which is fed local oscillator power through the 64-MHz buffer, Q11, which, in turn is fed from the VHF Reference card. The buffered output of the 70.4 to 71.9984 MHz VCO (buffered by IC3) is also fed to the mixer, and the 6.4 - 7.9984 MHz difference output from the offset mixer is fed to the minor loop variable divider.

The VCO is a form of Hartley oscillator whose frequency can be changed by varying the voltage across the varactor diodes CR4 and CR5. IC3, a cascode amplifier, buffers the VCO and feeds 70.4 - 71.9984 MHz energy both to the divide-by-16 on the Loop Translator card and to the minor loop offset mixer.

The minor loop sample-and-hold phase detector system consists of Q1, Q2, Q3, Q4, Q5, Q6, and Q7.

The ramp capacitor C15 is charged by the constant current generator Q2 and is discharged by the ramp switch Q1 triggered by the 1.6 kHz reference pulse. Sometime during the rise of the ramp voltage the output from the minor loop variable divider pulses-on sampler gate Q6 and Q7 for a short period of time. At this time energy is transferred from the sampler driver system Q3, Q4, and Q5 to the sample capacitor C18.

The DC amplifier composed of Q8, Q12, and Q9 amplifies the voltage across the sampler capacitor and applies it to the loop filter (R4, R5 and C3) and then to the 1.6 kHz T-notch filter (R37, R36, R38, and C20, C21, C22, and C24). The filtered DC is then applied to the varactors CR4 and CR5.

The principle of this phase lock system is that if successive voltage samples are not the same, the frequency is wrong and must be changed by the loop until successive samples are the same.

Diodes CR7 and CR8 serve to short the loop and notch filters for large voltage swings and thus serve to decrease the time to achieve acquisition of phase lock.

e. Minor Loop Variable Divider

The minor loop variable divider is made up of four programmable decade divider IC's and their associated decoding gates. Basically, the divider is preloaded with a number from the frequency-select front-panel switches (100 Hz, 1 kHz, 10 kHz switches) and counts down to zero. (The digit switch gives out a ground to indicate a "1" condition.) When the output recognizes a count of BCD 0000, a pulse is sent to the load-data input which allows the 4 ICs to be preset again. At each load-data point the last decade counter is preloaded to BCD 4.

For example, when the frequency select switches are set to 10 kHz = 0, 1 kHz = 0, and 100 Hz = 0, the counters are preset to ICA = 0000, ICB = 0000, ICC = 0000, and ICD =0010. The counter counts down pulses, at which point the counters are in the state ICA = 0000, ICB = 0000, ICC = 0000. ICD = 0000. This enables all the gates, and presets all the counters once again. Thus the variable counter in this case divides by 4000.

When the frequency select switches are set to 999 the counters are preset to ICA = 1001, ICB = 1001, ICC = 1001, and ICD = 0010. The counter counts down 4999 pulses. At this point the states are again all 0's, the gates are all enabled, and all the counters are preset once again. Thus, the variable counter in this case divides by 4999.

f. Loop Translator

The function of the Loop Translator is basically to allow the output of the minor loop to help control the ultimate frequency the major loop assumes.

The Loop Translator consists of three parts: The divide-by-16 and associated 6-MHz low-pass filter; the 88.4 - 88.4999 MHz double-balanced mixer, associated 84-MHz local oscillator buffer amplifier, and 88.45 MHz bandpass filter, and buffer amplifier.

The 70.4 -71.9984 MHz signal from the Minor Loop Analog card enters the Loop Translator, where it is buffered through an emitter-follower Q1 to ECL levels and then divided by 16 in the high speed four stage ECL divider contained in IC1 and IC2. The 4.4 - 4.4999 MHz output from the divider chain is buffered in Q2 and passed through a 6-MHz elliptical low-pass filter. It then goes to a double-balanced diode quad mixer. This mixer is fed from an FET buffer amplifier Q5, in turn fed from the 84-MHz output of the VHF Reference card.

The resultant 88.4 - 88.4999 MHz output from the mixer is filtered in a four-section bandpass filter centered on 88.45 MHz. The output from this filter feeds another double-balanced quad mixer (A1), whose local oscillator is the buffered output from the main loop VCO, from 92.0 to 121.9999 MHz. The output of this mixing action is from 3.6 - 33.5000 MHz.

This range passes through an elliptical 45-MHz low-pass filter consisting of C28, C34, C35, and L9, to amplifier IC3, where it is amplified and fed to another buffer Q3 and Q4. This buffer has a TTL-level output signal which feeds the Major Loop Variable Divider card.

g. Major Loop Variable Divider

The function of the Major Loop Variable Divider is to divide by N, where N is an even integer from 72 to 670; i.e., 72, 74, 76, 78 ... 670.

Since the counter counts even integral numbers a divide-by-two (ICA) precedes the actual programmable portion of the counter.

The frequency range fed to the variable counter card is 3.6 - 33.500 MHz. The range fed to the programmable portion of the variable counter (consisting of ICF, ICG, and ICH) is 1.8 -16.75 MHz. The IC's used in the programmable

portion of the variable counter have maximum counting rates just above the top end of this range, and the time delays involved in the presetting and count recognition process can be longer than the time between successive input pulses.

For this reason of excessive time delays, a side counter consisting of ICA and ICB fed in parallel with the programmable counters is used. This side counter is inhibited until the programmable counters have counted down from the number preset into them (from the frequency select switches) to the decimal number 166. The decoder gates at the programmable counter outputs then cause the side counter to start.

Once the side counter begins, further input pulses to the programmable counters are inhibited through gate K. Further, once the side counter starts, the programmable counter is allowed to preset. The side counter counts two pulses and then stops. The programmable counter then is again enabled, to begin the cycle over again.

In short, the operation proceeds as follows: The programmable counter counts $(\frac{N}{2}-2)$ pulses, where N is the desired divisor ratio and the divide-by-2 factor is due to the divide-by-2 preceding the programmable counters. The side counter begins at this point and counts a total of 2 pulses (4 pulses at the input to the card). When the side counter starts, the programmable counter is stopped and is preset to the number $(\frac{N}{2}-2)+166$ again. After the side counter has counted a total of 4 input pulses, the programmable counter starts again and goes through the cycle once again.

It can be seen then that the presetting function is given ample time to be performed properly by the action of the side counter.

A divider operation is illustrated in the following example. Suppose the desired frequency is 0.00 MHz. The desired N for the over-all counter is 72. The programmable counter must be preset to

$$(\frac{N}{2} - 2) + 166 = \frac{72}{2} - 2 + 166 = 200$$

The output of the frequency-select switches on the receiver front-panel is in the BCD code, the same code which the programmable decade counter that ICF, ICG, and ICH use. The 10-MHz output, however, is offset by 2; i.e., BCD 0 = 0000 becomes 0100 because of the offset. Thus, 10 MHz = 0100, 1 MHz = 0000 and 100 kHz = 0000 comes to be 200, preset into the programmable counters when the data-load input (pin 11 of each IC) is made low. In other words, the counters have been preset to 200 when the desired N is 72.

The programmable counters count down from 200 when gate K is enabled; i.e., after the side counter stops counting. They count down 34 pulses (68 pulses into the input ÷ 2). At this point the decoder gates are all enabled, and a logical 0 appears at pin 6 of gate J. This causes ICA pin 9 to go low, thereby preventing further pulses from entering the programmable counter (at pin 4, ICF) through gate K, and also causing the presetting to 200 to occur (data-load command is given to the decader-counters).

Gates L (pins 9 and 8) and M (pins 1, 2, 4, 5, and 6) delay the input signal to ICB (pin 13) referenced to the input signal to ICA (pin 5). This delay allows ICA to control the actions of the J-K flip-flop ICB. ICB produces an output pulse two input pulses after the decoder output has arrived. In other words, the ICA/ICB combination counts for 2 pulses after it has been enabled.

ICC (flip-flops associated with pins 12 and 9) and ICD lengthen the output pulse from ICB to a length useful for the input to the phase-detector on the Major Loop Analog card.

h. Decoder

The synthesizer in the 3020A covers 92-121.9999 MHz in five ranges with five switchable VCOs: VCO No. 1: 92.0 - 93.9999 MHz; VCO No. 2: 94.0 - 97.9999 MHz; VCO No. 3: 98.0 - 105.9999 MHz; VCO No. 4: 106.0 - 113.9999 MHz; VCO No. 5: 114.0 - 121.9999 MHz.

The function of the decoder board is to decode the front-panel frequency-select switches and enable the particular VCO whose output frequency corresponds to the dialed frequency.

i. Major Loop Analog and Acquisition

The Major Loop Analog and Acquisition card consists of five parts: Sample-and-hold phase detector system; acquisition system (frequency discriminator); 50-kHz T-notch filter and loop filter; five VCOs and the VCO switching control system.

The sample-and-hold phase detector system is very similar to that found on the Minor Loop Analog card, with the exception that the time constants are set for a 50-kHz sampling rate rather than the 1.6-kHz sampling rate found in the minor loop.

The ramp capacitor C26 is charged by the constant current generator (Q8) and is discharged by switch Q7, when Q7 is triggered by a 50-kHz reference pulse. Sometime during the rise of the ramp voltage the output from the major loop variable counter pulses-on the sampler gate (Q11 and Q12). This causes energy transfer from the ramp capacitor through buffer amplifiers Q9, Q5, and Q10, to sampler capacitor C19.

The DC amplifier (Q13 and Q6) amplifies the voltage across the sampler capacitor and applies this amplified voltage to the 50-kHz T-notch filter, consisting of C20, C12, C13, C28, and R31, R32, R20, and R33. The purpose of this notch filter is to remove residual 50-kHz energy that appears as ripple on the DC amplifier output.

The output from the notch filter is applied to the loop filter, (R46, R37, and C33) and then to the VCO varactor control lines.

In sum, the principle of the phase-lock system is that if successive voltage samples to the sampler capacitor are not the same, the frequency is wrong and must be changed by the loop until the levels of successive samples are the same.

Because of the relatively large frequency ranges covered by the major loop VCOs; however, a means must be employed to prevent false locks; that is, loop lock-up when phase detector input frequencies are harmonically related. An acquisition circuit, consisting of flip-flop IC3, IC4, IC5, and associated gates, recognizes pulse interlace between the reference pulses and the output from the Major Loop Variable Divider ($\div$ N) card. If in between every two reference pulses there is one and only one $\div$ N pulse, the frequency of the two pulse trains is the same. If pulse interlace does not occur the acquisition circuit causes the end of the ramp capacitor to go either to ground or to +5V. When the ramp is sampled, the resulting lower or higher voltage causes the VCO frequency to shift off the offending false-lock point. Flip-flops IC4 and IC5 serve to length the output pulses out of the discriminator system to give the VCO time to move off the false-lock point.

The five VCO's all operate in a form of Harley configuration whose frequency is changed by varying the voltage on the varactor control line.

The VCO for the desired frequency range is selected by applying a logical 0 to the control input of the desired VCO. This enables the switching transistor associated with that VCO, and then the VCO.

j. Major Loop VCO Buffer

The VCO output of the major loop is fed to two places: The local oscillator input of the 1st Mixer in the signal path, and also to the input to the Major Loop Variable Divider via the loop translator. However, the 1st Mixer must be materially free of digital switching noise from the variable divider contaminating its local oscillator signal. The Major Loop VCO Buffer thus has two amplifier chains (with good reverse attenuation characteristics) fed in parallel but feeding the two different output loads.

Good reverse attenuation (that is, failing to pass a signal that might appear at its output backwards to its input) is achieved with three common-base wideband transformer-coupled transistor stages per amplifier.

SECTION 5

GENERAL SERVICE INFORMATION

CAUTION

The 3020A is entirely solid state, and therefore routine periodic maintenance is not required. No attempt should be made to "touch-up" the equipment unless specific operational difficulties are encountered.

5.1 INTRODUCTION

The ITT Mackay Marine 3020A receiver is highly modularized, with approximately 90 percent of the circuit components on plug-in cards. This makes most troubleshooting a matter of simply isolating and replacing a faulty card. Repairs to the defective card preferably should be done at the factory, but can be done in the field by trained personnel familiar with 3020 equipment.

The receiver can be broken up into three functional parts: The signal path; the synthesizer; and the power supply. The power supply is common to both signal path and synthesizer circuits.

A failure in the synthesizer may be difficult to isolate since the correct output frequency from the synthesizer is the result of the complex interaction of eight cards. If any one of those cards becomes defective the synthesizer may "break lock;" that is, not achieve phase lock at the desired frequency.

5.2 SIGNAL PATH

A defective card in the Signal Path may generally be found by proceeding from the speaker to the front-end, introducing signal generators tuned to the appropriate frequency at each point and listening for the presence or absence of audio output.

For example, assume that a malfunction occurs in the 2nd Mixer card and the desired signal is completely lost. The start of a typical service procedure would be to listen for IF noise in the speaker with the audio and RF gain controls advanced. The presence of noise would indicate that the audio amplifier chain at least is functional. The next step would be to insert a signal generator tuned to 8 MHz at the input to the 8 MHz IF Amplifier card to see whether a signal can be put through the IF and detector chains. In this case a signal can indeed be fed down this chain.

The next step in the signal path tracing would be to put a signal at 92 MHz into the 2nd Mixer card. In our example no signal could be forced down the

receiver at this point, and this fact would show that a failure exists somewhere between the input to the 2nd Mixer card and the input to the 8 MHz IF Amplifier card. Replacing the 2nd Mixer card with a known good one should restore the receiver to operation.

A chart of the signal levels required for 10 dB S + N/N audio output at various points in the signal path is given in figure 4. 1, along with the conditions necessary for these measurements. Further gain and level information is available from the block diagram.

5. 3 SYNTHESIZER

Most of the cards in the synthesizer contain high-speed digital integrated circuits. The operation of these can be observed best with the aid of a high frequency oscilloscope, which has a frequency response out of at least 100 MHz, and one which has high frequency external triggering capability. (A familiarity with the operation of TTL digital circuitry is almost essential.) The gates used are primarily of the NAND, AND, and INVERT variety. Truth tables for the IC logic block are given in figure 5. 1.

When the minor loop is locked, the voltage at the junction of R39, C24, C21, and R38 on the Minor Loop Analog card should be stable and within the range of 9 to 13 volts at frequency extremes of 00000. 0 to 00999. 9 kHz. When the minor loop is not locked, the voltage at the above point will not be a DC voltage but rather a slowly varying voltage as the loop searches for lock.

Two pulses that must be present before the minor loop can lock are the outputs (both positive and negative-going) from the minor loop variable divider, and the positive-and negative-going 1. 6 kHz reference pulses. These pulses are standard TTL logic level pulses (0 to 3 volts) and are approximately 15 μsec wide.

Another waveform that must be present before the minor loop can lock is the ramp voltage, found at the junction of the collectors of Q1 and Q2 and C15. This is a sawtooth wave going from 0 to 7 volts in 625 μsec.

The loop can be made to run "open-loop" if the end of resistor R39 connected to C24, C21, and R38 is lifted from the board and connected to a variable voltage power supply. As the voltage is swung between 9 and 13 volts the output frequency of the VCO should swing between 70. 4 and 71. 9984 MHz.

If the Minor Loop Variable Divider is working properly, the number of output pulses in a given time period will vary as the frequency is varied by changing the varactor voltage.

Further, if the sampler and DC amplifiers are working properly (and the loop locked when run closed-loop) the voltage appearing at the point where R39 was lifted from the board should be the same as the voltage applied to the varactors from the variable power supply.

TRUTH TABLES: 3020 A

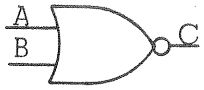
0= 0 Volts (TTL Low)
1= 3 Volts (TTL High)

NAND

A	B	C
0	0	1
0	1	1
1	0	1
1	1	0

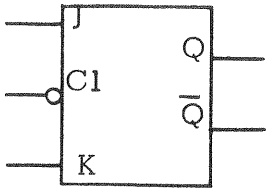
AND

A	B	C
0	0	0
0	1	0
1	0	0
1	1	1



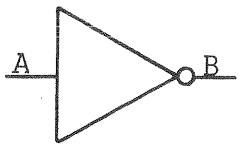
NOR

A	B	C
0	0	1
0	1	0
1	0	0
1	1	0



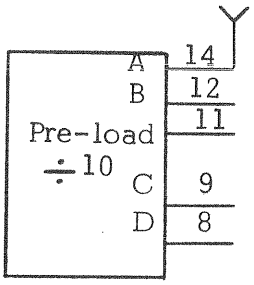
J-K Flip-Flop

J	K	Cl Pulse	QN + 1	
0	0	0	QN	Inhibit
0	1	0	0	Clear
1	0	0	1	Set
1	1	0	$\overline{QN}$	Toggle



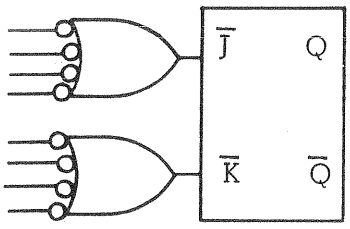
Inverter

A	B
0	1
1	0



÷ 10

A	B	C	D	BCD No.
0	0	0	0	0
1	0	0	0	1
0	1	0	0	2
1	1	0	0	3
0	0	1	0	4
1	0	1	0	5
0	1	1	0	6
1	1	1	0	7
0	0	0	1	8
1	0	0	1	9
0	0	0	0	0



J-K ECL Flip-Flop

$\overline{J}$ ND	$\overline{K}$ ND	$\overline{CD}$	QN
0	0	1	$\overline{QN}$
0	1	1	1
1	0	1	0
1	1	1	QN

CD= One $\overline{J}$ and one $\overline{K}$ tied together
ND= Not defined

Figure 5. 1.

The major loop, of course, cannot be locked to the correct frequency if the minor loop is not at the right frequency. If the minor loop is locked but the major loop still is not, test for the presence of both negative and positive-going reference and major loop variable divider output pulses, just as for the minor loop.

Again, just as for the minor loop, a ramp is necessary for the major loop to function. However, due to the action of the acquisition (frequency discriminator) circuitry the ramp when the loop is out of lock can start at either 0 or roughly 5 volts, depending on the state of the output stage of IC5 on the Major Loop Analog and Acquisition card. The ramp is capable of rising to roughly 5 or 10 volts depending on whether it is started from 0 or 5 volts. When the loop is locked the ramp goes from roughly 5 to 10 volts.

The major loop can be run "open-loop" if CR20, CR21, and R46 are removed from the card and a variable power supply is connected to the junction of R37, R47, R48, R49, R50, and R60.

If the loop is run open-loop the acquisition circuitry will tend to cause confusing symptoms and it should be disabled. This cannot be done easily, but can be effected if ICL is removed from the board. The ramp will then travel between 5 and 10 volts.

NOTE

On sets having R61 and C52 on Major Loop Analog board, the acquisition circuit can be disabled by connecting a jumper from junction of these components to +5 volts.

The Frequency Translator card contains 4 different frequency ranges, since it contains 2 different frequency mixes and a ÷16. Analysis of this card is difficult without either a frequency selective voltmeter or a spectrum analyzer.

The two variable dividers, the Major and Minor Loop Variable Dividers, can be confusing to troubleshoot owing to the high-speed digital circuitry used. Defects can be spotted by externally synchronizing the scope to the slowest pulse in a suspicious area and observing the various command pulses that should be causing that output pulse. For example, the decoder output on the Major Loop Variable Divider available at Pin 6 of ICJ can be used to synchronize the scope while the outputs of the programmable dividers ICF, ICG, and ICH are observed.

SECTION 6

CARD TEST AND SETUP INSTRUCTIONS

6.1 INTRODUCTION

Many of the printed-circuit cards used in the 3020A have no adjustable components on them. For example, the variable divider cards are completely digital, with no tuning adjustments of any sort.

The cards that do have adjustable components should not be adjusted indiscriminately, especially without the availability of test equipment. The cards are properly adjusted as they come from the manufacturer's plant. The adjustable components have silicone rubber cement on them to lock their settings, and should not require readjustment or touchup unless major components are replaced. Such major component replacement normally should be performed at the factory, where proper realignment is done as a matter of course.

6.2 SIGNAL PATH ADJUSTMENTS

As mentioned previously, cards are adjusted properly as they come from the Manufacturer's plant. "Touchup" or "optimization" alignment is discouraged, as the possibility of enhancing performance of the receiver slightly is far overshadowed by the probability of badly misaligning the receiver.

Only highly qualified personnel should attempt the following alignment procedures, and then only with the use of adequate test equipment.

a. RF Section Alignment (Refer to RF Section Schematic Diagram, Page 7.1)

1. Set up receiver as follows:
   a. AGC Off, RF Gain fully clockwise.
   b. 8.0 kHz IF Bandwidth.
   c. Mode: CW.
   d. Preselector: Wideband.
   e. Antenna Attenuation: Out.
   f. Fine Tune: Pushed in.
   g. Audio Gain: Comfortable level.
   h. Speaker: On.
   i. RF Voltmeter with 50-ohm termination at rear panel IF Output.
2. Connect voltmeter between junction of R1 and R2 and ground. Adjust R1 for 0.4 VDC. This level corresponds to 40 ma of drain current thru Q1.
3. Introduce signal at 5.005 MHz at a 5 μV level, and tune generator into antenna jack for zero beat. Set RF meter on .03 volt scale.

Put RF Section card on extender card, and tune L4 and L5 for maximum output.

NOTE

The 92 - 122 MHz Synthesizer input to RF section is approximately 400 mV rms. Delayed AGC voltage goes between about 8.2 Volts at Maximum RF gain to 1.4 volts with RF Gain fully counterclockwise.

b. 2nd Mixer Alignment (Refer to 2nd Mixer Schematic Diagram, page 7.3)

1. Set up receiver as for RF Section Alignment 1.
2. Test 8 kHz wide passband response: Introduce signal into receiver tuned to 5.005 MHz at a 5 μV level and tune for maximum level on RF voltmeter connected to IF Output jack. While observing RF voltmeter, change receiver 1 kHz digiswitch until output drops 6 dB. The upper and lower -6 dB points frequencies should be greater than 8.0 kHz apart, and the passband ripples should be less than 3 dB. If these conditions are not met L2 and L3 must be adjusted.
3. The tuning of L2 and L3 has a major effect on the bandwidth and the passband ripples in FL1.

   L2 and L3 can most easily be adjusted with use of a sweep generator. (They can be adjusted alternatively; however, by a "cut and try" method, tuning first one and checking the passband, then the other, until the passband shape and width are satisfactory.) A sweep generator that can be set to a center frequency of 10 kHz and that can be adjusted to a sweep width of about 10 kHz is necessary, as is an oscilloscope with external sweep input terminals, and with a 30 mV/centimeter sensitivity at 8 MHz.
4. Set receivers up as follows:
   a. AGC: On.
   b. IF Bandwidth: 8 kHz.
   c. Mode: CW.
   d. Preselector: Wideband.
   e. Antenna Attenuation: Out.
   f. Fine Tune: Pushed In.
   g. Audio Gain: Comfortable Level.
   h. Speaker: On.
   i. Oscilloscope connected to IF Output jack on rear panel.
   j. AGC: Slow.
   k. Meter Switch: RF Input.
   l. Frequency Select Switches: 10000.0 kHz.
5. Set up sweep generator for approximately 1 mV rms output at 10.0 MHz, with a sweep rate of about 10 sweeps per second. Connect sweep generator to receiver. Tune sweep generator carefully for audio output and observe level on RF In Meter. Remove generator from receiver input and turn RF Gain control clockwise until RF In Meter indicates level observed above. Replace sweep generator at receiver input and observe swept display on oscilloscope.

6. Put 2nd Mixer card on extender card and adjust L3 and L2 for the combination that results in maximum amplitude, consistent with least ripples in the passband.

7. Put 2nd Mixer back in receiver and do Step 2, above, to check flatness.

8. Go to Steps 1. and 2. for the 8 MHz IF amplifier also.

NOTE

84 MHz input level to the 2nd Mixer board is 100 mV rms.

c. 8 MHz IF Amplifier Alignment (Refer to 8-MHz IF Amplifier Schematic Diagram, page 7. 5)

1. The input coil L1 on this card affects the passband shape of the 8 kHz wide filter (FL1) on the 2nd Mixer card. L1 should be tuned by using an extender card and following the same test setup and procedure employed to tune L2 and L3 on the 2nd Mixer card.

2. Use the same setup as in preceding Step 1. Tune L7 for maximum output amplitude of the 8 MHz output signal. Repeat Steps 6., 7., 8., in 2nd Mixer alignment procedure.

3. Depress USB IF Bandwidth button. Slow sweep speed down to to about 3 - 4 sweeps per second and adjust L3 for best passband shape (i. e., lack of passband ripples). Hum on the sweep generator output can cause presentation of a confusing picture. If the hum is excessive, the generator may have to be replaced with a hum-free generator that can then be swept "by hand" while observing passband ripples. Since this adjustment involves only one coil the correct spot can be found quickly.

4. Remove 2nd Mixer card. Put signal generator tuned to 8. 0 MHz at 3 mV rms output between terminal B on 8 MHz IF amplifier connector and ground. Set up receiver as in preceding Step 1 for RF Section Alignment, except turn RF Gain switch clockwise just enough for switch to click (RF In meter will indicate full-scale).

   Turn R2 (multiturn pot) until output read on RF voltmeter at the 8 MHz Output jack is 14 mV ±1 mV.

   Remove signal generator and replace the 2nd Mixer card to restore receiver to operating condition.

NOTE

The AGC control voltage at Pin L of the connector goes from 1. 45 volts when the RF Gain control is fully counterclockwise (AGC on) to 11. 1 volts when the RF Gain control is turned clockwise just past the point where the switch clicks.

d. AM and Product Detector Alignment (Refer to AM and Product Detector Schematic Diagram, page 7.7))

1. Remove 8 MHz IF Amplifier card from receiver. Place AM and Product Detectors card on extender card. Depress AM mode switch.
2. Set up signal generator for 3 mV rms output, modulated 30% at 1000 Hz, at 8.0 MHz. Apply generator's output between terminal L of the AM and Product Detectors connector and ground. Connect oscilloscope to terminal Y of the same connector. Turn R13 for maximum output, and then peak L6 per maximum output. Back off R13 until the peak-to-peak scope indication is 120 mV peak-to-peak.
3. Set signal generator for 7 mV rms output, with 80% modulation at 1000 Hz. Connect audio distortion analyzer to terminal Y and ground and trim L6 for minimum distortion, which should be less than 5%. If necessary readjust R13 for 120 mV peak-to-peak output level for 30% 1000 Hz modulation at 3 mV input.
4. Depress CW mode button. Set signal generator to CW with 3 mV rms output. Connect scope to junction of R3, R4, and C9, tune L1 and L2 for maximum indication. Adjust R10 for 120 mV peak-to-peak output at terminal Y.

NOTE

The product detector BFO injection level should indicate 1V rms.

e. AGC Amplifier Alignment (Refer to AGC Amplifier Schematic Diagram, page 7.9)

1. Use extender card. Set AGC to "on" position and remove 8 MHz IF Amplifier and AM and Product Detectors cards.
2. Adjust R12 and R21 fully clockwise. Tune signal generator to 8.0 MHz with 3 mV rms output between terminal Y of the AGC Amplifier connector and ground. Set digital voltmeter (or accurate VTVM) between IF AGC, terminal K, and ground. Adjust R4 for maximum voltage, and peak L1 for maximum voltage. Readjust R4 for 5V DC.
3. Increase signal generator to 7 mV rms output. The IF AGC voltage should rise to 10 ±. 5 VDC.
4. Decrease signal generator level to point where IF AGC output voltage is 9 VDC. Connect digital voltmeter to delayed AGC output, terminal B. Adjust R12 for 7 VDC. Adjust signal generator output level for 7.5 mV rms. Adjust R21 for minimum output level, which should be less than 2.5 VDC.
5. Repeat preceding Step 4 as many times as is necessary to achieve the limits of 7 VDC at delayed AGC output for 9 VDC at 8 MHz.
6. Observe RF meter reading. Set signal generator for 5 mV rms

output and adjust R14 for a -3 dBm reading. Set signal generator for 7 mV rms and adjust R16 for an 80 dB reading.

7. Repeat preceding Step 6 as many times as necessary to achieve the two limit conditions.

f. Regulator Alignment (Refer to Regulator Schematic Diagram, page 7. 11)

1. Remove bottom cover nearest rear of receiver.
2. Connect digital voltmeter between C56 and ground. Adjust R7 for +24. 0 VDC.
3. Connect digital voltmeter between C25 and ground. Adjust R19 for +24. 0 VDC.
4. Connect digital voltmeter between C56 and ground. Adjust R26 for +5. 6 VDC.
5. Replace cover.

6. 3 SYNTHESIZER ADJUSTMENTS

a. Minor Loop Analog Alignment (Refer to Minor Loop Analog Schematic Diagram, page 7.13)

1. Use extender card. Put a DC-coupled oscilloscope at the junction of R39, C24, CR8, CR7, CR21, and R38 (varactor voltage test point).
2. Set front-panel frequency-select switches to 00000. 0 kHz indication and depress Fine Tune switch on front panel. Turn on receiver. The voltage seen on the scope should be DC if the minor loop is in lock. (If the loop is not locked there will be a voltage varying at a slow rate.) Measure the voltage at the varactor voltage test point. It should be 9. 0 volts when locked.

   Set front-panel frequency-select switches to 00099. 9 kHz. The voltage at the varactor voltage test point should be a DC voltage, 13. 0 volts.
3. If the loop is either out of lock or not at the voltages listed in preceding Step 2, C31 and T3 must be adjusted. Set C31 to the middle of its range. Adjust T3 until phase lock is achieved. Repeat preceding Step 2. If the varactor voltage excursion is too small between the extremes of the switch settings (smaller than 9 to 13 volts) C31 must be adjusted for more capacity and T3 adjusted for less inductance. If the varactor voltage excursion is too large C31 must be adjusted for less capacity. The trimmer C31 controls the frequency range spread and T3 shifts the frequency, keeping the range essentially intact.
4. Repeat preceding Steps 2 and 3 until conditions are correct.
5. Rapidly change 10-kHz switch from 0 to 9, and back again. The loop should rapidly respond by locking (the transient AC waveform at the varactor voltage test point should rapidly go

to a DC voltage).

NOTE

The level of the 70. 4 - 71. 9984 MHz output should be 300 mV rms across 50 ohms (terminal Z on the connector). The voltage level fed to the minor loop variable divider should be a minimum of 150 mV across 50 ohms (terminal W). The level of the 64 MHz signal from the VHF Reference card should be 50 mV rms into 50 ohms (at terminal M of minor loop analog connector).

b. Loop Translator Alignment (Refer to Schematic Diagram, page 7. 15)

1. Use extender card. Connect high impedance probe of RF voltmeter (Boonton 91 CA recommended) to C27 and ground. Adjust L8 for maximum output, which should be greater than 500 mV rms.
2. The alignment of the 4-pole 88. 45-MHz bandpass filter must be done with a sweep generator that has 50-ohm output termination . The green output lead from T1 must be disconnected and the A1 mixer must be removed to get at the filter. Connect equipment according to figure 6. 1. The filter should be tuned according to figure 6. 2. (The insertion loss should be less than 14 dB.)
3. The response should be 35 dB minimum down at 93. 45 and 83. 45 MHz (reading referenced to 0 dB = insertion loss level). Note that this particular measurement should be performed with the sweep generator set for CW and an RF voltmeter with 50-ohm termination (Boonton 91 CA recommended) at the output of the filter.
4. Carefully re-connect T1 output transformer green lead and mixer A1.

NOTE

The 3. 6 - 33. 5999 MHz output level between terminal Z and ground of the connector should be at TTL level; i. e., 0. 8 volt maximum for logical 0 and 2 volt minimum for logical 1.

The level of the 92 - 121. 9999 MHz signal from the Major Loop VCO Buffer at terminal U should be 300 mV rms minimum into to 50 ohms.

The level of the 70. 4 - 71. 9984 MHz signal from the Minor Loop Analog card at terminal D should also be 300 mV rms minimum into 50 ohms.

The level of the 84 MHz signal from the VHF Reference card at terminal L should be 100 mV rms minimum into 50 ohms.

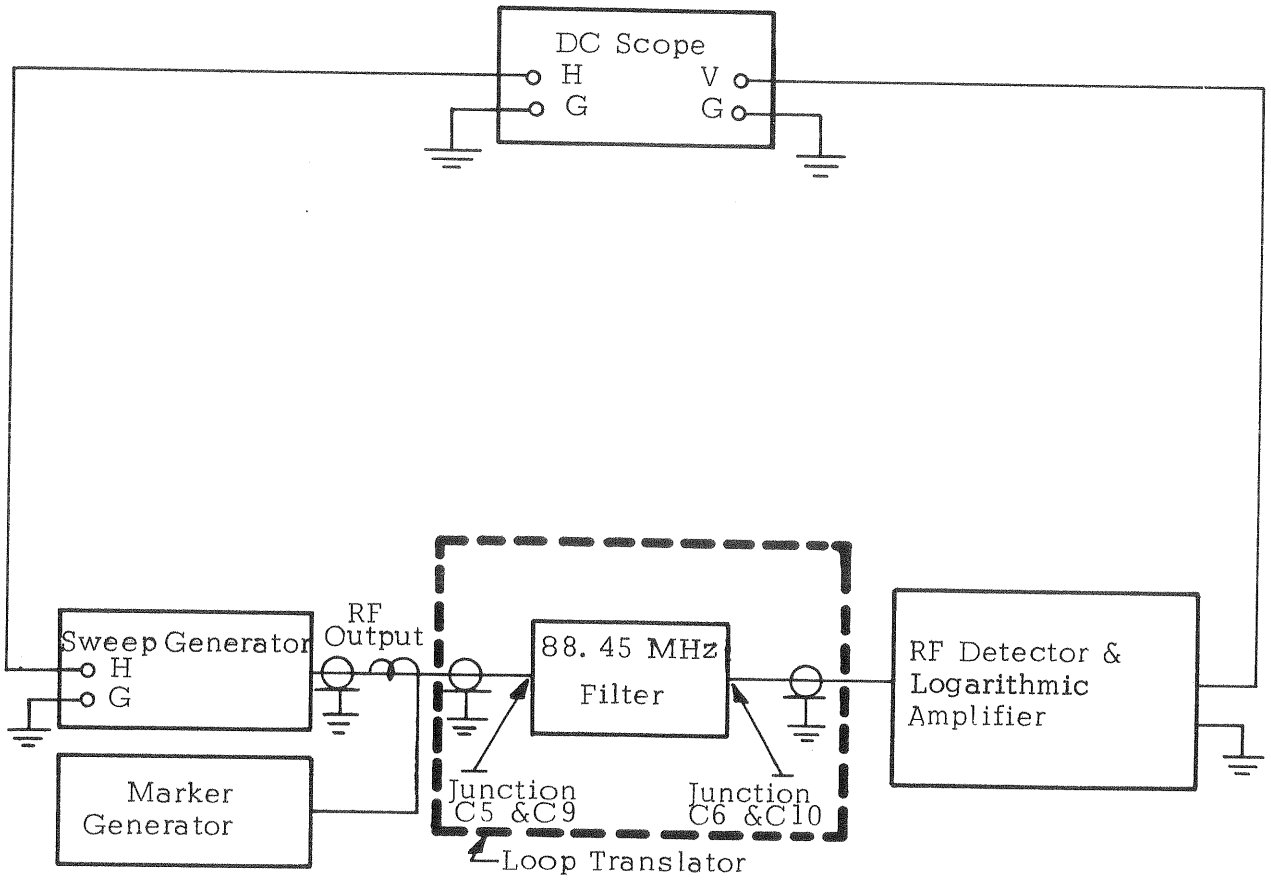


Figure 6. 1 Test set-up: 88. 45-MHz filter alignment.

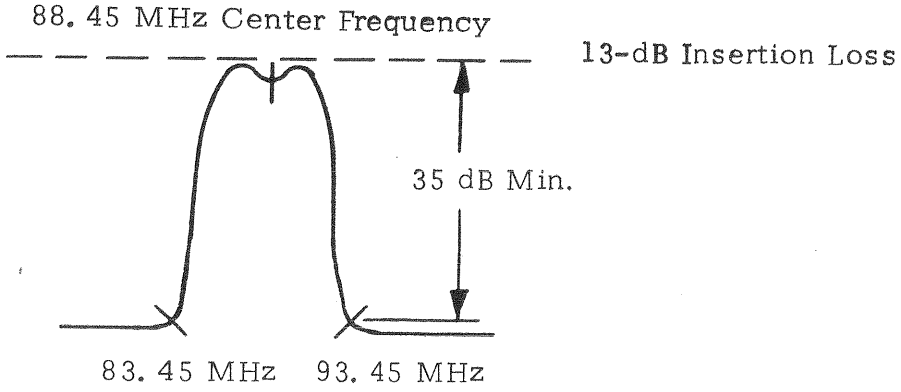


Figure 6. 2 Response of 88. 45-MHz filter.

c. VHF Reference Alignment (Refer to Schematic Diagram, page 7. 17)

1. Depress Fine Tune control on Front panel. Use extender card.
2. Disconnect 84 MHz coax (push-on connector) from jack on bulkhead shielding signal path compartment from synthesizer compartment, J23 (second jack from rear of receiver). Connect RF voltmeter with 50 ohm termination to 84 MHz output plug using proper connector.
3. Tune L1 and L2 (slug position should be near bottom of coil) for maximum output, which should be greater than 150 mV rms. Disconnect RF voltmeter and replace with high-frequency counter with 50 ohm termination. Frequency indicated should be 84. 003 MHz ±1 kHz. Fine tune L1 if necessary to obtain this frequency. Recheck output level. It should remain greater than 150 mV rms.
4. Pull out Fine Tune control. Connect digital voltmeter (or accurate VTVM) at terminal M of connector. Adjust Fine Tune knob for 11 VDC. Remove Minor Loop Analog card from receiver. Connect high-frequency counter with 50 ohm termination between terminal R and ground. Tune C27 and L4 until counter indicates 64. 0 MHz ±100 Hz.
5. Turn Fine Tune knob fully clockwise. Counter should indicate higher than 64. 0016 MHz.
6. Turn Fine Tune knob fully counterclockwise. Counter should indicate lower than 63. 9984 MHz. By changing C27 and retuning L4 attempt to center 64. 0 MHz ±100 Hz in center of Fine Tune knob's rotation.
7. Reconnect RF voltmeter in place of counter. Output should exceed 50 mV rms.

d. Major Loop Analog and Acquisition Alignment (Refer to Schematic Diagram, page 7.19)

NOTE

There are two methods of adjusting the VCOs used on the Major Loop Analog and Acquisition card: Either open-loop (preferable) or closed-loop (alternative).

1. Open Loop Method of Adjustment

(a) Remove R46, CR20, and CR21 from board. Attach variable power supply capable of going between roughly 8 - 20 VDC to junction of R37 and C33. (Note that a variable power supply can be made by connecting a 10K pot across the 24 VDC bus to ground.) Use extender card so that adjustment points can be easily reached.

(b) Disconnect synthesizer output plug from signal-path bulkhead push-on connector J24 (one nearest rear of receiver). Through suitable adapters connect synthesizer output to high frequency counter with 50-ohm termination.

(c) VCO #1.

(1) Set C40 to the middle of its range. Set front-panel Frequency-Select switches to 01000.0 kHz. Set variable power supply to 10 VDC. Adjust T3 until the counter reads 92 MHz ±50 kHz.

(2) Adjust power supply to 15 VDC. Counter should indicate 94 MHz ±50 kHz.

(3) If the range is too small; i.e., frequency at 15 VDC is lower than 94 MHz ±50 kHz, C40 capacitance must be reduced. If frequency at 15 VDC is higher than 94 MHz ±50 kHz, C40 capacitance must be increased. Proceed back to preceding Step (1). Repeat process until range is correct.

(d) Repeat preceding Steps (a), (b), and (c) for the following table:

Frequency Select Switch	Frequency Limit	Power Supply	Frequency Limit	Power Supply	Adjust
01000.0 kHz	92 MHz ±50 kHz	10 VDC	94 MHz ±50 kHz	15 VDC	C40, T3
03000.0 kHz	94 MHz ±50 kHz	10 VDC	98 MHz ±50 kHz	16 VDC	C41, T4
07000.0 kHz	98 MHz ±50 kHz	9 VDC	106 MHz ±50 kHz	17 VDC	C42, T5
15000.0 kHz	106 MHz ±50 kHz	9 VDC	114 MHz ±50 kHz	17 VDC	C43, T6
25000.0 kHz	114 MHz ±50 kHz	9 VDC	122 MHz ±50 kHz	17 VDC	C48, T7

(In each VCO note that the trimmer capacitor spreads out the range while the inductor shifts the frequency range keeping the frequency spread relatively intact.)

(e) Replace R46, CR20, and CR21 on board and remove the variable power supply. Put a scope probe at the point where the variable power supply was formerly connected. Move the front-panel Frequency-Select switches through all MHz positions and observe to see that loop locks at all frequencies. Lock is indicated when a steady DC voltage is observed on the scope rather than an AC beat note.

2. Closed Loop Method of Adjustment (Alternative)

NOTE

As the name implies, the loop is kept closed in this method and the trimmer capacitor and inductor for each VCO are adjusted so that the loop remains in lock and also so that the correct voltage appears at the varactor control line over the frequency range the particular VCO covers.

(a) The scope is left hooked to the junction of R46, CR20, CR21,

CR18, CR19, R37, and the VCO control line. A digital voltmeter is also placed on the varactor control line to monitor the DC voltage where when the loop is in lock.

(b) For each VCO the adjustable components are tuned until the loop is locked and until the correct varactor voltage appears as per the following chart. (The capacitors, as before, are first preset to the middle of their ranges.)

Major Loop VCO Setup

VCO No.	Frequency Select Switches	Varactor Voltage	Adjustable Components
1	00000.0 kHz	10 VDC	C40, T3
1	01999.9 kHz	15 VDC	C40, T3
2	02000.0 kHz	10 VDC	C41, T4
2	05999.9 kHz	16 VDC	C41, T4
3	06000.0 kHz	9 VDC	C42, T5
3	13999.9 kHz	17 VDC	C42, T5
4	14000.0 kHz	9 VDC	C43, T6
4	21999.9 kHz	17 VDC	C43, T6
5	22000.0 kHz	9 VDC	C48, T7
5	29999.9 kHz	17 VDC	C48, T7

As before, the trimmer capacitor for each VCO spreads out the range while the inductor shifts the frequency range, keeping the frequency range relatively intact.

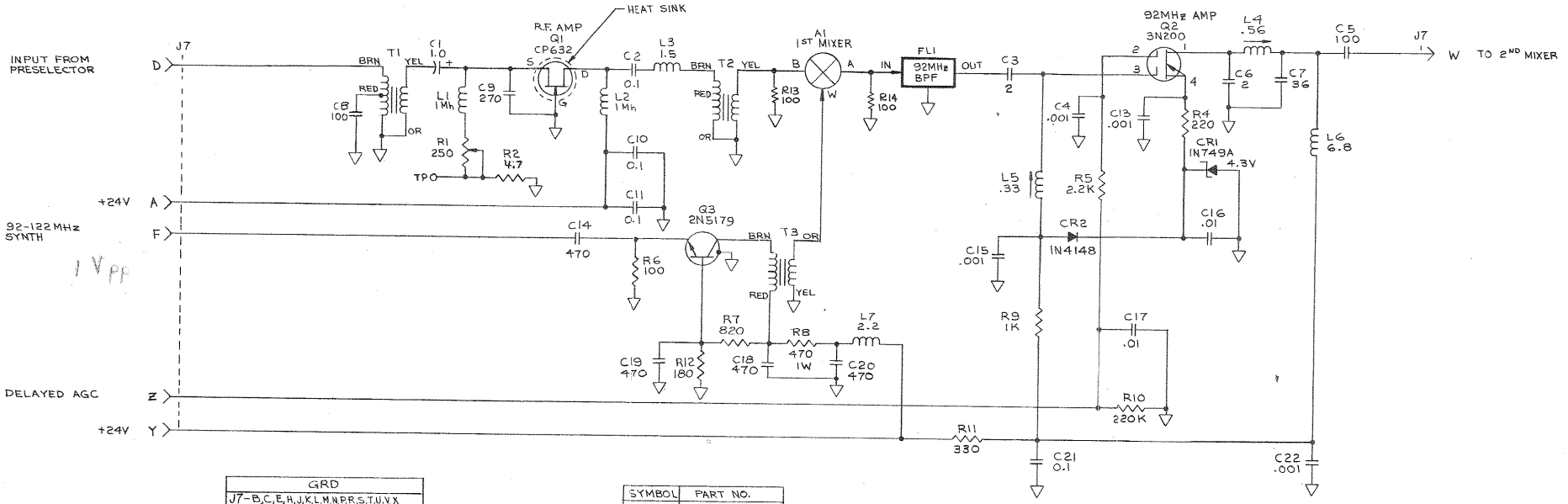
NOTE

The output of the card into a 50-ohm load (with VCO buffer card removed) is 100 mV rms minimum from 92 - 122 MHz.

SECTION 7

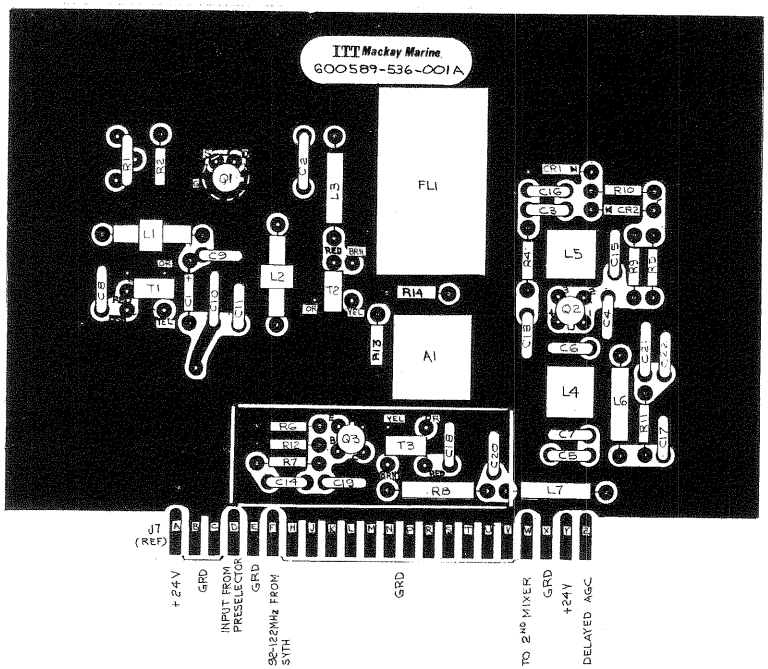
SCHEMATIC AND WIRING DIAGRAMS AND ASSEMBLY DRAWINGS

Contents



GRD
J7-B,C,E,H,J,K,L,M,N,P,R,S,T,U,V,X

SYMBOL	PART NO.
T1,T2	600052-512-001
T3	600050-512-001



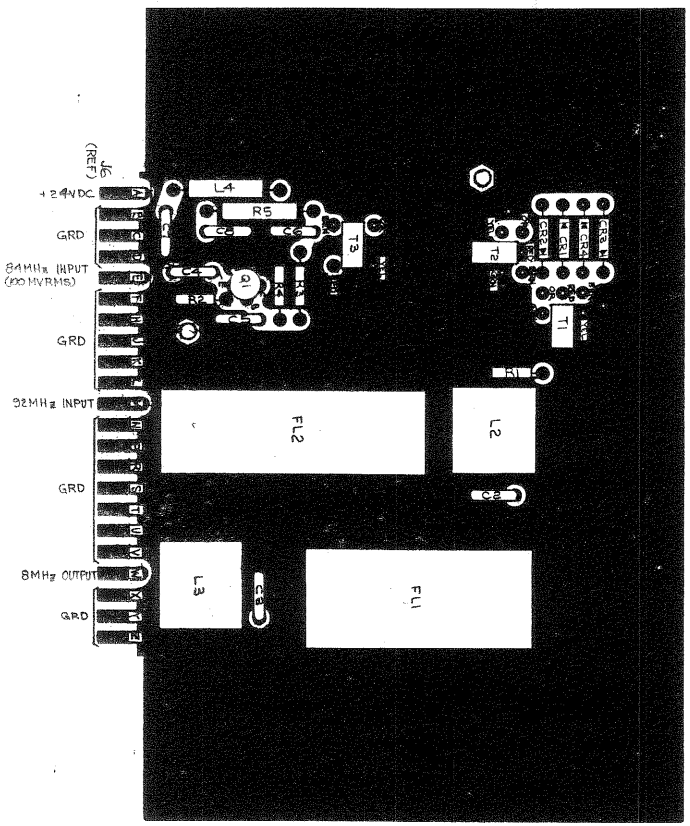
NOTES:
1-UNLESS OTHERWISE SPECIFIED;
ALL CAPACITANCE VALUES GREATER THAN 1.0 ARE IN Pf.
ALL CAP VALUES 1.0 AND SMALLER ARE IN μf.
ALL INDUCTANCE VALUES μh.
ALL RESISTANCE VALUES IN OHMS
K=1000

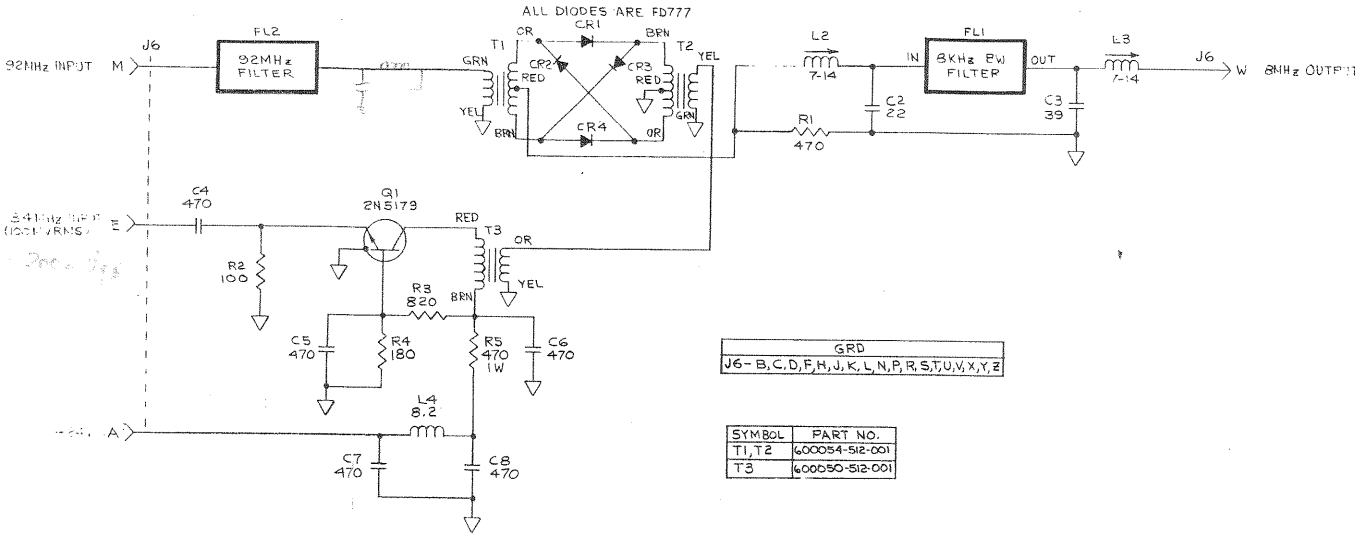
0895D021

ITT Mackay Marine
33 TERMINAL AVE. CLARK N.J. U.S.A.

TITLE: SCHEMATIC R.F. SECTION

SCALE | APP'D ENG | CHK'D | DWG 620589-534 | REV A





GRD
J6-B,C,D,F,H,J,K,L,N,P,R,S,T,U,V,X,Y,Z

SYMBOL	PART NO.
T1,T2	600054-512-001
T3	600050-512-001

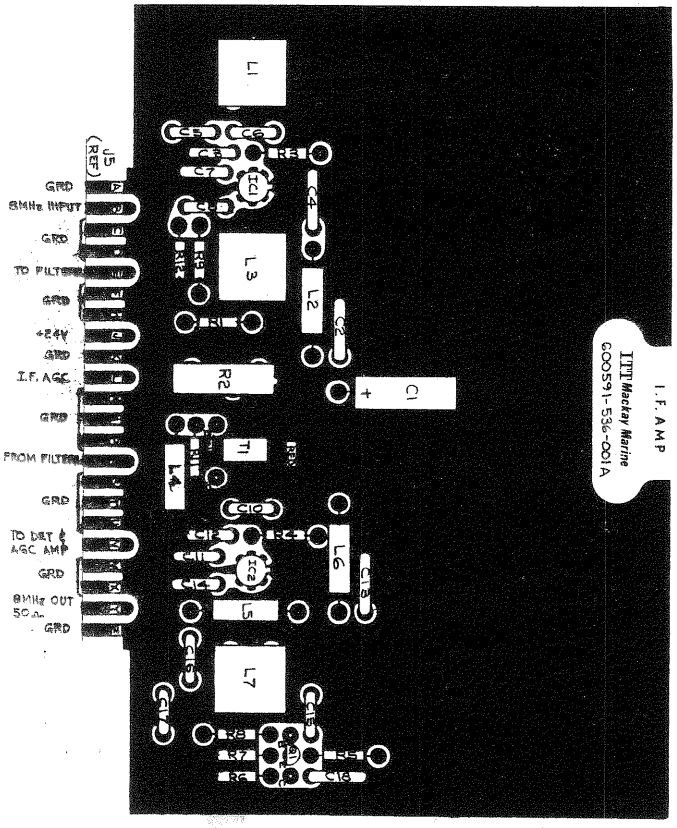
NOTES:
1. UNLESS OTHERWISE SPECIFIED:
   ALL CAPACITANCE VALUES GREATER THAN 1.0 ARE IN pf.
   ALL CAP VALUES 1.0 AND SMALLER ARE IN μf.
   ALL INDUCTANCE VALUES ARE μh.
   ALL RESISTANCE VALUES IN OHMS.

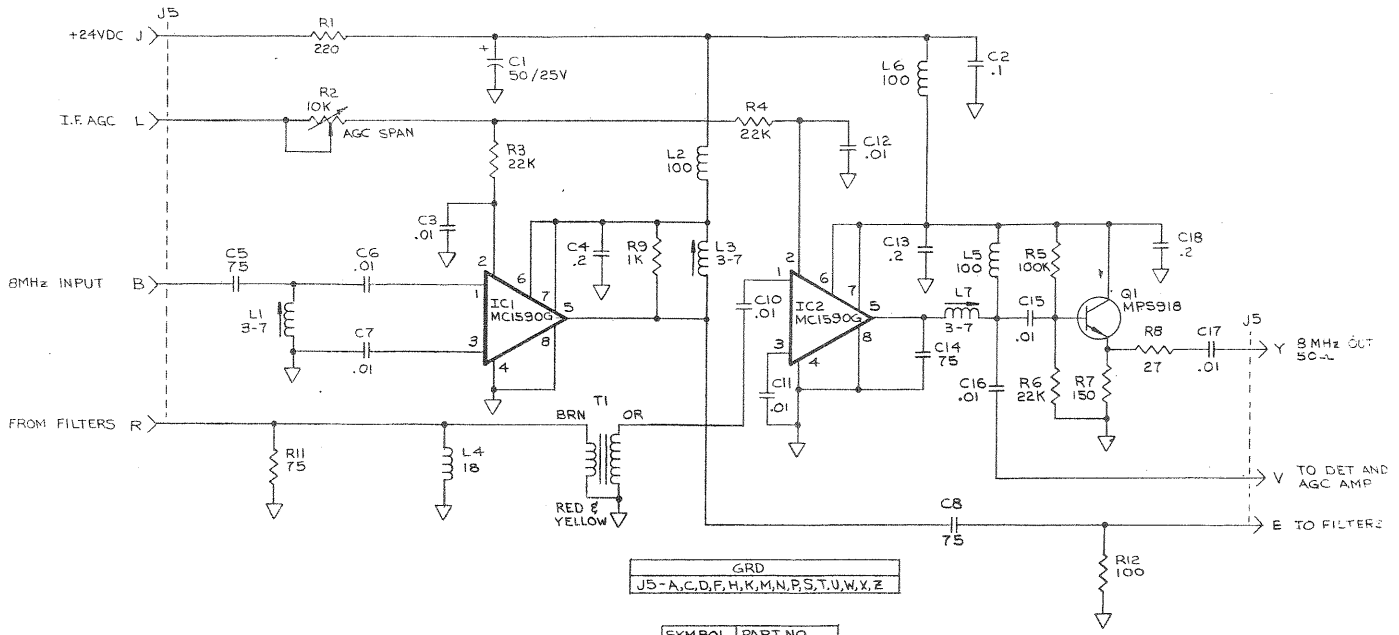
0895-CRL

ITT Mackay Marine
123 TERMINAL AVE. CLARK N.J. U.S.A.

TITLE: SCHEMATIC 2ND MIXER

SCALE | APPD | DWN | CHK'D | DWN | 620590-534 | REV A





SYMBOL	PART NO.
T1	600055-512-001

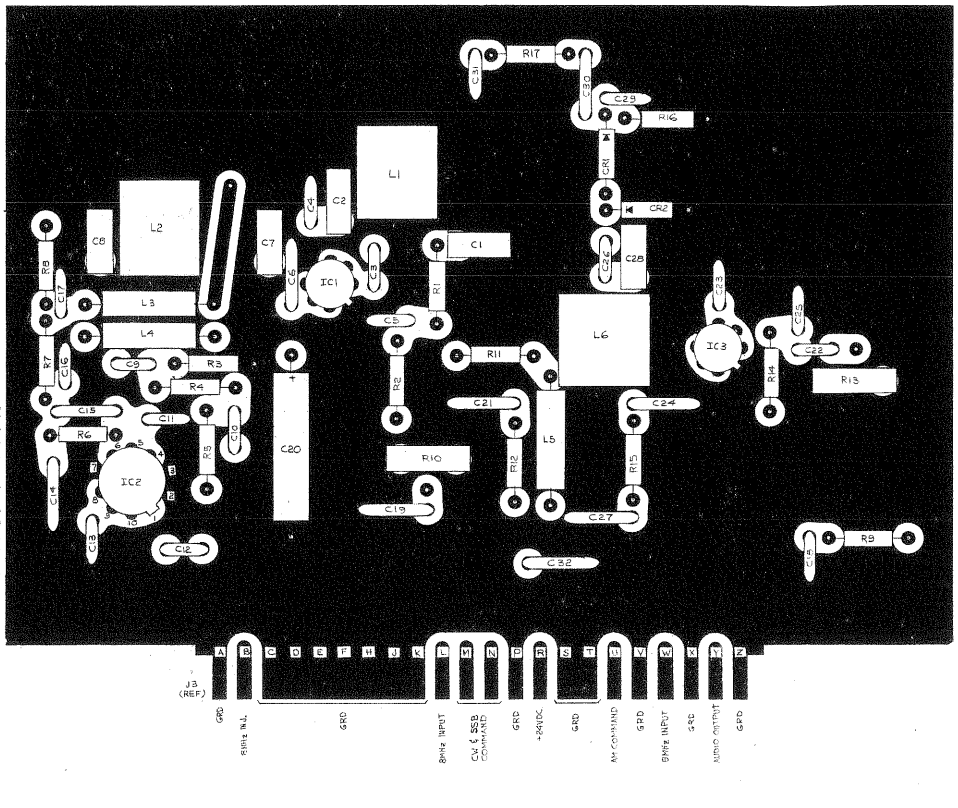
NOTES:
1-UNLESS OTHERWISE SPECIFIED:
ALL CAPACITANCE VALUES 1.0 AND SMALLER ARE IN μF.
ALL INDUCTANCE VALUES μh.
ALL RESISTANCE VALUES OHMS.
K=1000

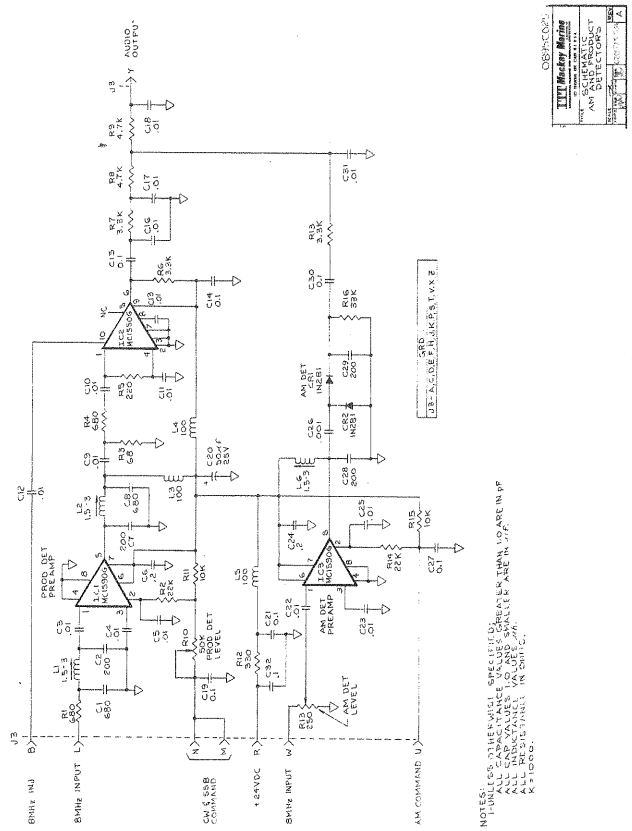
0895C023

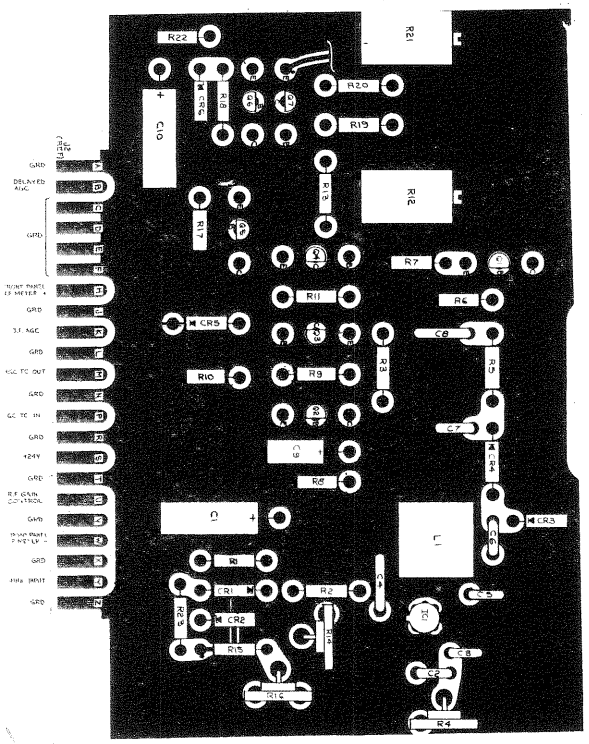
ITT Mackey Marine
133 TERMINAL AVE CLARK N.J. U.S.A.

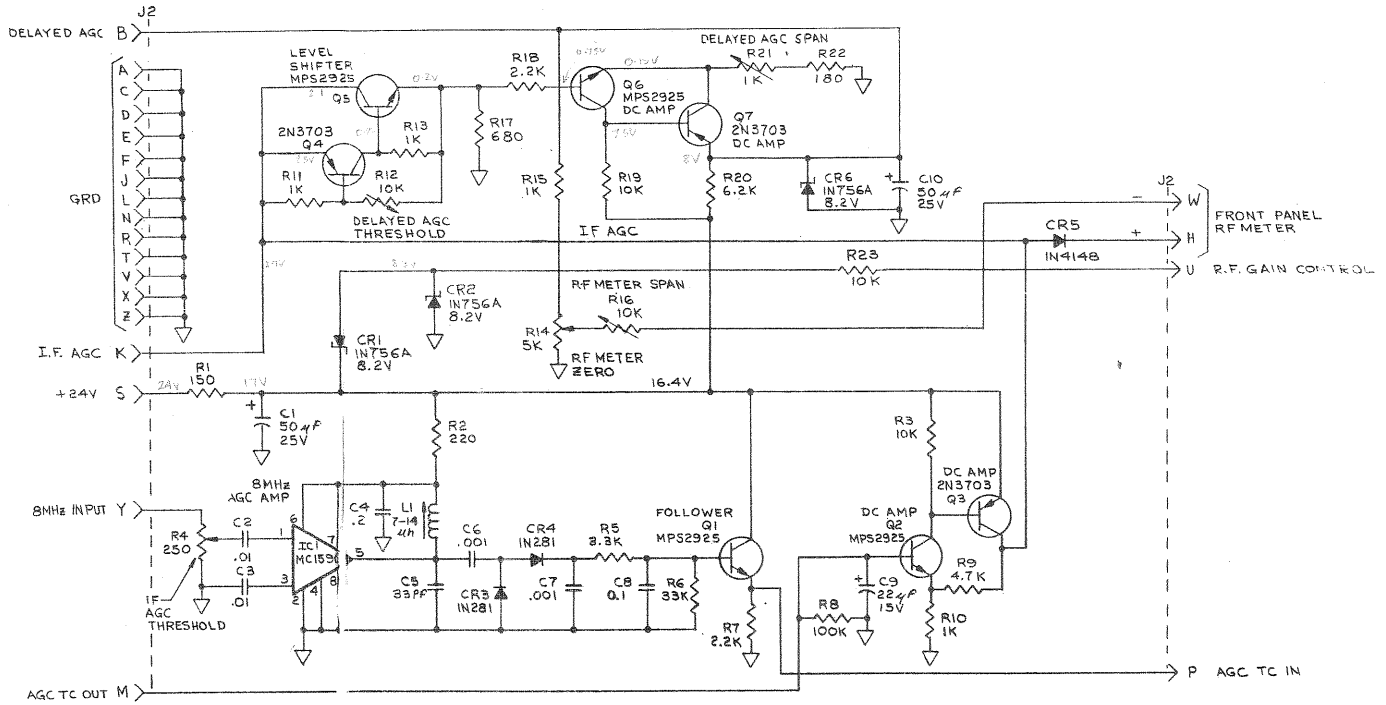
TITLE: SCHEMATIC 8MHz I.F. AMPLIFIER

SCALE		620591-536	REV A
APPD	ENG	CHK'D	DRN
		WLC	


J3 (REF)
GRD
8MHz INJ.
GRD
8MHz INPUT
CW & SSB COMMAND
GRD
+24VDC
GRD
AM COMMAND
GRD
8MHz INPUT
GRD
AUDIO OUTPUT
GRD
L1
L2
L3
L4
L5
L6
IC1
IC2
IC3
C1
C2
C4
C5
C6
C7
C8
C10
C11
C12
C13
C14
C15
C16
C17
C18
C19
C20
C21
C22
C23
C24
C25
C27
C28
C29
C30
C31
C32
R1
R2
R3
R4
R5
R6
R7
R8
R9
R10
R11
R12
R13
R14
R15
R16
R17
CR1
CR2


J3
8MHz INJ.
8MHz INPUT
CW & SSB COMMAND
+24VDC
8MHz INPUT
AM COMMAND
AUDIO OUTPUT
PROD DET PREAMP
PROD DET LEVEL
AM DET PREAMP
AM DET LEVEL
AM DET
GRD
NOTES:
UNLESS OTHERWISE SPECIFIED:
ALL CAPACITANCE VALUES GREATER THAN 1.0 ARE IN pF
ALL CAPACITANCE VALUES SMALLER ARE IN μF
ALL INDUCTANCE VALUES ARE IN μH
ALL RESISTANCE VALUES ARE IN OHMS
K = 1000
ITT Mackay Marine
SCHEMATIC
AM/CW PRODUCT DETECTORS



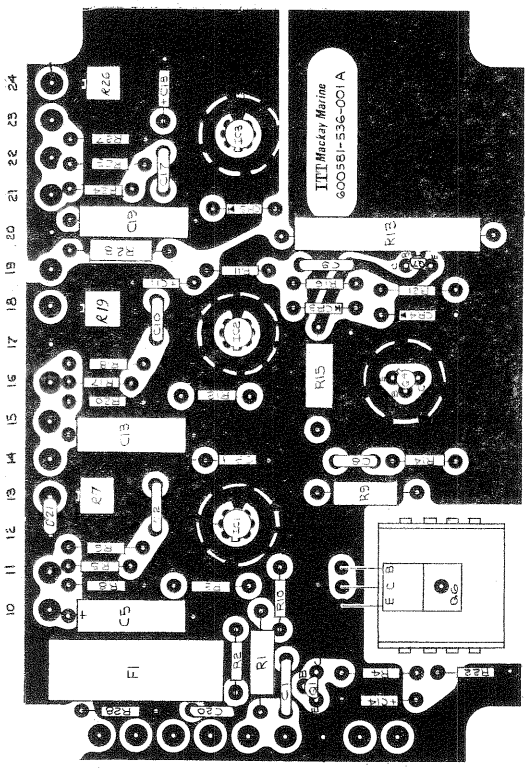


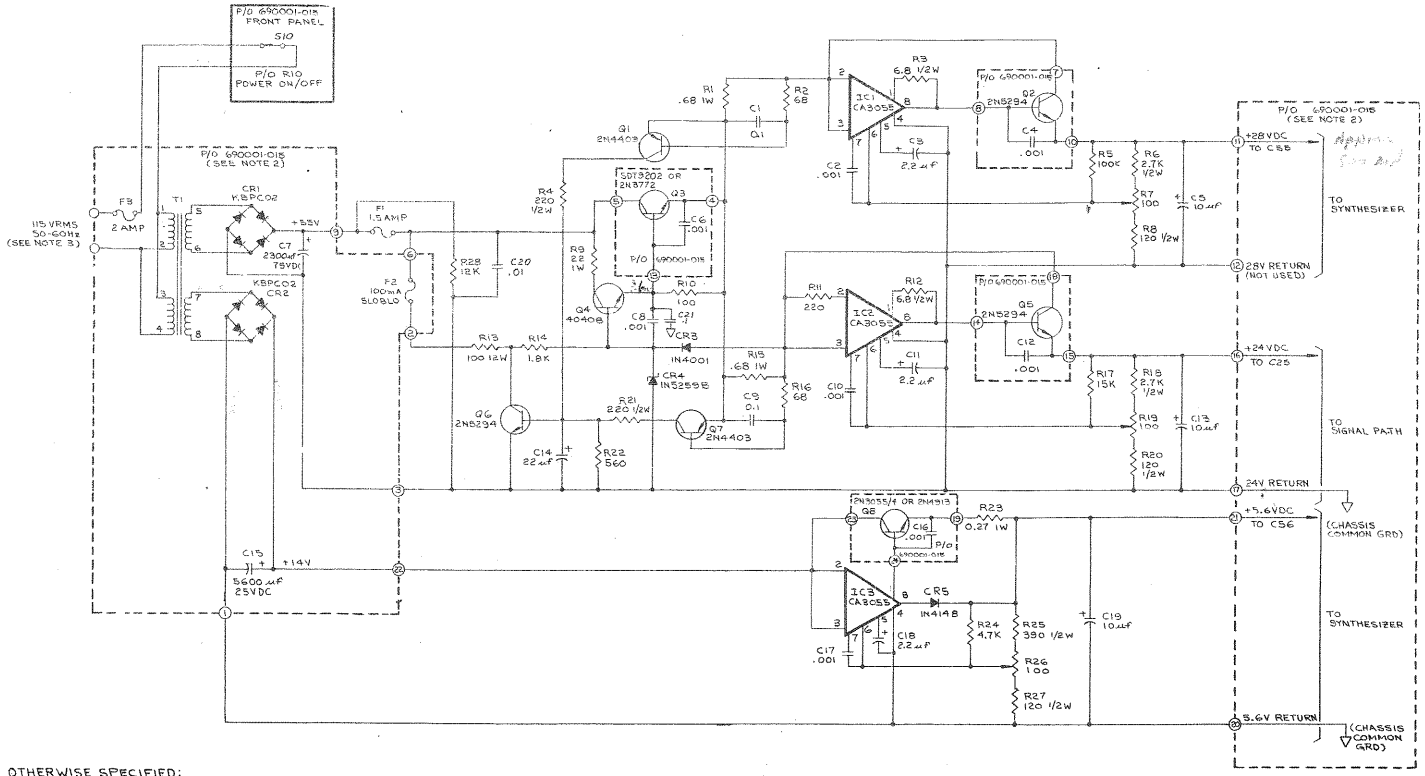
NOTES:
1- UNLESS OTHERWISE SPECIFIED;
ALL CAPACITANCE VALUES 1.0 AND SMALLER ARE IN μF
ALL RESISTANCE VALUES IN OHMS
K = 1000

0895C026

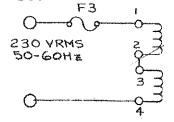
ITT Kenkay Marine	
TITLE	SCHEMATIC AGC AMPLIFIER
SCALE NONE	CE0594536 REV A

Use CA 3085 as replacement for CA 3055





NOTES:
1. UNLESS OTHERWISE SPECIFIED; ALL CAPACITANCE VALUES 1.0 AND SMALLER ARE IN uf. ALL RESISTANCE VALUES IN OHMS. K=1000.
2. ALL COMPONENTS WITHIN DOTTED LINES APPEAR ON 690001-015 "INTERCONNECTION DIAGRAM".
3. FOR 230 VRMS OPERATION CONNECT TRANSFORMER PRIMARY WINDINGS IN SERIES:



AND CHANGE F3 TO 1 AMP

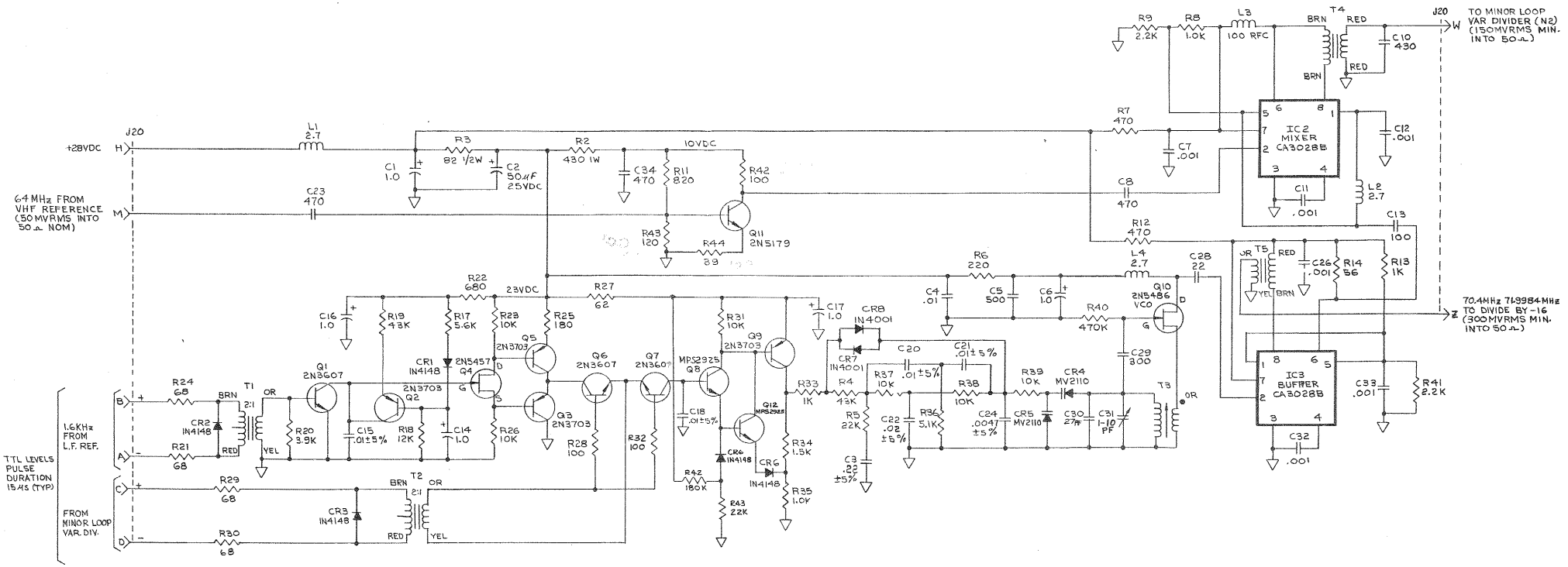
SYMBOL	PART NO.
T1	600047-512-001

0895D038

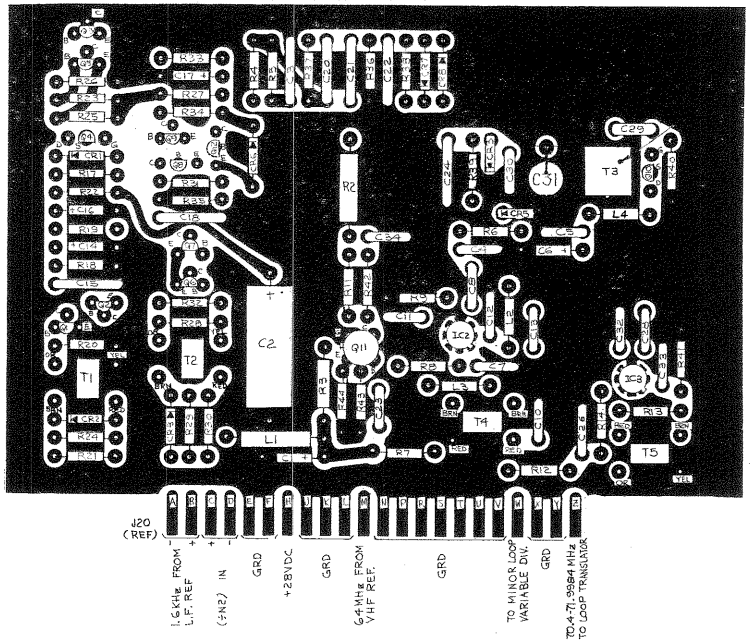
ITT Mackay Marine
133 TREMONT AVE CLARE N.J. U.S.A.

TITLE: SCHEMATIC REGULATOR

SCALE | APP'D | CHK'D | DWN | 420581-536 | REV A



NOTES:
1- UNLESS OTHERWISE SPECIFIED;
ALL CAPACITANCE VALUES GREATER THAN 1.0 ARE IN P.F.
ALL CAP VALUES 1.0 AND SMALLER ARE IN μF.
ALL INDUCTANCE VALUES μh.
ALL RESISTANCE VALUES IN OHMS.
K=1000



GRD
J20 E,F,J,K,L,N,P,R,S,T,U,V,X,Y

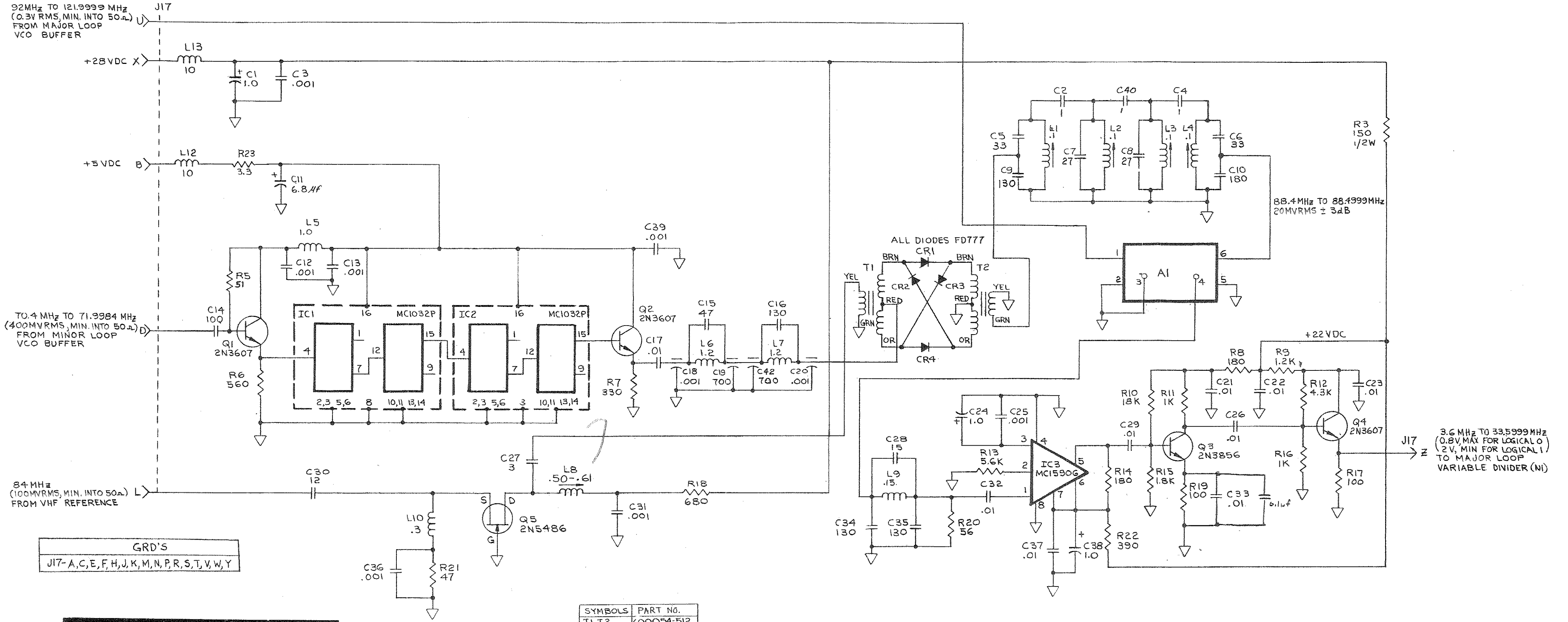
SYMBOL	PART NO.
T1,T2	600053-512-001
T3	600060-512-001
T4	600056-512-001
T5	600050-512-001

0895D035

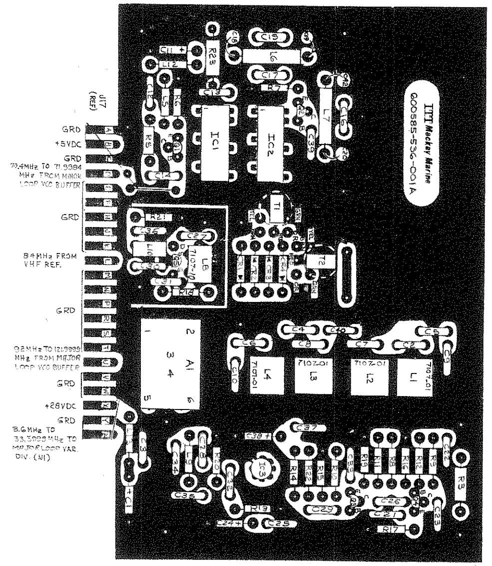
ITT Mackay Marine
A DIVISION OF INTERNATIONAL TELEPHONE AND TELEGRAPH CORPORATION
123 TERMINAL AVE. CLARK N.J. U.S.A.

TITLE: SCHEMATIC MINOR LOOP ANALOG

SCALE | APPD | CHKD | DRN | 620579-536 | SHT | A



SYMBOLS	PART NO.
T1,T2	600054-512



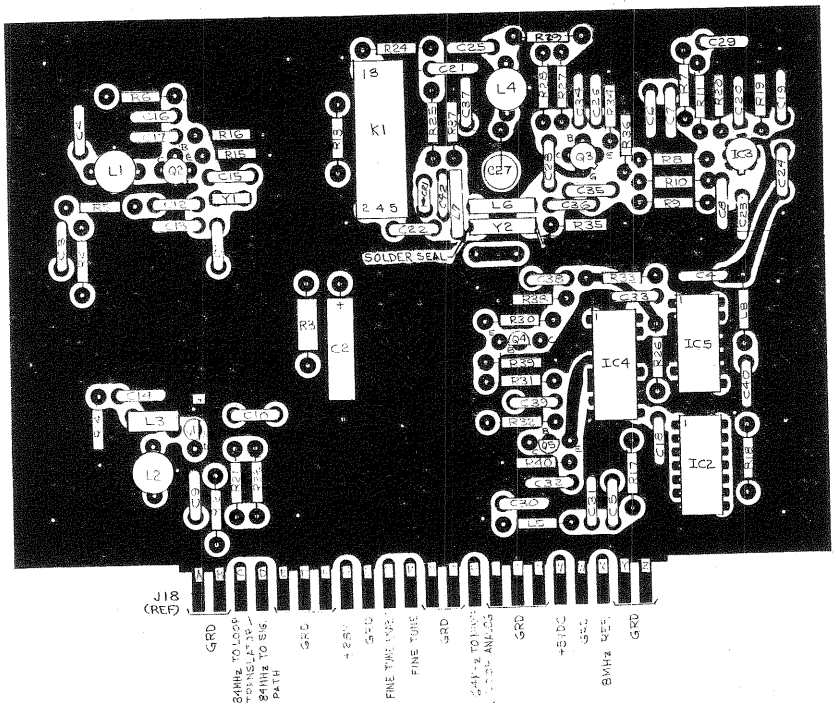
NOTES:
1- UNLESS OTHERWISE SPECIFIED:
ALL CAPACITANCE VALUES GREATER THAN 1.0 ARE IN pf.
ALL CAP VALUES 1.0 AND SMALLER ARE IN uf.
ALL INDUCTANCE VALUES Uh.
ALL RESISTANCE VALUES IN OHMS
K=1000

0895D032

ITT Mackay Marine

TITLE SCHEMATIC LOOP TRANSLATOR

620585-536 REV A



GRD
J18-A,B,E,F,H,K,N,P,S,T,U,W,Y,Z

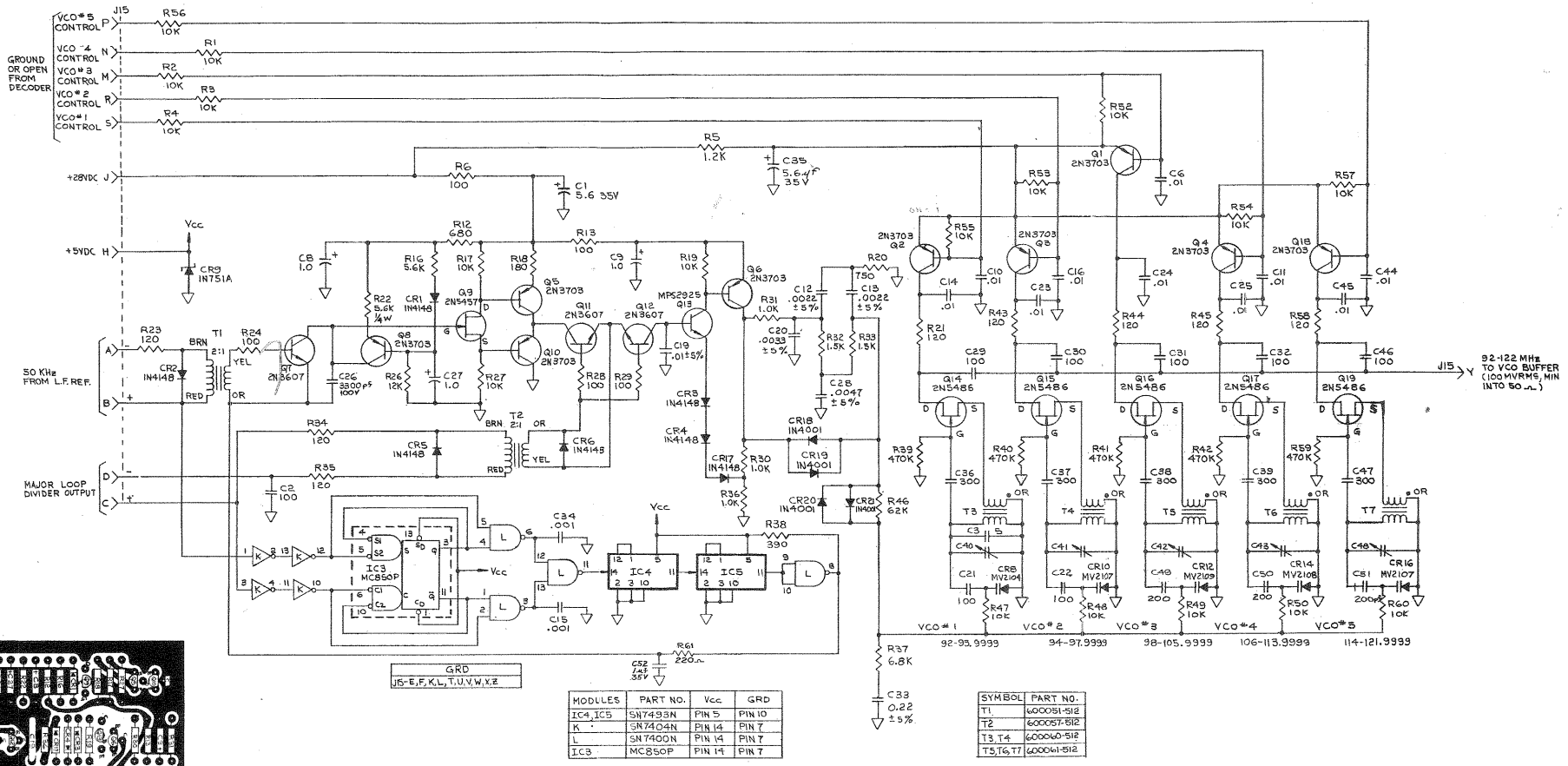
NOTES:
1-UNLESS OTHERWISE SPECIFIED;
ALL CAPACITANCE VALUES GREATER THAN 1.0 ARE IN PF.
ALL CAP VALUES 1.0 AND SMALLER ARE IN UF.
ALL INDUCTANCE VALUES ARE IN Uh.
ALL RESISTANCE VALUES IN OHMS.
K=1000

0895D033

ITT Mackay Marine
123 TOWNSEND AVE. CLIFTON, N.J. U.S.A.

TITLE: SCHEMATIC VHF REFERENCE

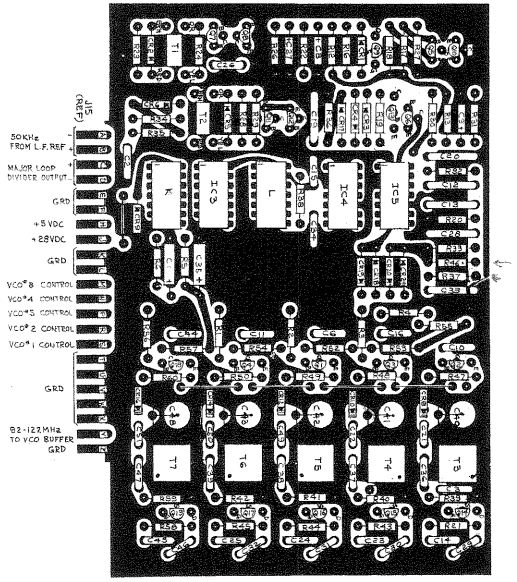
SCALE: NONE | DRWN: [illegible] | CHKD: [illegible] | DATE: 6/20/84 | REV: A



GRD
J15-E,F,K,L,T,U,V,W,X,Z

MODULES	PART NO.	Vcc	GRD
IC4, IC5	SN7493N	PIN 5	PIN 10
K	SN7404N	PIN 14	PIN 7
L	SN7400N	PIN 14	PIN 7
IC3	MC850P	PIN 14	PIN 7

SYMBOL	PART NO.
T1	600051-512
T2	600057-512
T3, T4	600060-512
T5, T6, T7	600061-512



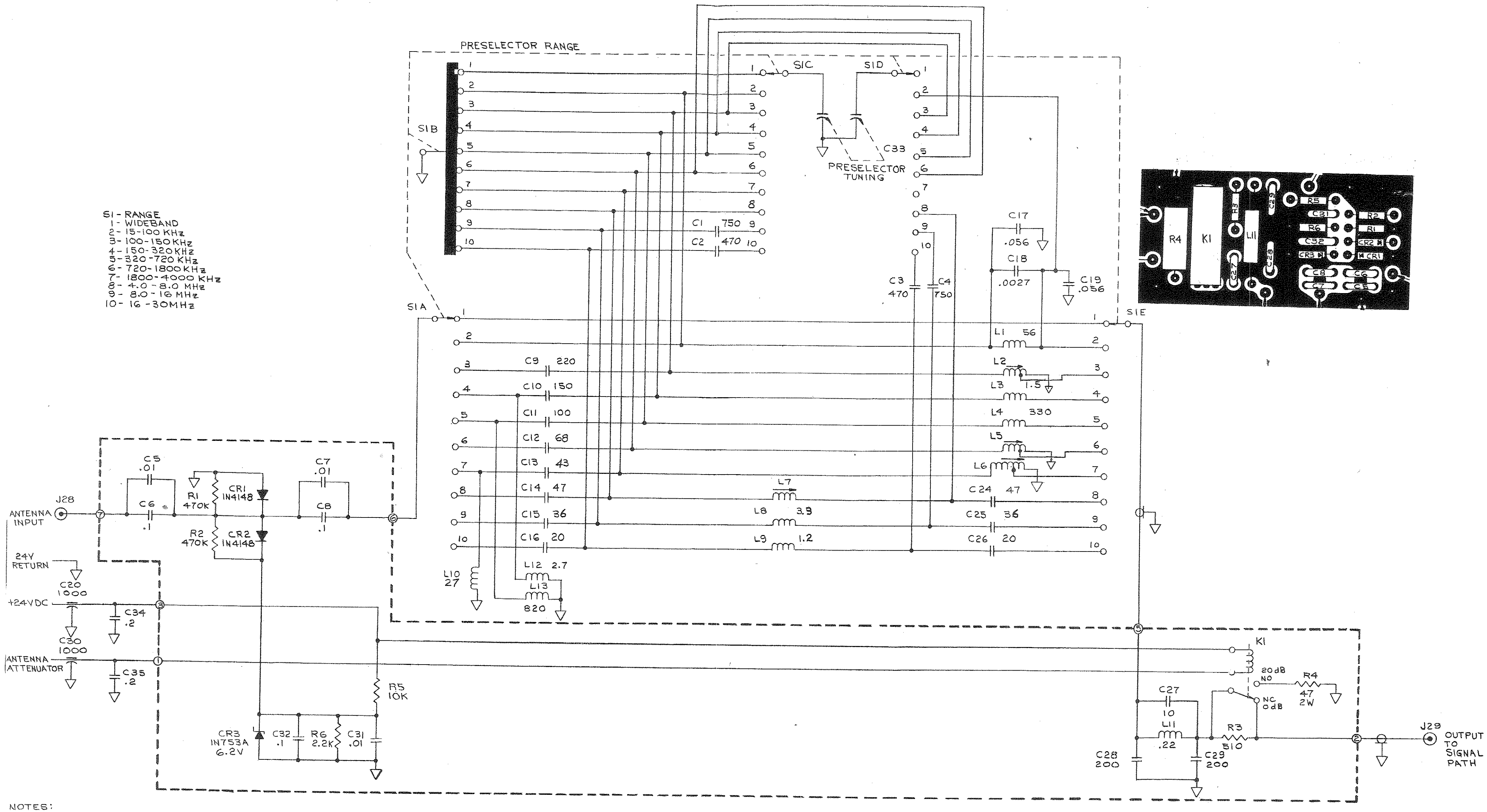
NOTES:
1-UNLESS OTHERWISE SPECIFIED;
ALL CAPACITANCE VALUES GREATER THAN 1.0 ARE IN PF.
ALL CAP VALUES 1.0 AND SMALLER ARE IN μF.
ALL RESISTANCE VALUES IN OHMS.
K=1000

0895D030

ITT Mackay Marine
123 TERMINAL AVE. CLARK N.J. U.S.A.

TITLE: SCHEMATIC MAJOR LOOP ANALOG AND ACQUISITION

SCALE	DRN	CHKD	DES	620580534	REV
A PRTD	ENG				A



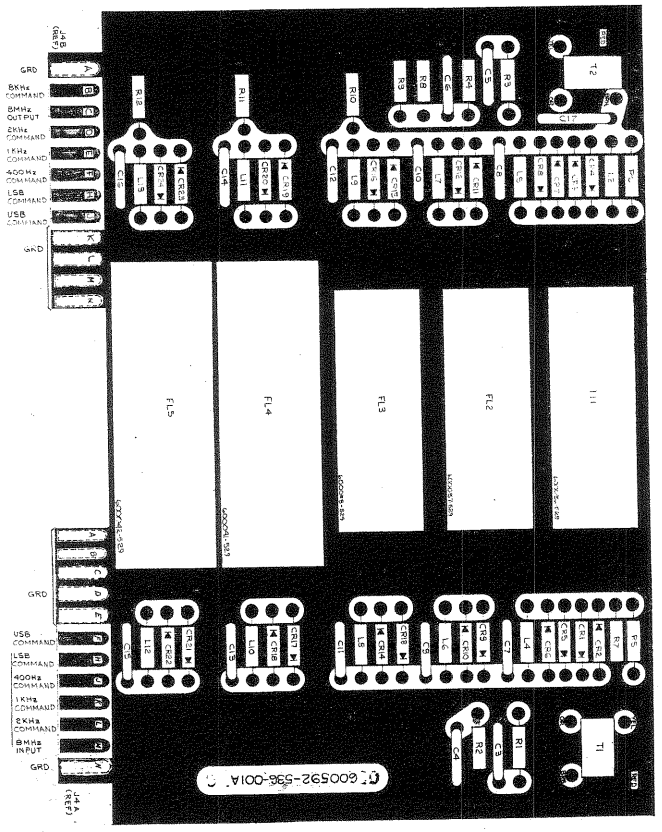
NOTES:
1-UNLESS OTHERWISE SPECIFIED;
ALL CAPACITANCE VALUES GREATER THAN 1.0 ARE IN PF.
ALL CAP VALUES 1.0 AND SMALLER ARE IN µF.
ALL INDUCTANCE VALUES µh.
ALL RESISTANCE VALUES IN OHMS.
K=1000.

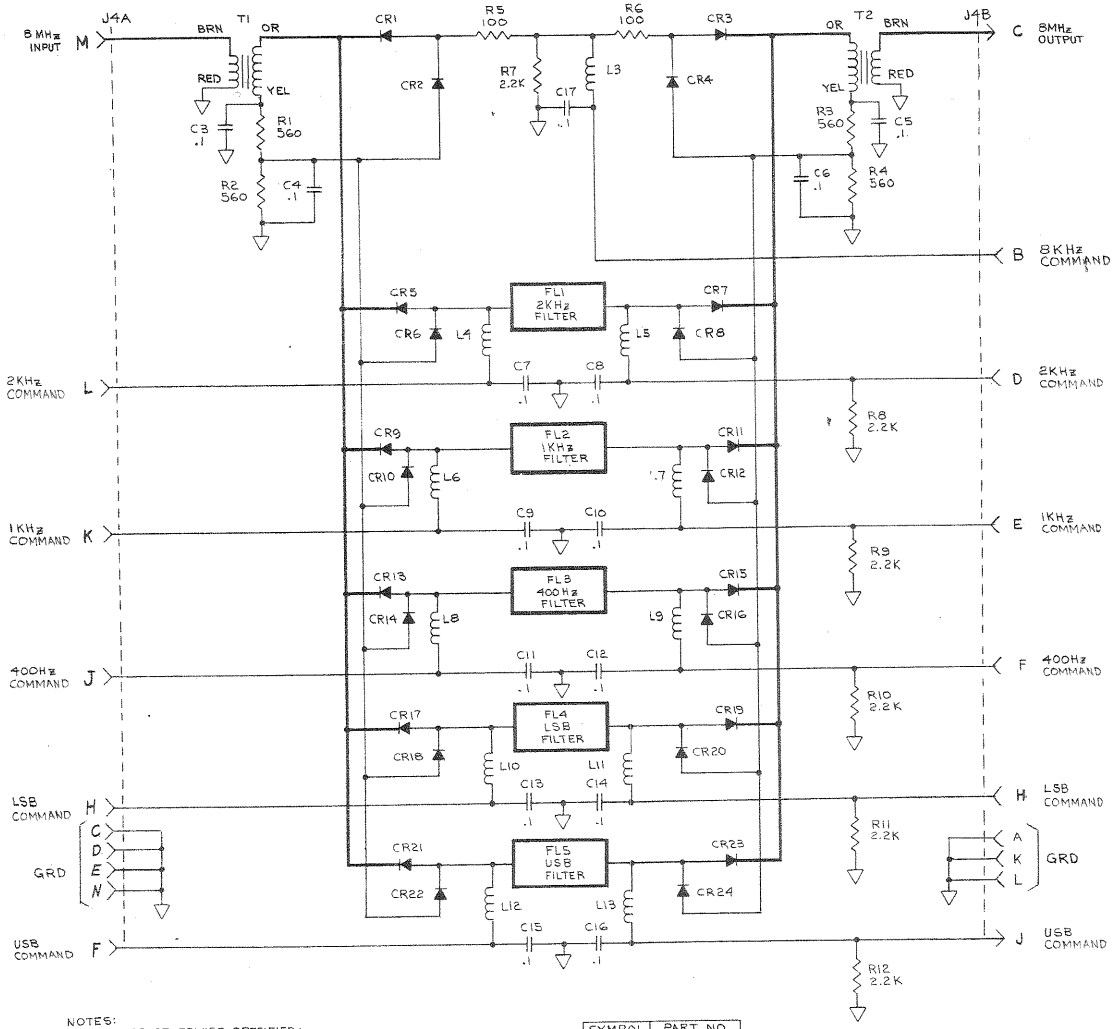
0895D039

ITT Mackay Marine
A DIVISION OF INTERNATIONAL TELEPHONE AND TELEGRAPH CORPORATION
133 TERMINAL AVE. CLARK N.J. U.S.A.

TITLE SCHEMATIC PRESELECTOR

SCALE | 620125-537 | REV A





NOTES:
1- UNLESS OTHERWISE SPECIFIED:
ALL CAPACITANCE VALUES GREATER THAN 1.0 ARE IN pf.
ALL CAP VALUES 1.0 AND SMALLER ARE IN μF.
ALL INDUCTANCE VALUES ARE 68μH.
ALL RESISTANCE VALUES IN OHMS.
ALL DIODES ARE IN4148.
K = 1000.

SYMBOL	PART NO.
T1, T2	600055-512

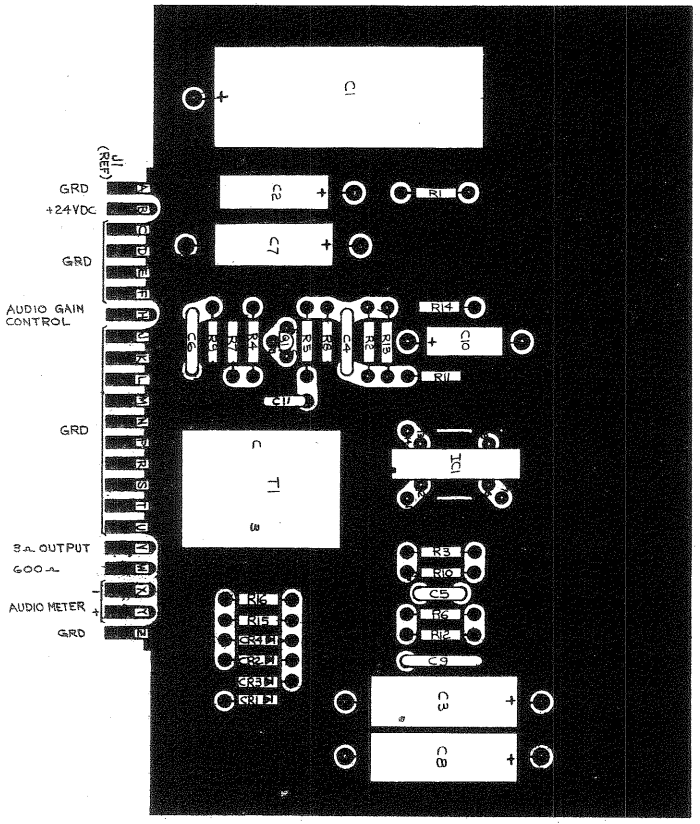
0895D024

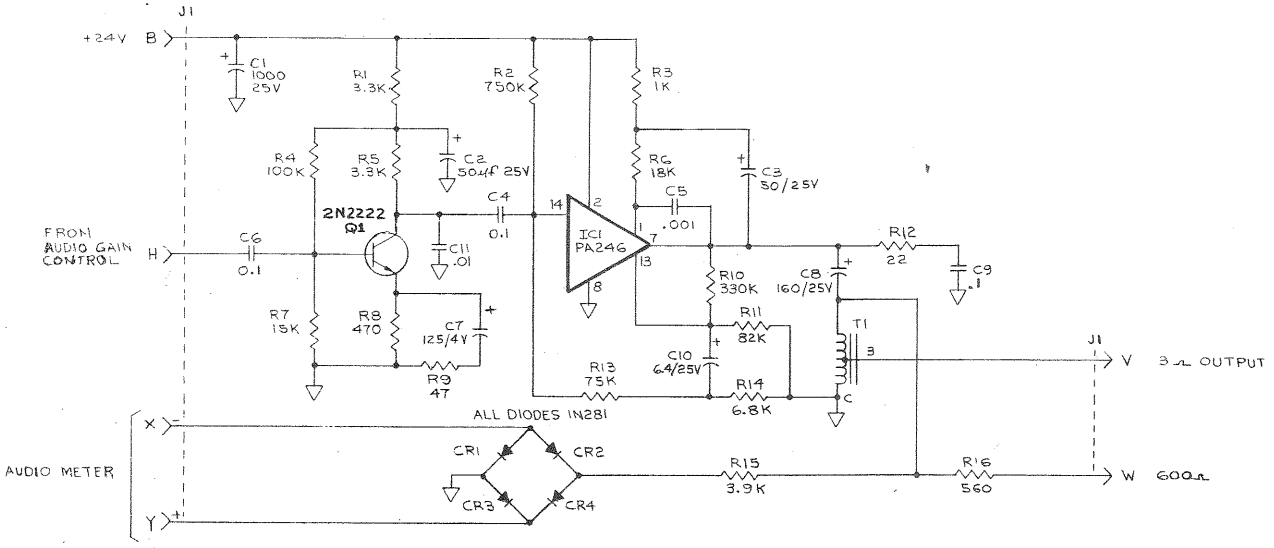
ITT Mackay Marine
133 TERMINAL AVE. CLARK N.J. U.S.A.

TITLE: SCHEMATIC INFORMATION FILTERS

SCALE: NONE | REV: A

20592-536





GRD
J1-A,C,D,E,F,J,K,L,M,N,P,R,S,T,U,Z

NOTES:
1-UNLESS OTHERWISE SPECIFIED;
ALL CAP VALUES ARE IN μF
ALL RESISTANCE VALUES IN OHMS
K = 1000

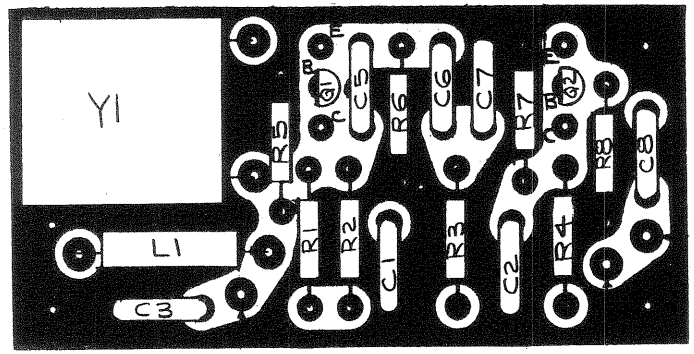
SYMBOL	PART NO.
T1	600048-512-001

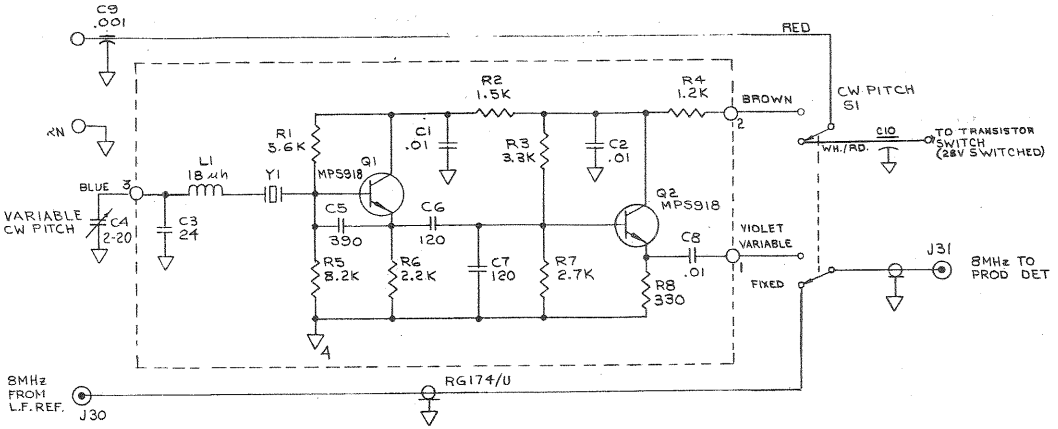
08958027

ITT Mackay Marine
(3) TERMINAL AVE. CLARK N.J. U.S.A.

TITLE: AUDIO AMPLIFIER SCHEMATIC

SCALE	APP'D	DWG	CHK'D	DRN		REV
	AP			dc	620595-536	A





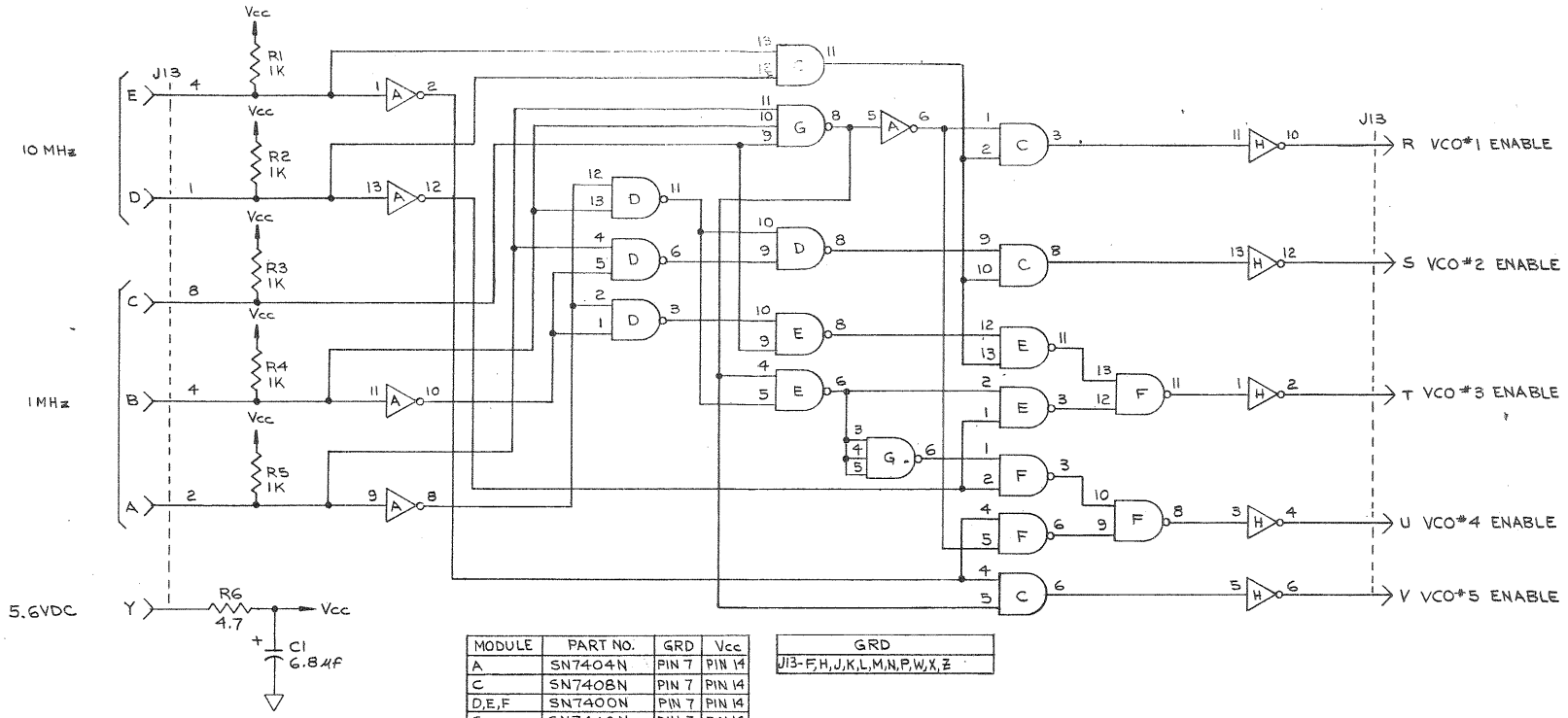
NOTES:
1-UNLESS OTHERWISE SPECIFIED;
ALL CAPACITANCE VALUES GREATER THAN 1.0 ARE IN PF
ALL CAP VALUES 1.0 AND SMALLER ARE IN µf.
ALL RESISTANCE VALUES IN OHMS.
K=1000

0895B037

ITT Mackay Marine

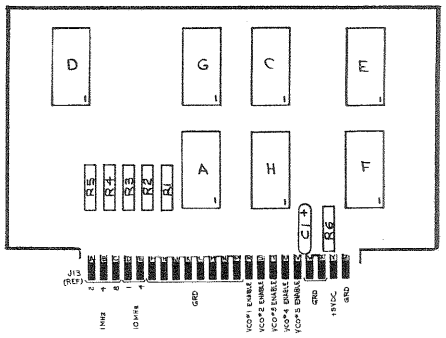
TITLE
SCHEMATIC
VARIABLE B.F.O.

SCALE | APP'D | CHK'D | DWN | 620578-3% | REV A



MODULE	PART NO.	GRD	Vcc
A	SN7404N	PIN 7	PIN 14
C	SN7408N	PIN 7	PIN 14
D,E,F	SN7400N	PIN 7	PIN 14
G	SN7410N	PIN 7	PIN 14
H	SN7406N	PIN 7	PIN 14

GRD
J13-F,H,J,K,L,M,N,P,W,X,Z



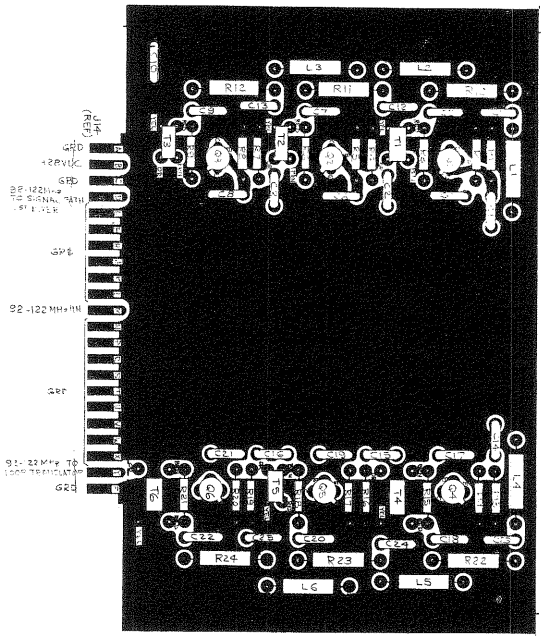
NOTES:
1- UNLESS OTHERWISE SPECIFIED; ALL RESISTANCE VALUES IN OHMS. K=1000.

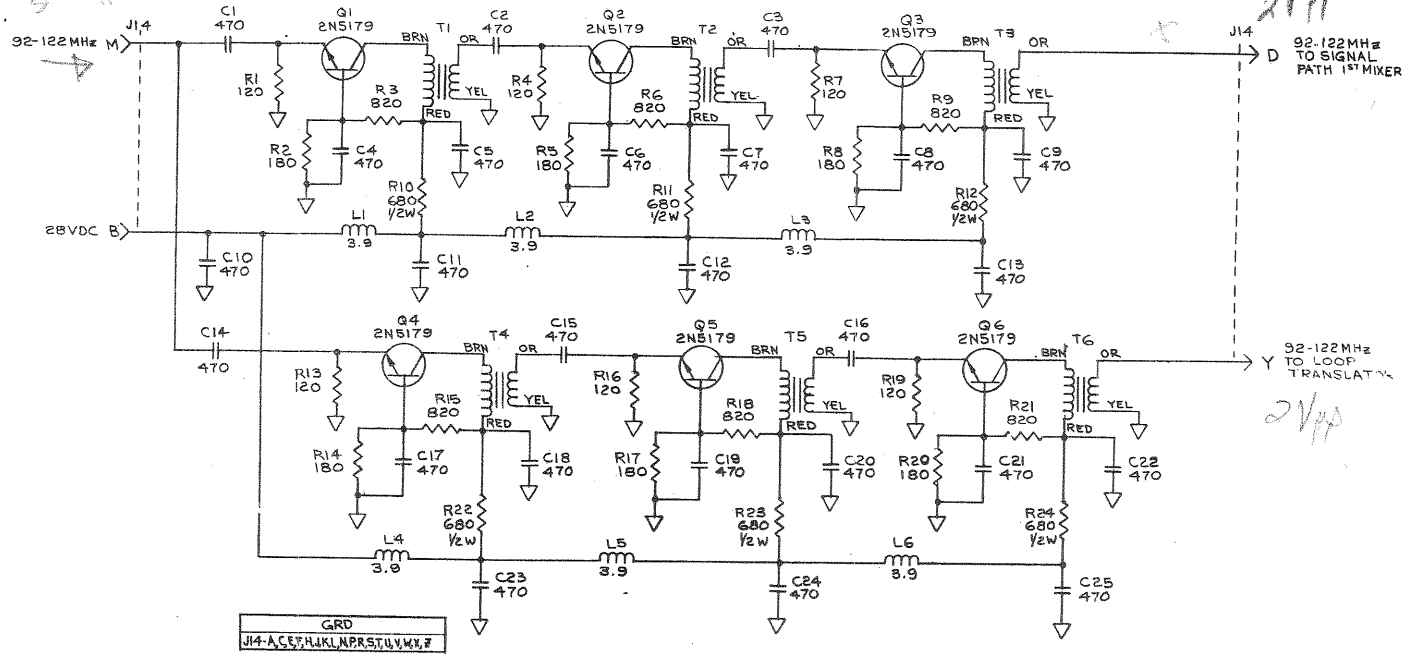
08950028

ITT Mackay Marine
ENGINEERED BY INTERNATIONAL TELEPHONE AND TELEGRAPH CORPORATION
131 TERMINAL AVE. CLARK N.J. U.S.A.

TITLE: DECODER SCHEMATIC

SCALE | APP'D | ENG | CHK'D | DRW: | 620582-536 | REV A



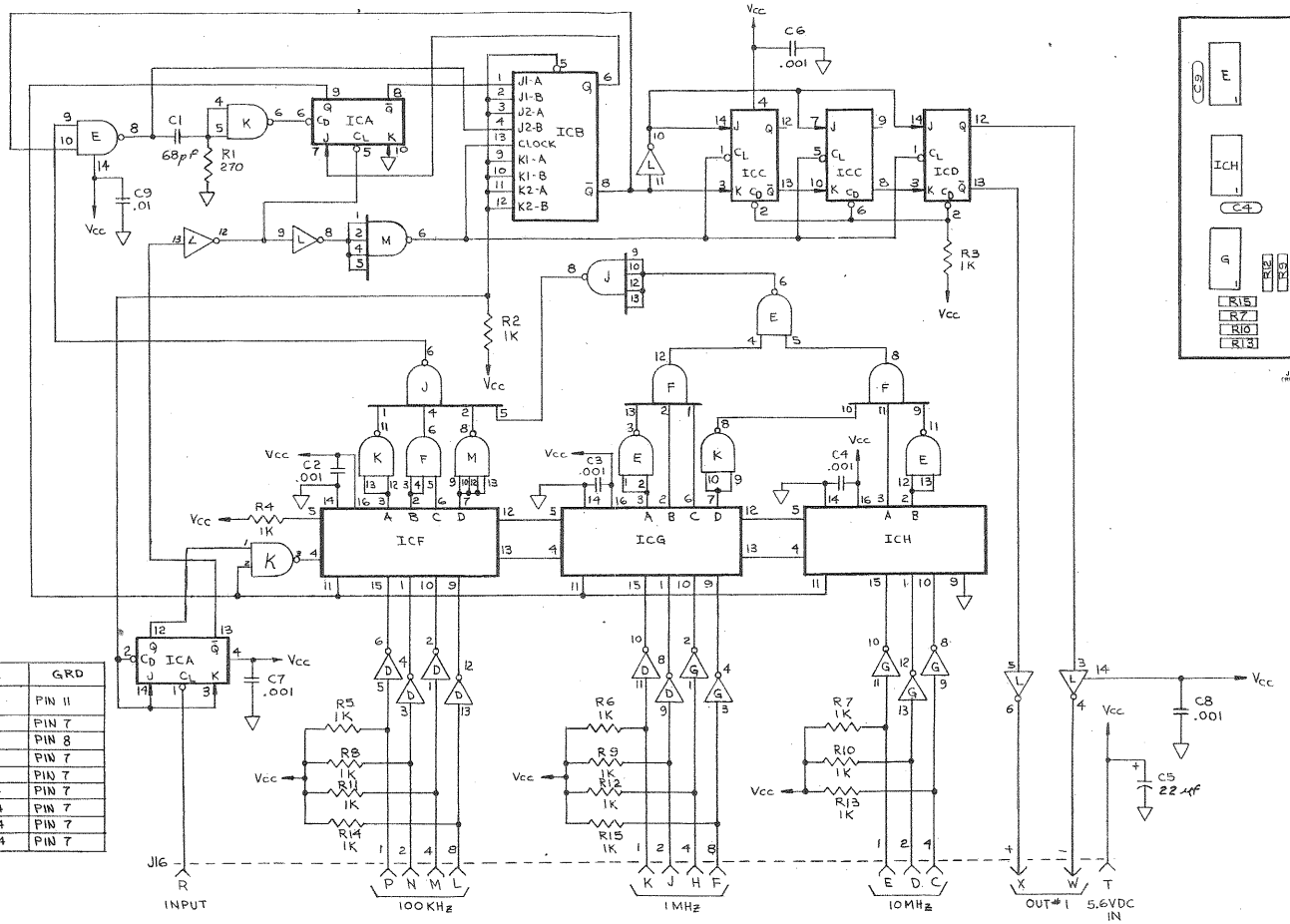


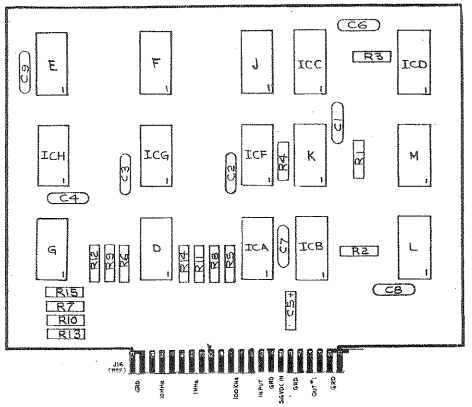
SYMBOLS	PART NO.
T1,T2,T3,T4,T5,T6	600059-512-001

NOTES:
1-UNLESS OTHERWISE SPECIFIED:
ALL CAPACITANCE VALUES ARE IN PF.
ALL INDUCTANCE VALUES IN μh.
ALL RESISTANCE IN OHMS

08950029

UTT Mackay Marine	133 TERMINAL AVE. CLARK N.J. U.S.A.
TITLE	SCHEMATIC MAJOR LOOP VCO BUFFER
SCALE	620583-534 REV. A





MODULES	PART NO.	Vcc	GRD
ICA, ICC, ICD	SN74H103N	PIN 4	PIN 11
ICB	SN74H101N	PIN 14	PIN 7
ICF, ICG, ICH	SN74192N	PIN 16	PIN 8
D, G	SN7404N	PIN 14	PIN 7
E, K	SN74H00N	PIN 14	PIN 7
F	SN74H11N	PIN 14	PIN 7
J	SN74H20N	PIN 14	PIN 7
L	SN74H04N	PIN 14	PIN 7
M	SN74H40N	PIN 14	PIN 7

GRD
J16-A, B, S, U, V, Y, Z

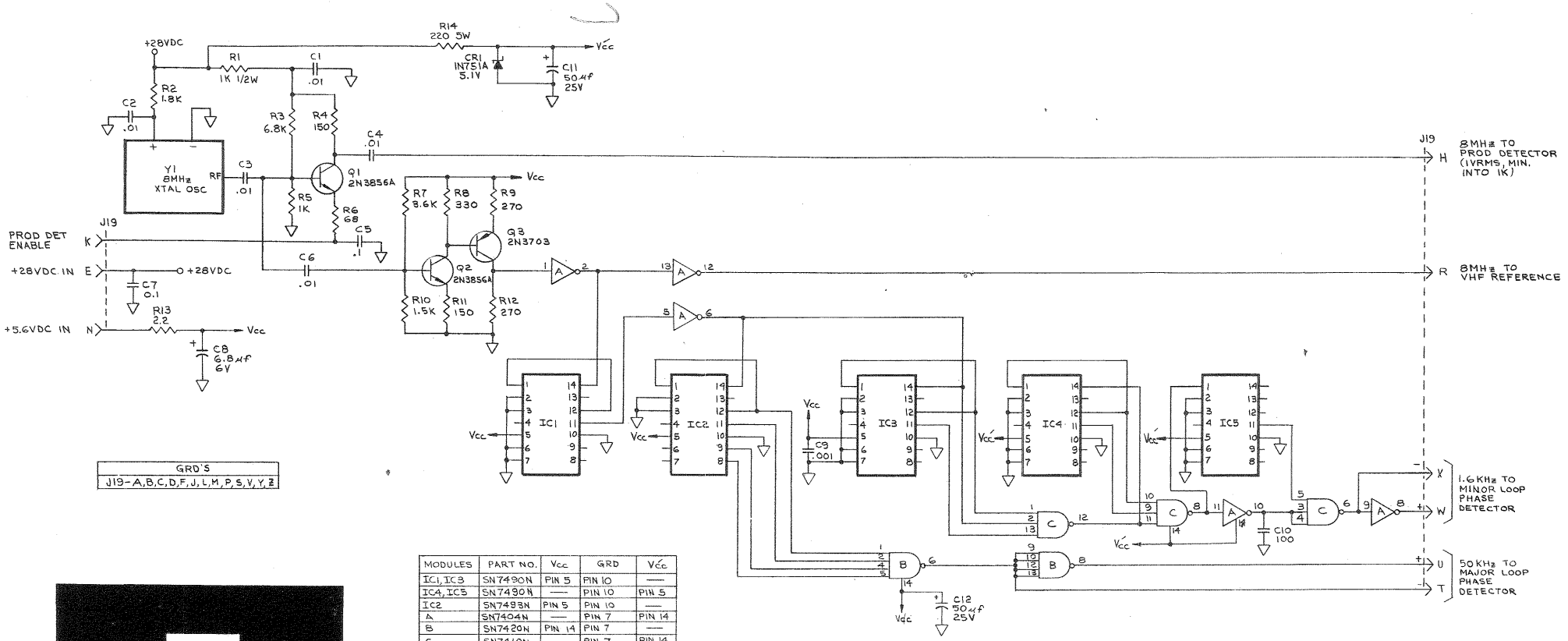
NOTES:
1- UNLESS OTHERWISE SPECIFIED;
ALL RESISTANCE VALUES IN OHMS
K=1000

0895D031

ITT Mackay Marine

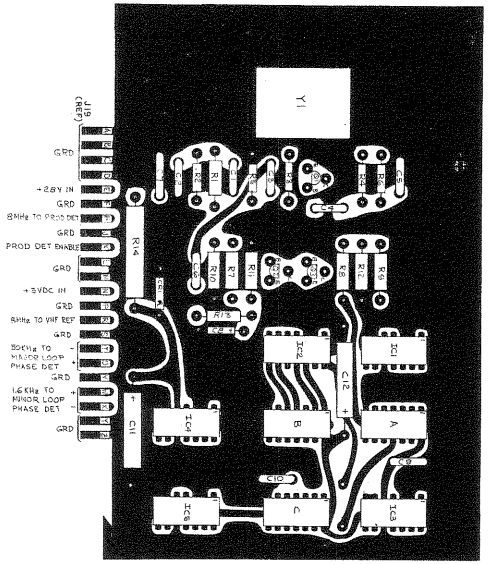
TITLE: SCHEMATIC
MAJOR LOOP
VARIABLE DIVIDER

SCALE: NONE | 220584-536 | REV: A



GRD'S
J19-A,B,C,D,F,J,L,M,P,S,V,Y,Z

MODULES	PART NO.	Vcc	GRD	Vcc
IC1, IC3	SN7490N	PIN 5	PIN 10	—
IC4, IC5	SN7490N	—	PIN 10	PIN 5
IC2	SN7493N	PIN 5	PIN 10	—
A	SN7404N	—	PIN 7	PIN 14
B	SN7420N	PIN 14	PIN 7	—
C	SN7410N	—	PIN 7	PIN 14



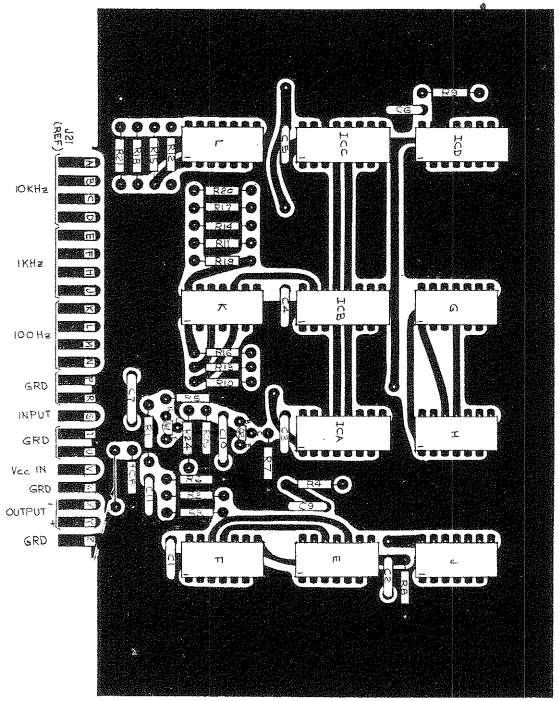
NOTES:
1. UNLESS OTHERWISE SPECIFIED;
   ALL CAPACITANCE VALUES GREATER THAN 1.0 ARE µF
   ALL CAP VALUES 1.0 AND SMALLER ARE IN µF
   ALL RESISTANCE VALUES IN OHMS
   K= 1000

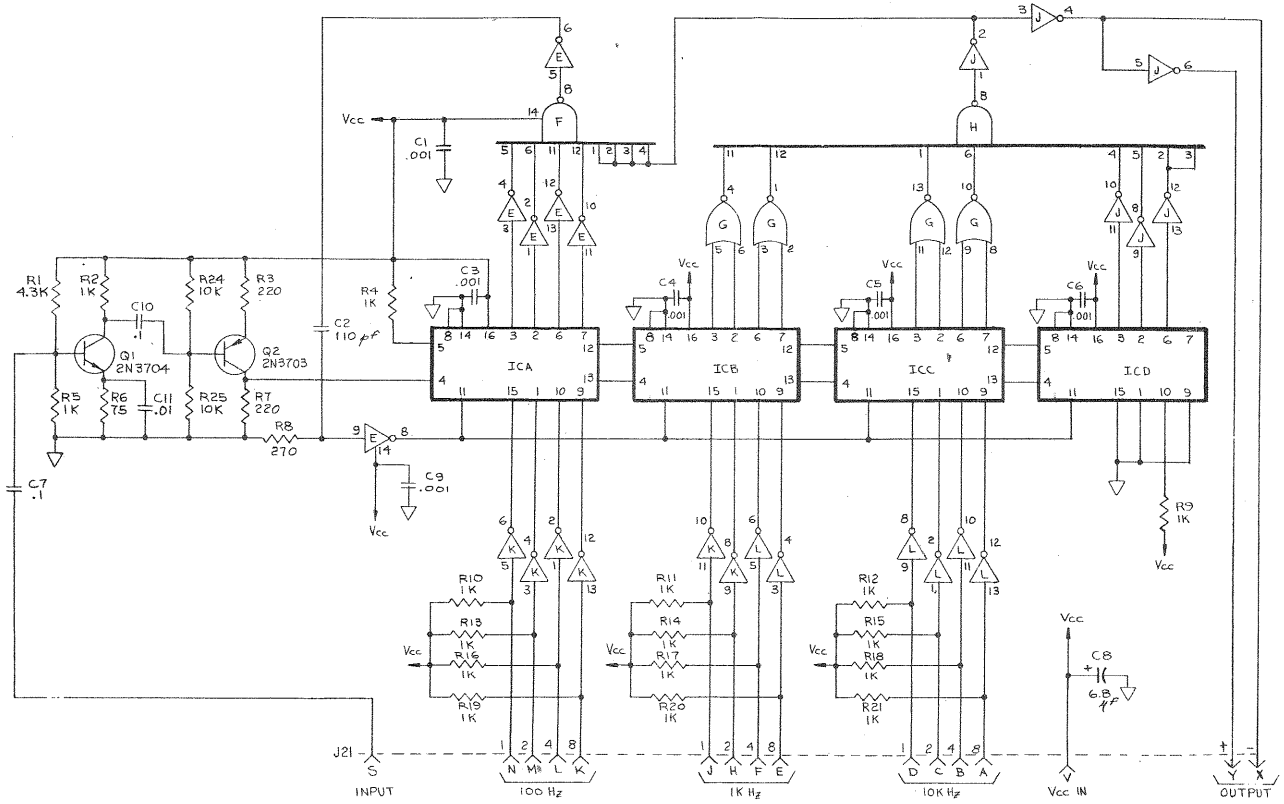
0895D034

ITT Mackay Marine
(33 TERMINAL AVE. CLARK N.J. U.S.A.

TITLE: SCHEMATIC
LOW FREQUENCY
REFERENCE

SCALE | APPD | CHKD | DWN | 420587-536 | REV A





NOTES:
1- UNLESS OTHERWISE SPECIFIED:
ALL CAP VALUES 1.0 AND SMALLER ARE IN uf
ALL RESISTANCE VALUES IN OHMS
K = 1000

MODULES	PART NO.	Vcc	GRD
ICA, ICB ICC, ICD	SN74192N	PIN 16	PIN 14,8
E	SN74H04N	PIN 14	PIN 7
F	SN74H30N	PIN 14	PIN 7
G	SN7402N	PIN 14	PIN 7
J, K, L	SN7404N	PIN 14	PIN 7
H	SN7430N	PIN 14	PIN 7

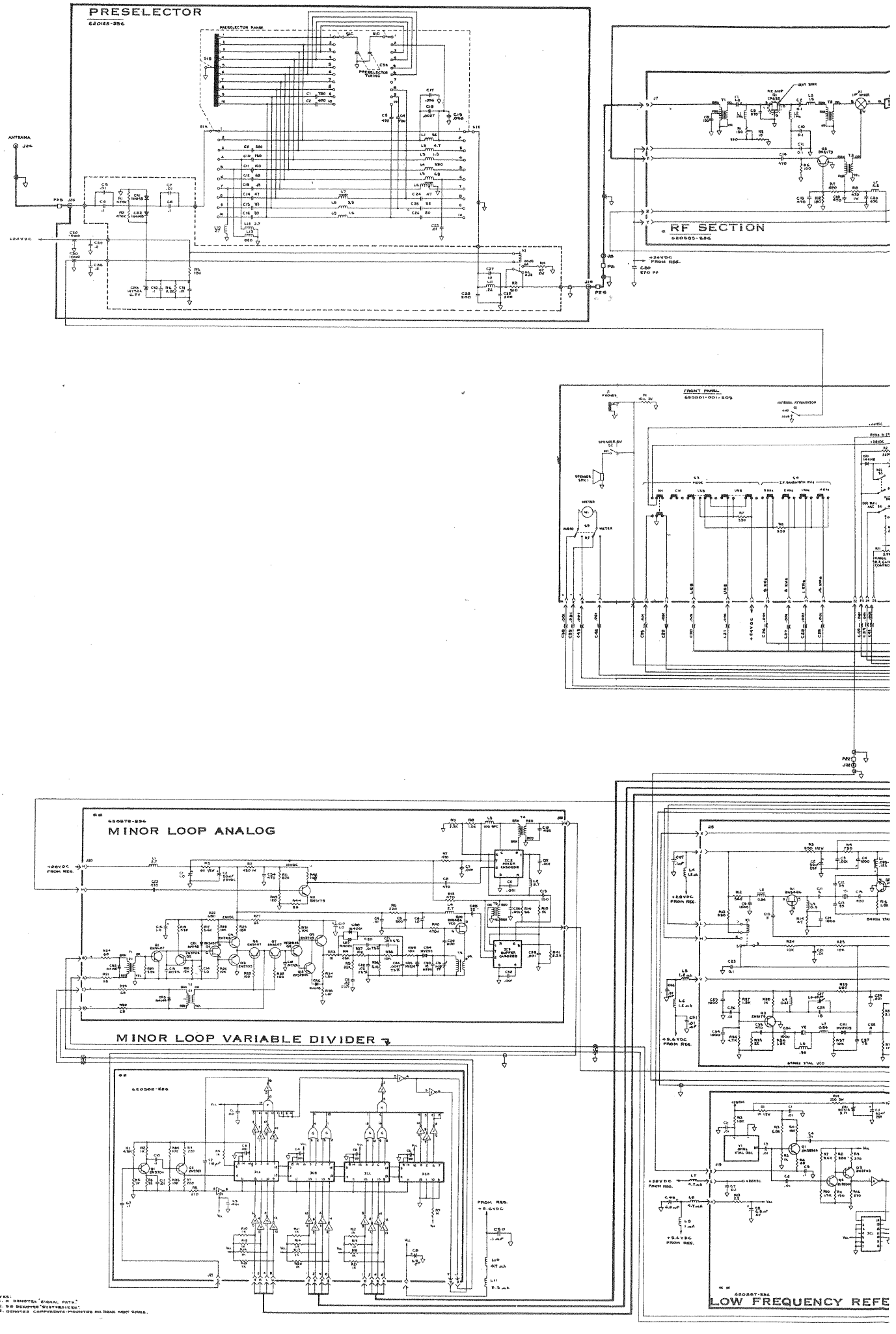
GRD
J21-P,R,T,U,W,Z

0895D036

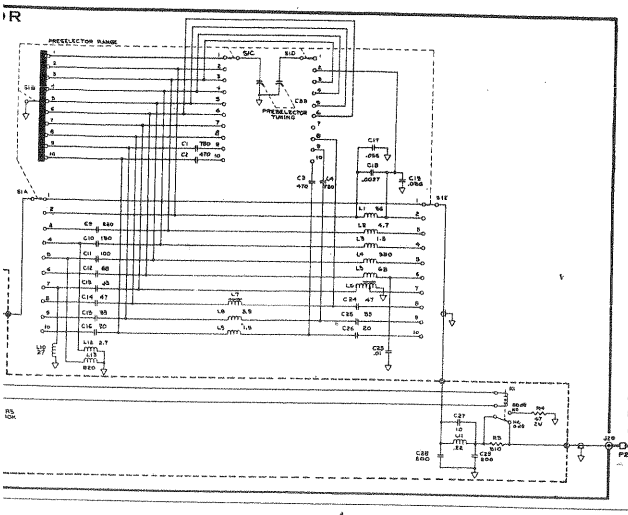
ITT Mackay Marine
123 TERHUNE AVE. CLARE N.J. U.S.A.

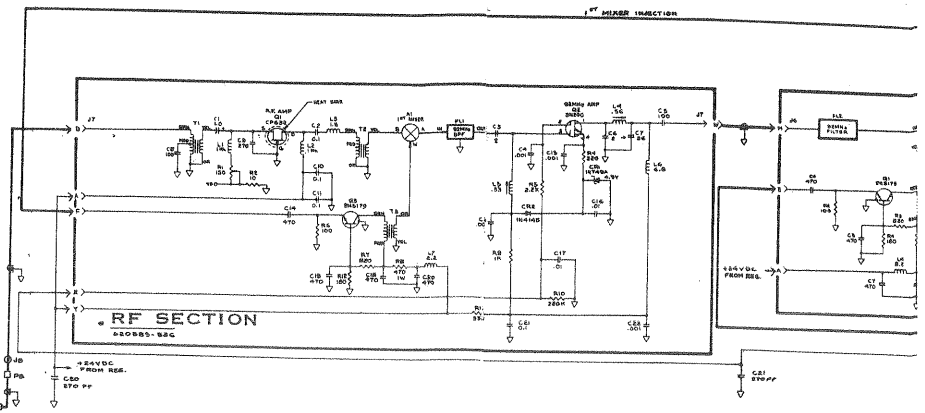
TITLE: SCHEMATIC
MINOR LOOP VARIABLE DIVIDER

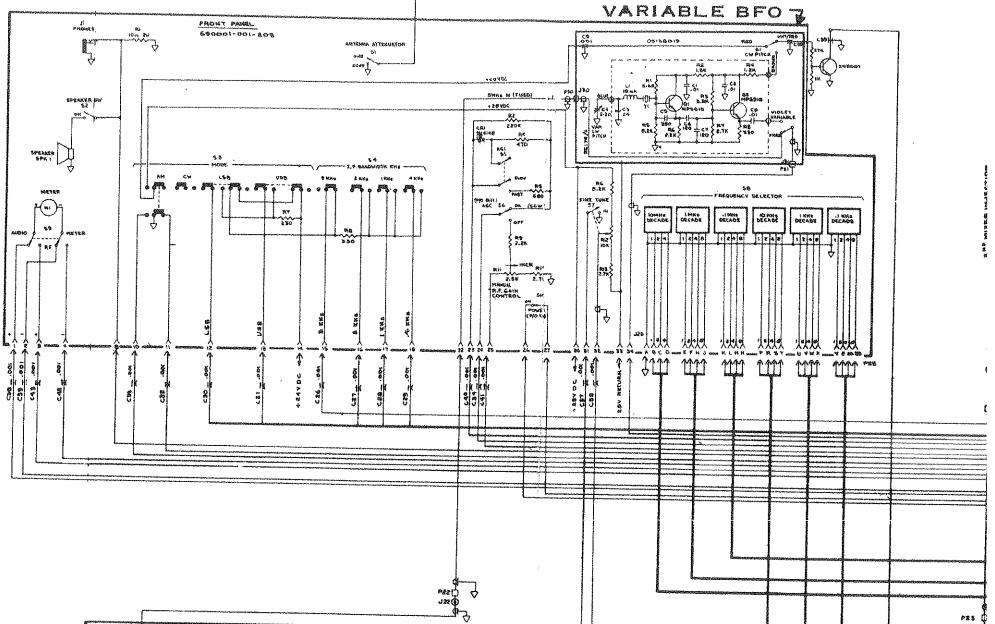
SCALE: NONE | REV: A

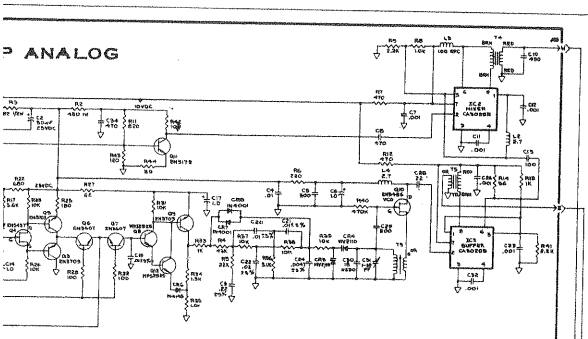


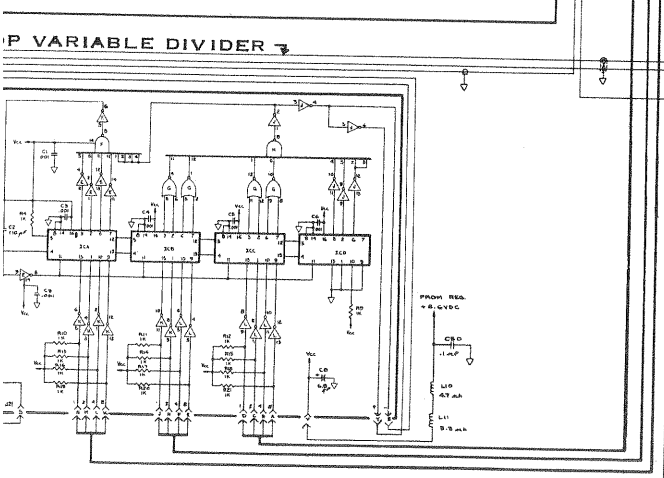
NOTES:
1. ⊕ DENOTES "SIGNAL PATH."
2. S.S. DENOTES "SYNTHESIZER."
3. ▭ DENOTES COMPONENTS MOUNTED ON REAR PANEL SWGS.

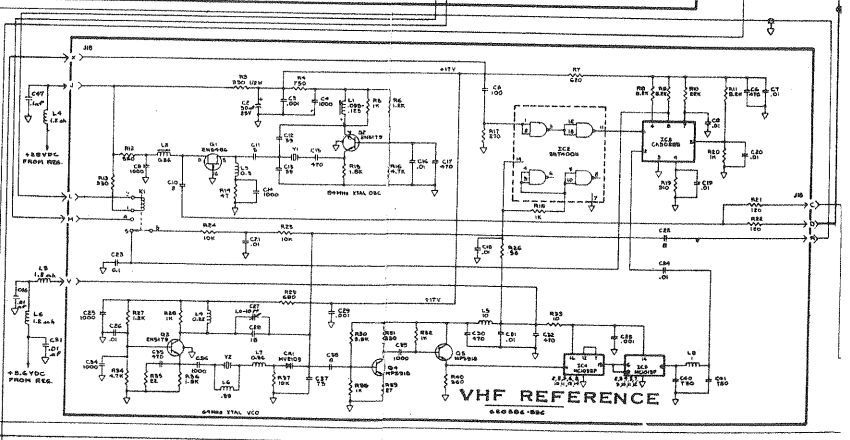

PRESELECTOR RANGE
PRESELECTOR TUNING

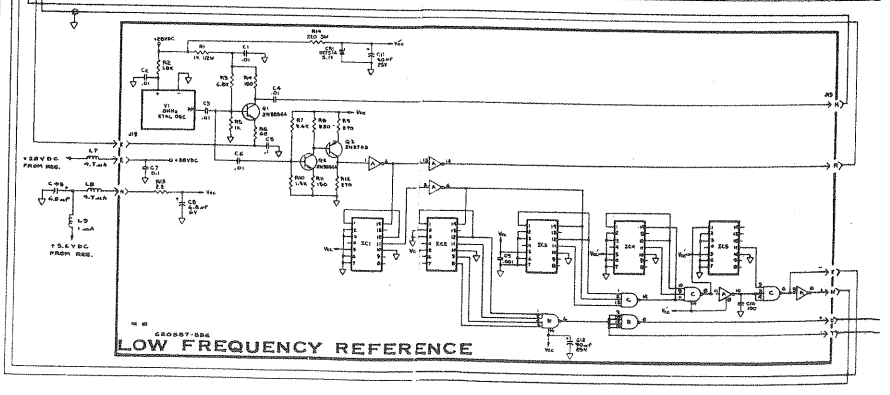

1ST MIXER INJECTION
RF SECTION
620585-526
+24VDC FROM REG.

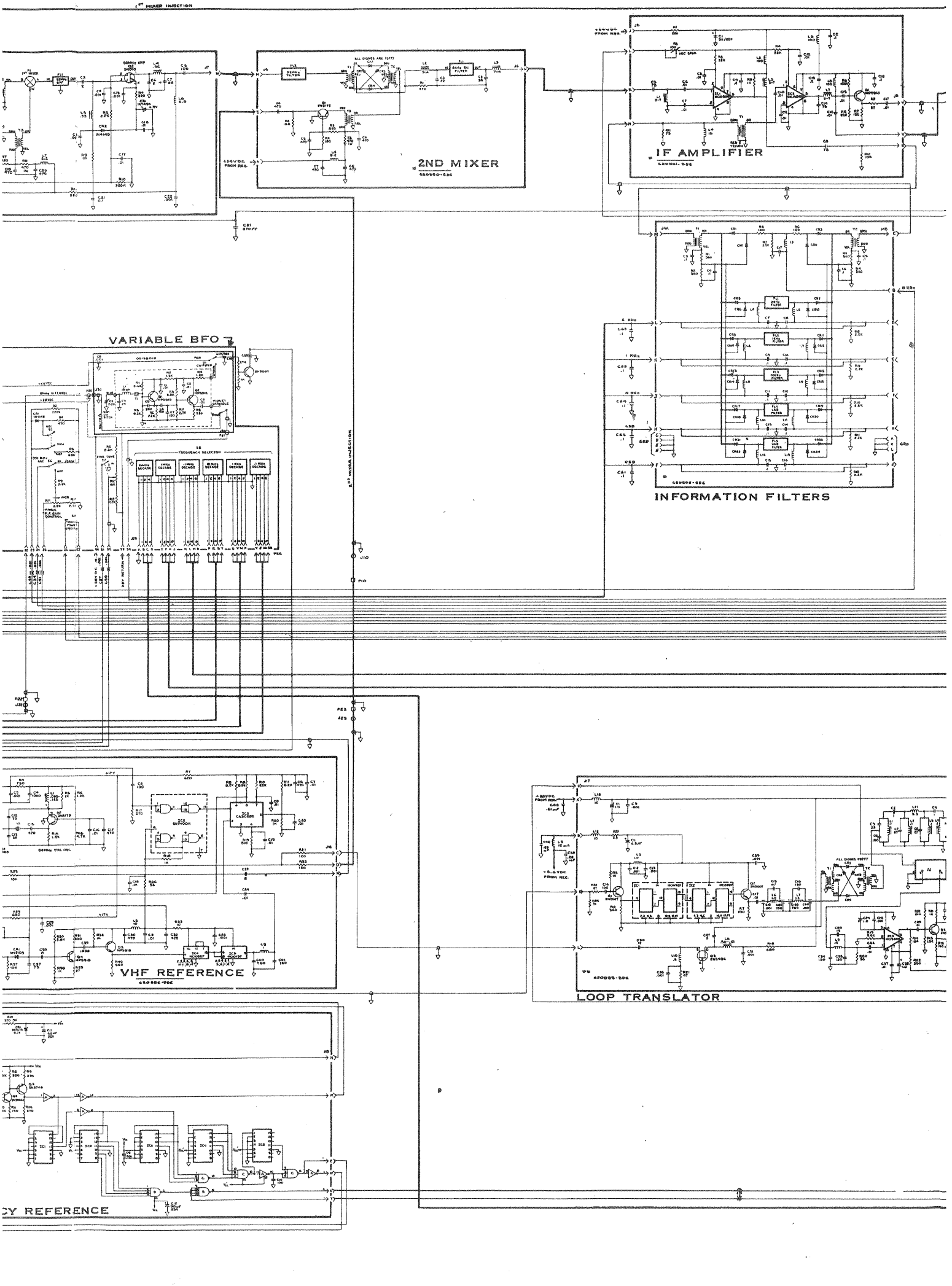

VARIABLE BFO
FRONT PANEL
690001-001-205
FREQUENCY SELECTOR

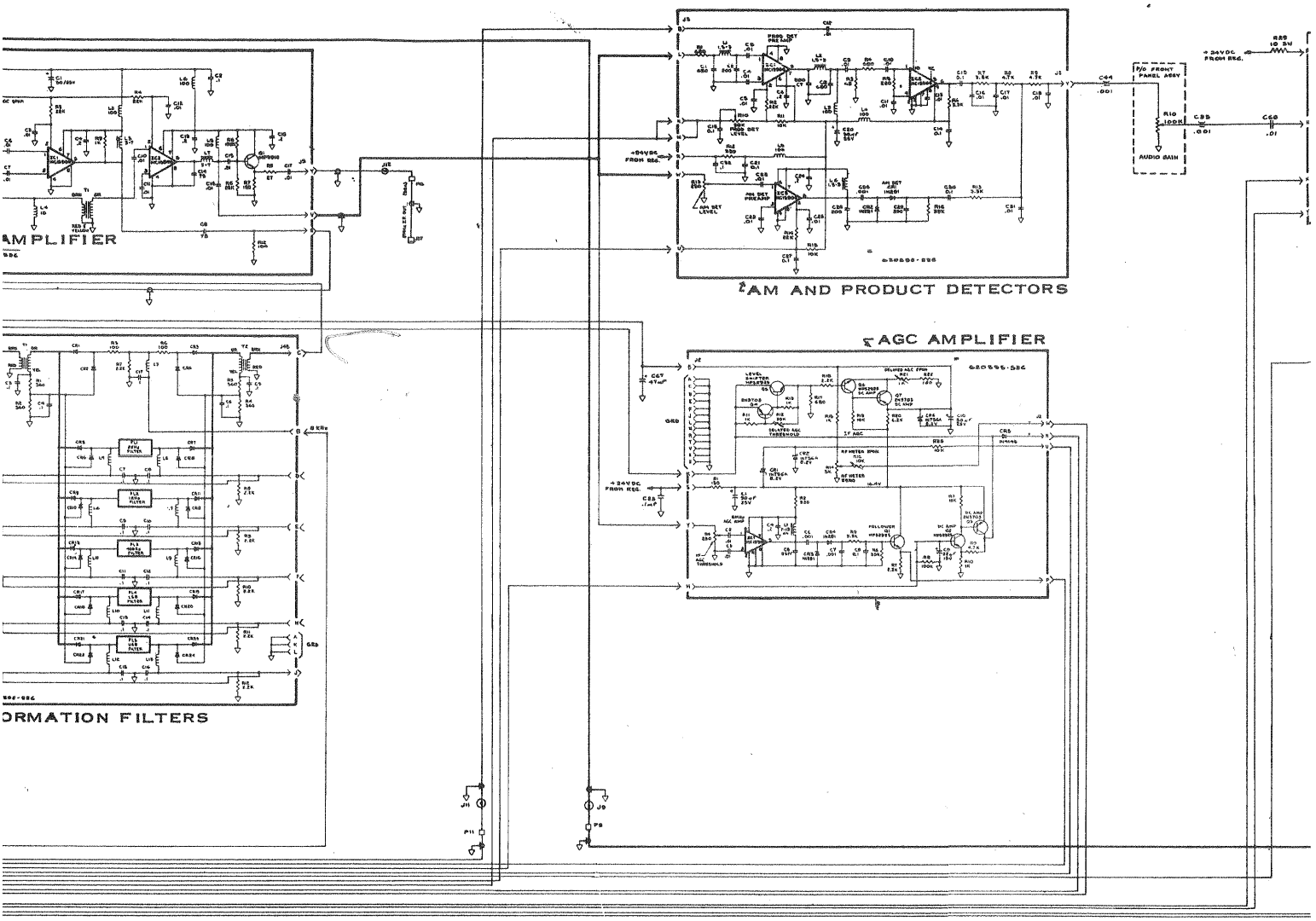

ANALOG

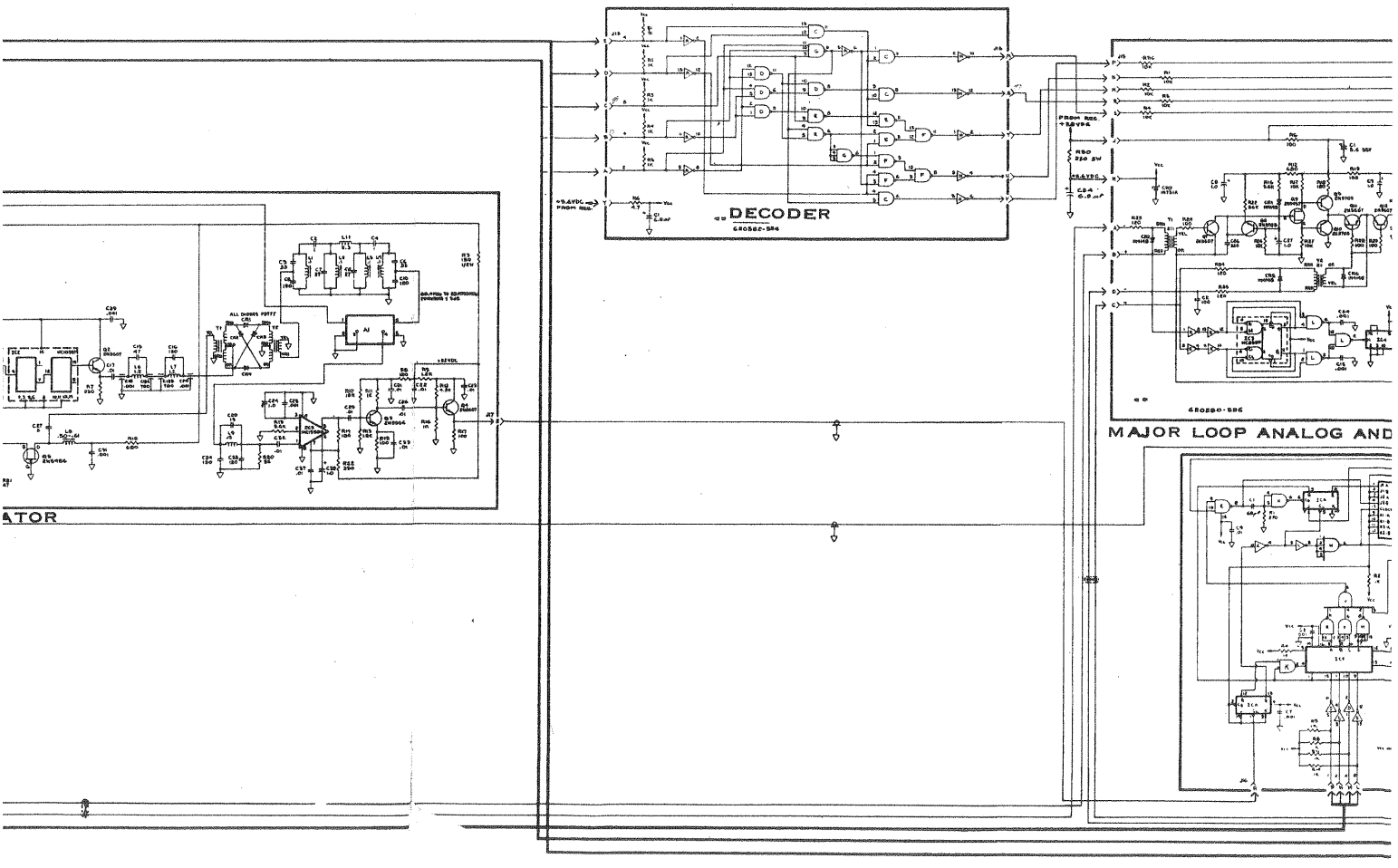

VARIABLE DIVIDER
FROM REG. +8.6VDC

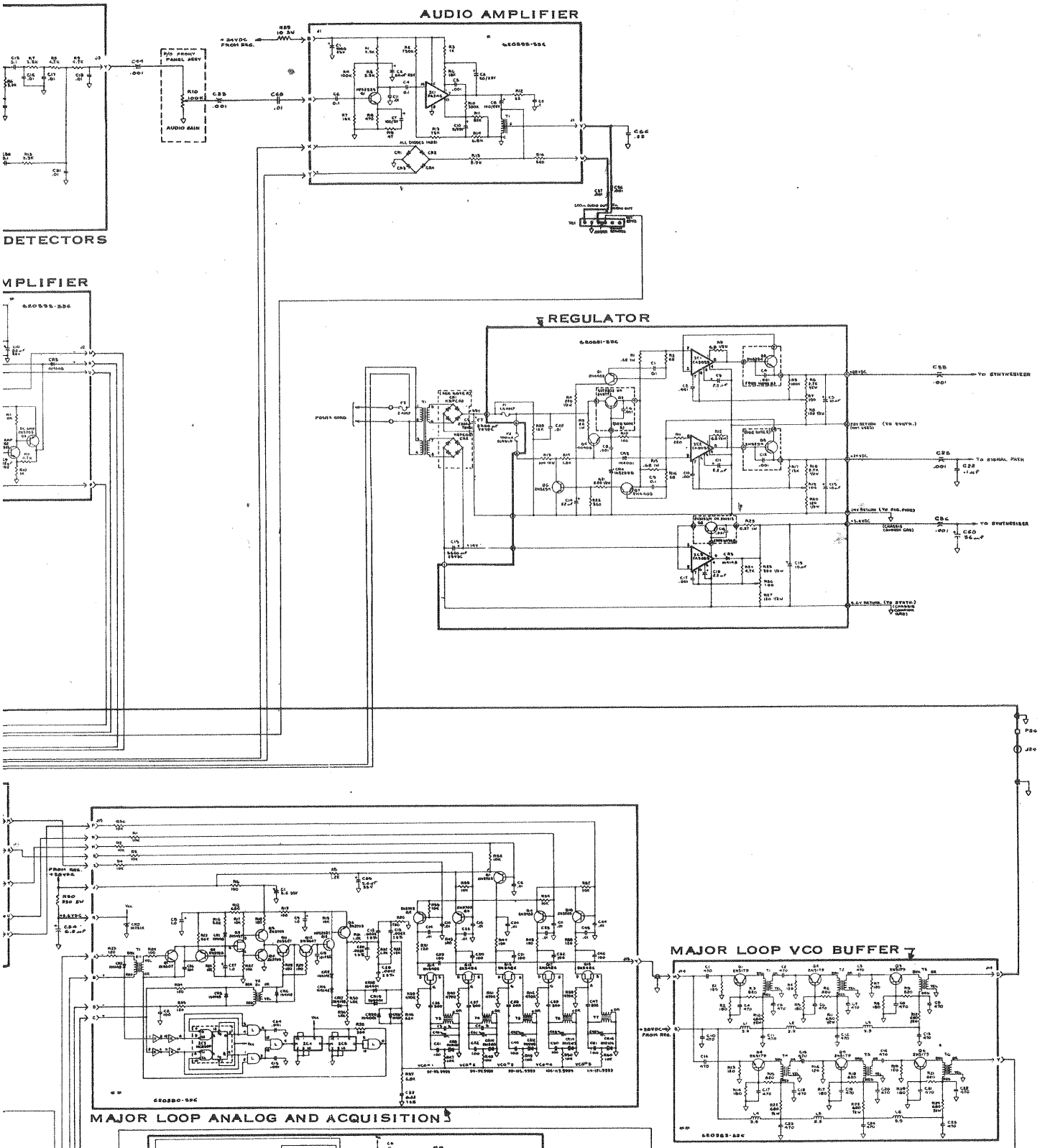

VHF REFERENCE
620584-526


LOW FREQUENCY REFERENCE
620587-526

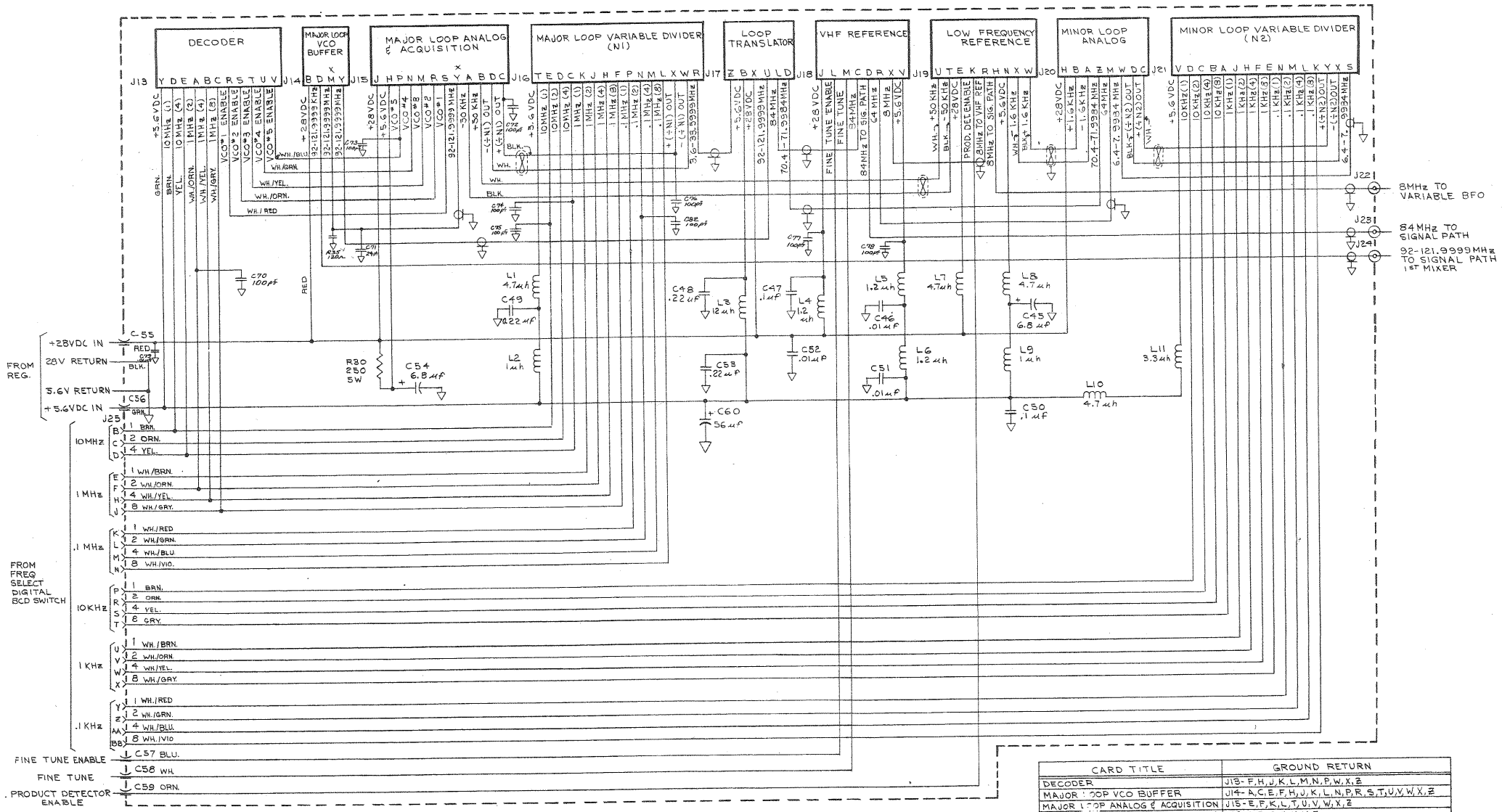

1ST MIXER INJECTION
2ND MIXER
IF AMPLIFIER
INFORMATION FILTERS
VARIABLE BFO
2ND MIXER INJECTION
VHF REFERENCE
LOOP TRANSLATOR
CY REFERENCE


AMPLIFIER
AM AND PRODUCT DETECTORS
AGC AMPLIFIER
ORMATION FILTERS
+24VDC FROM REG.
AUDIO GAIN
P/O FRONT PANEL ASSY


DECODER
MAJOR LOOP ANALOG AND
ATOR



3020A Receiver Schematic Diagram.



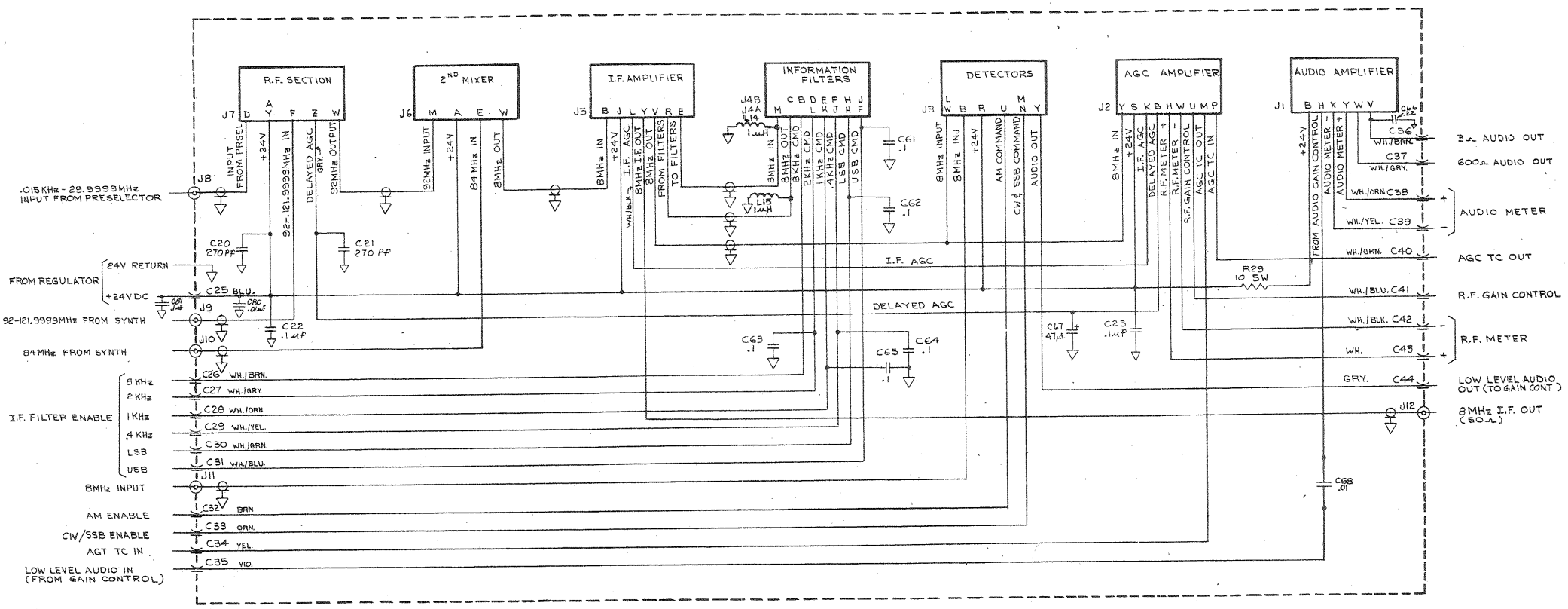
CARD TITLE	GROUND RETURN
DECODER	J13- F,H,J,K,L,M,N,P,W,X,Z
MAJOR LOOP VCO BUFFER	J14- A,C,E,F,H,J,K,L,N,P,R,S,T,U,V,W,X,Z
MAJOR LOOP ANALOG & ACQUISITION	J15- E,F,K,L,T,U,V,W,X,Z
MAJOR LOOP VARIABLE DIVIDER (N1)	J16- A,B,S,U,V,Y,Z
LOOP TRANSLATOR	J17- A,C,E,F,H,J,K,M,N,P,R,S,T,V,W,Y
VHF REFERENCE	J18- A,B,E,F,H,K,N,P,S,T,U,W,Y,Z
LOW FREQUENCE REFERENCE	J19- A,B,C,D,F,J,L,M,P,S,V,Y,Z
MINOR LOOP ANALOG	J20- E,F,J,K,L,N,P,R,S,T,U,V,X,Y
MINOR LOOP VARIABLE DIVIDER(N2)	J21- P,R,T,U,W,Z

0895D807

ITT Mackay Marine
123 TERMINAL AVE. CLARK, N.J. U.S.A.

TITLE: FRAME WIRING DIAGRAM
FREQUENCY SYNTHESIZER

SCALE: NONE | DWN: RD | CHKD: | 690001-001-251 | REV: A



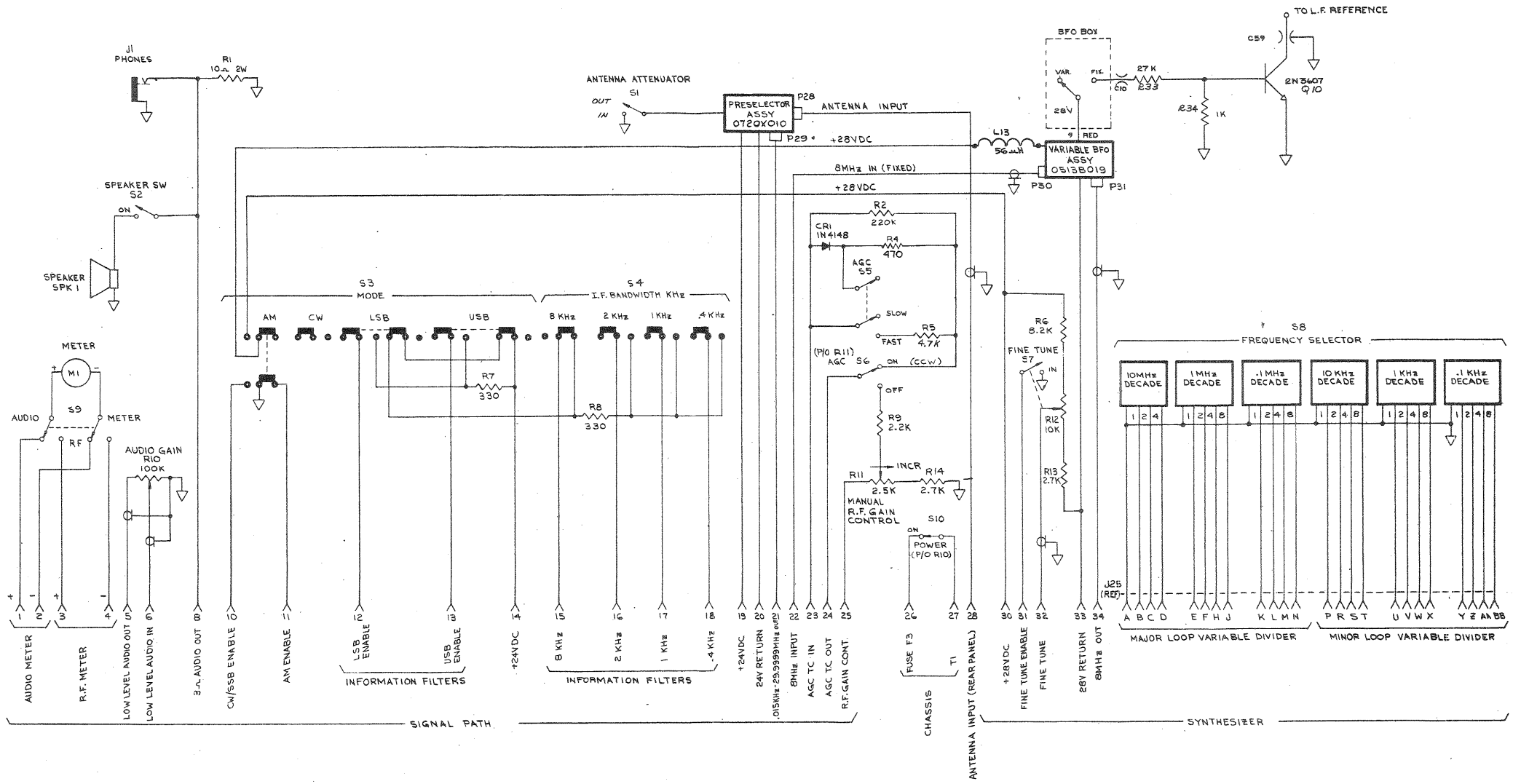
TITLES	GRD
R.F. SECTION	J7- B,C,E,H,J,K,L,M,N,P,R,S,T,U,V,X
2ND MIXER	J6-B,C,D,F,H,J,K,L,N,P,R,S,T,U,V,X,Y,Z
I.F. AMPLIFIER	J5-A,C,D,F,H,K,M,N,P,S,T,U,W,X,Z
INFO FILTER	J4A-C,D,E,N J4B - A,K,L
DETECTORS	J3-A,C,D,E,F,H,J,K,P,S,T,V,X,Z
AGC AMP.	J2- A,C,D,E,F,J,L,N,R,T,V,X,Z
AUDIO AMP	J1- A,C,D,E,F,J,K,L,M,N,P,R,S,T,U,Z

0895D806

ITT Mackay Marine

TITLE: FRAME WIRING DIAGRAM SIGNAL PATH

SCALE | 690001- | REV
APP'D | ENG | CHK'D | 001-202 | B



NOTES:

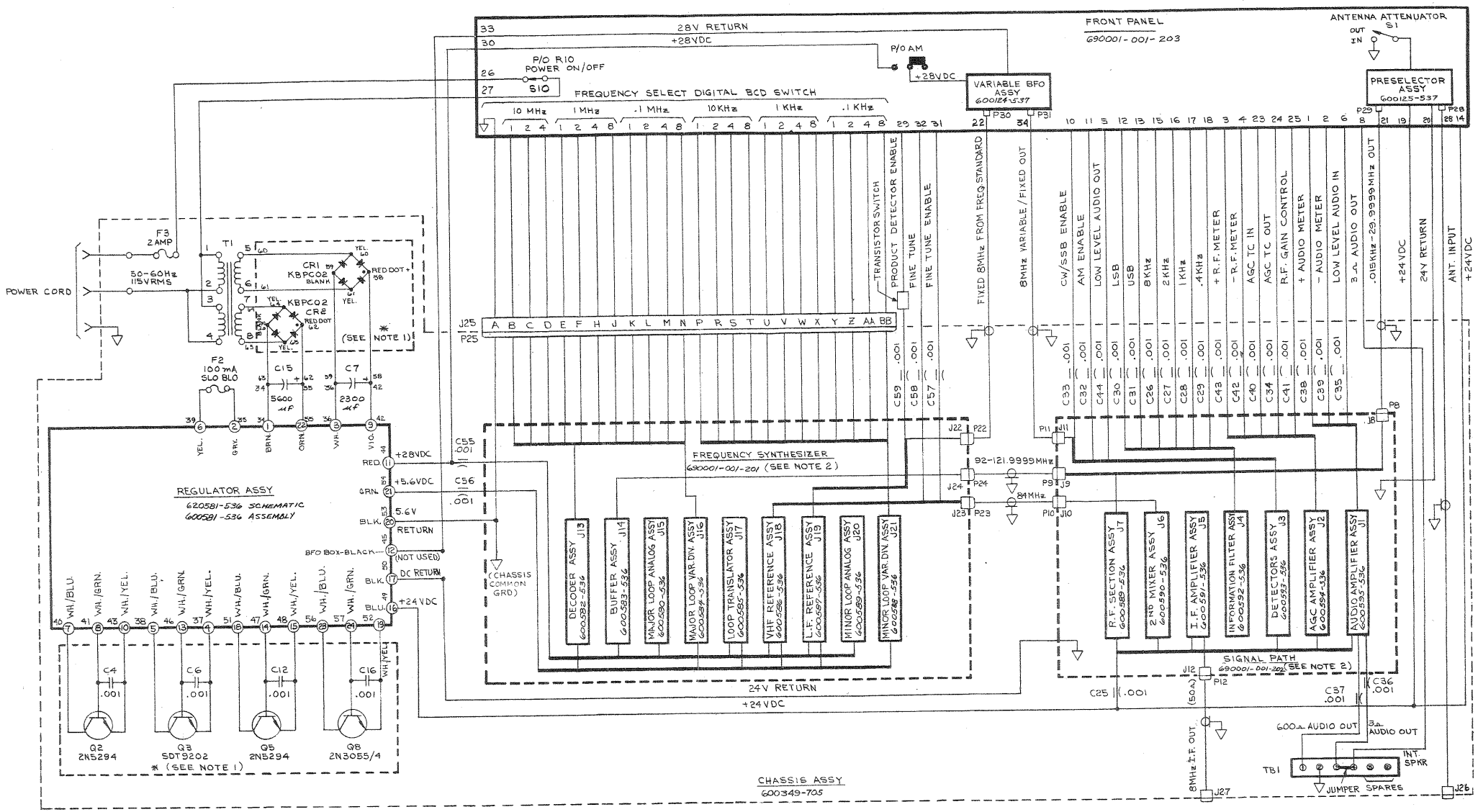
1- ALL SLIDE SWITCHES IN ⟶ OUT ⟵
2- MODE, I.F. BANDWIDTH AND AGC SWITCHES INTERLOCK.
3- UNLESS OTHERWISE SPECIFIED:
ALL RESISTANCE IN OHMS
K=1000

0895D805

ITT Mackay Marine

TITLE: SCHEMATIC FRONT PANEL

SCALE | DRWG NO. 690001-005-203 | REV A



NOTES
1- * DENOTES COMPONENTS MOUNTED ON REAR HEAT SINKS.
2- FOR DETAIL WIRING OF J1 THRU J23 SEE DRAWINGS 690001-001-202 AND 690001-001-201.

0895D808

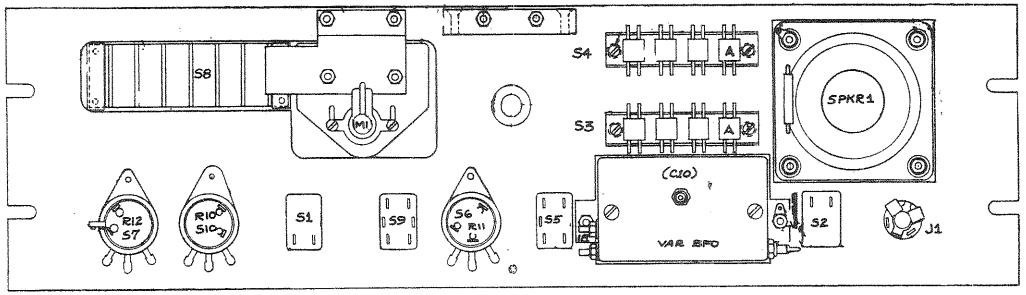
ITT Mackay Marine

TITLE INTERCONNECTION DIAGRAM 3020A

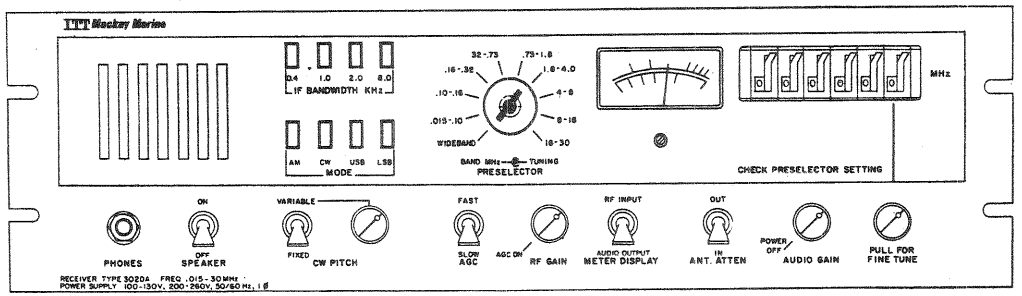
SCALE — 690001-015 REV A

FRONT PANEL: REPLACEABLE PARTS

Item	Part Number
Variable BFO	600124-537-001
Switch assembly wired (S3-S4)	600174-713-001
Mini-lever switch assembly (S3-S4)	600175-713-001
RF and Audio meter	600017-368-001
Potentiometer, 100 KΩ (2W, with SPDT switch) (S10)	600068-360-001
Potentiometer, 2.5 KΩ (2W, with SPDT switch) (S6)	600069-360-001
Potentiometer, 10 KΩ (2W, with SPDT switch) (S7)	600070-360-001
SPST toggle switch (S1, S2)	600117-616-001
DPDT toggle switch (S5, S9)	600117-616-002
Control knob (4)	600101-618-001
Head phone jack	600046-611-001
Speaker (3 by 3 inches) (SPKR 1)	600007-570-001
56-μH choke (L13)	600119-376-022



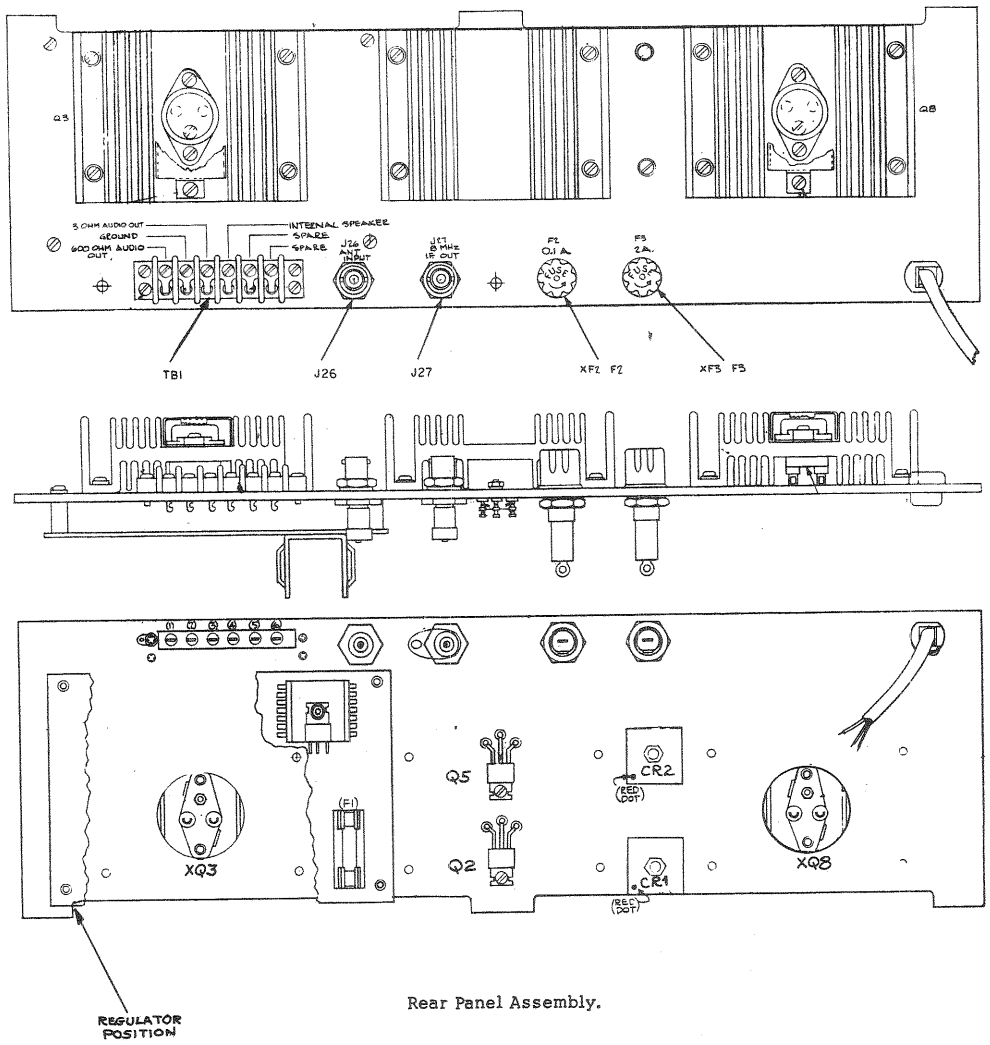
Reverse of Front Panel.



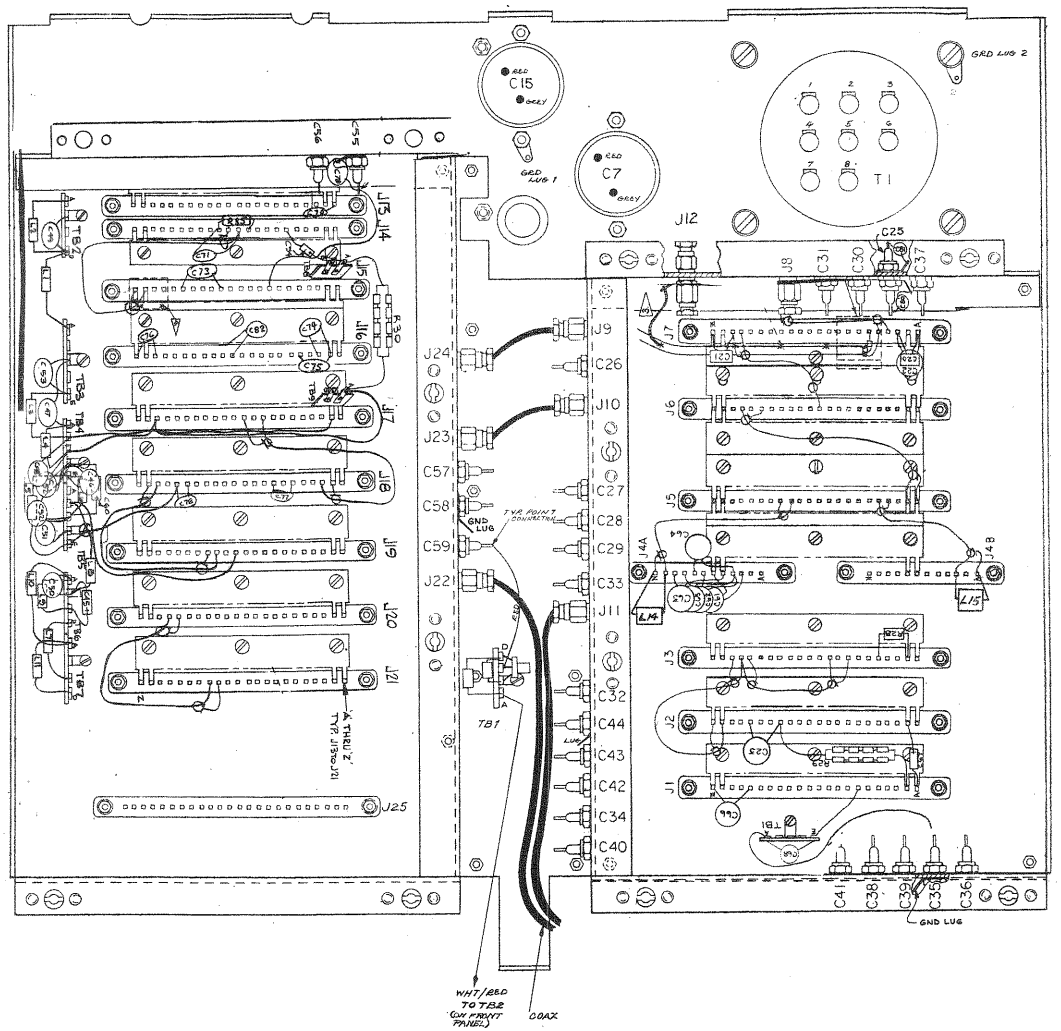
Front Panel Controls.

REAR PANEL: REPLACEABLE PARTS

Item	Description	Part Number
	Heat sink	601428-602-001
Regulator	Printed circuit card	600581-536-001
CR1, CR2	Rectifier bridge	600027-416-001
F1	(On Regulator Board)	
F2, F3	0.1A slo-blo fuse	600006-396-004
XF2, XF3	Fuseholder	600014-613-001
J26	Jack (BNC, bulkhead)	600193-606-001
J27	Jack (BNC, bulkhead)	600014-606-001
Q2	NPN transistor (1N5294)	600178-413-001
Q3	NPN transistor (SDT-9202)	600187-413-001
Q5	Same as Q2	
Q8	NPN transistor (2N3055/4)	600188-413-001
XQ3	Transistor socket	600062-419-001
XQ8	Transistor cover	601423-602-001
	Power cord	600055-102-001
TB1	Terminal board	600099-631-002



Rear Panel Assembly.



Main Chassis Assembly.

CHASSIS ASSEMBLY: REPLACEABLE PARTS

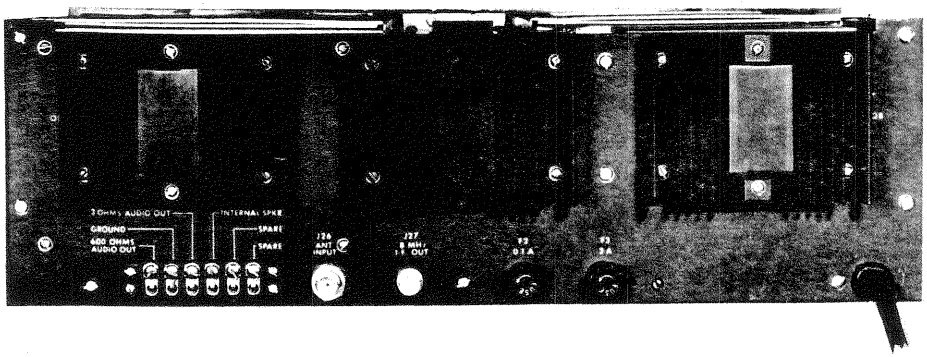
Item	Description	Part Number
T1	Power transformer	600047-512-001
C7	2300 µf, 75V	600183-314-003
C15	5600 µf, 25V	600184-314-004
	SIGNAL PATH	
	Connectors	
J1-J3	22-pin connector	600058-605-002
J4A, J4B	12-pin connector	600058-605-001
J5-J7	Same as J1	
J8	Jack, submin assembly	600102-540-005
J9, J10	Jack, submin assembly	600102-540-002
J11, J12	Jack, submin assembly	600102-540-002
	Capacitors	
C20, C21	270 pf, 100V, ±5%	600215-314-029
C22, C23	0.1 µf, 25V, +80, -20	600215-314-016
C25-C44	0.001 µf, feed-thru	600219-314-001
C61-C65	0.1 µf, 25V	600189-314-016
C66	0.2 µf, 25V	600160-314-005
C67	47 µf, 15V	647055-319-200
C68	0.01 µf, 100V	600189-314-015
C80	100 pf	600189-314-021
	Resistors	
R29	10Ω, 5W, ±5%	600062-340-025
	Terminal Strips	
TB1	5-pin terminal strip	600160-631-003
	SYNTHESIZER	
	Connectors	
J13-J21	Same as J1	
J22, J23	Jack, submin assembly	600102-540-004
J24	Jack, submin assembly	600102-540-001
J25	24-pin connector	600056-605-003

CHASSIS ASSEMBLY: REPLACEABLE PARTS (Cont)

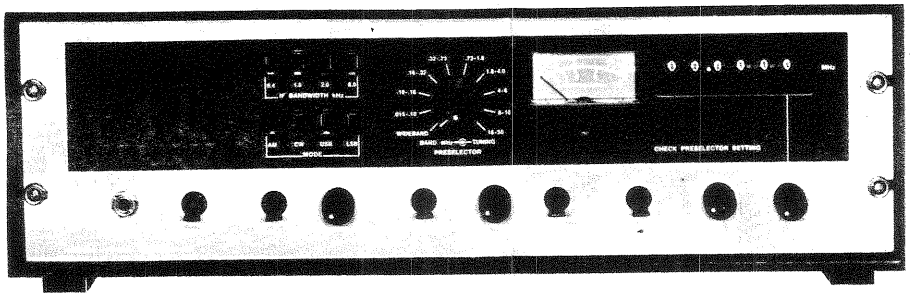
Item	Description	Part Number
	Capacitors	
C45	6.8 μf, 6V	668045-319-609
C46	0.01 μf, 100V	600189-314-015
C47	0.10 μf, 100V	600189-314-017
C48, C49	0.2 μf, 25V	600160-314-005
C50	0.1 μf, 25V	600189-314-016
C51, C52	Same as C46	
C53	Same as C48	
C54	6.8 μf, 6V	668045-319-609
C55-C59	0.001 μf, feed-thru	600219-314-001
C60	56 μf, 15V	656055-319-150
C70	Same as C46	
C71	24 pf	600215-314-012
C72-C76	100 pf	600215-314-021
C77, C78	Same as C47	
C79	Same as C46	
C82	Same as C72	
	Chokes	
L1	RF, 4.7 μH	600119-376-009
L2	RF, 1.0 μH	600119-376-001
L3	RF, 12.0 μH	600119-376-014
L4-L6	RF, 1.2 μH	600119-376-002
L7, L8	Same as L1	
L9	Same as L2	
L10	Same as L1	
L11	RF, 3.3 μH	600119-376-007
L14, L15	Same as L2	
	Resistors	
R30	250Ω, 5W, ±5%	600062-340-025
R35	120Ω, 1/4W, ±5%	612004-341-075
	Terminal Strips	
TB2	4-pin	600160-631-001
TB3	5-pin	600160-631-003

CHASSIS ASSEMBLY: REPLACEABLE PARTS (Cont)

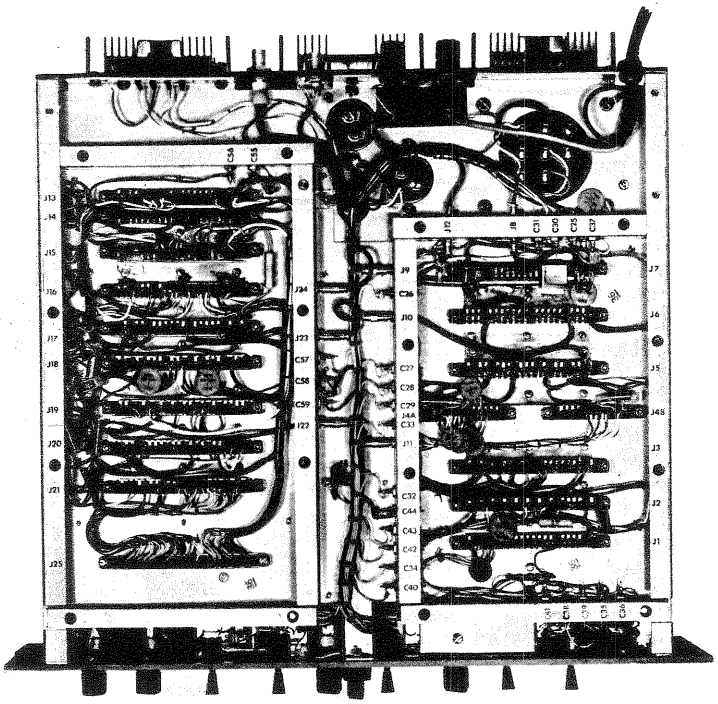
Item	Description	Part Number
TB4	5-pin	600160-631-002
TB5	Same as TB4	
TB6, TB7	Same as TB2	
TB8	2-pin	600160-631-004



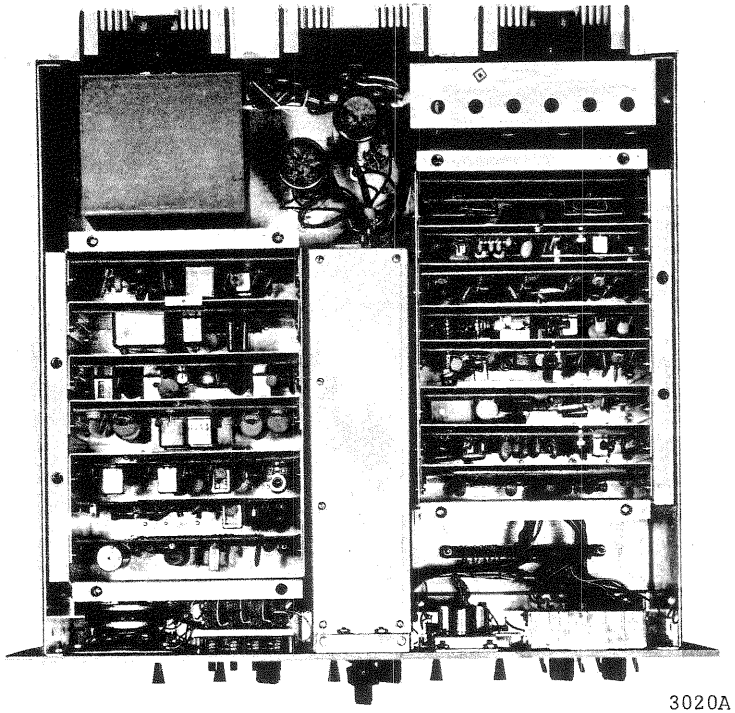
Rear Panel



Front Panel



Bottom View



Top View

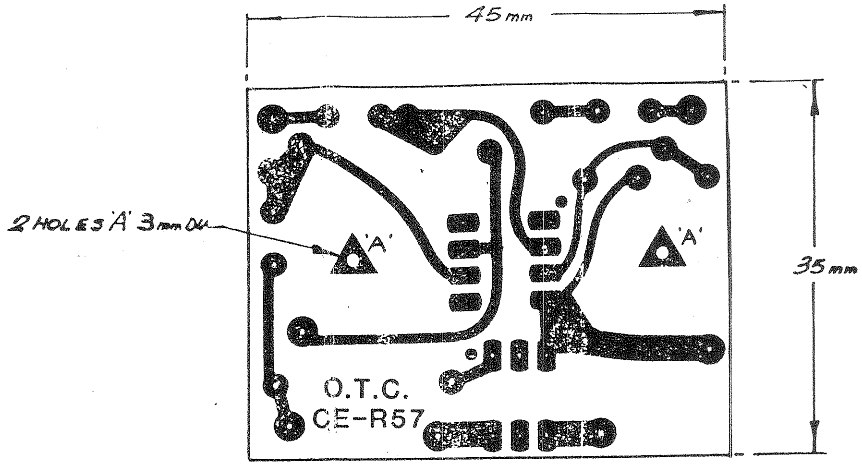
3020A Receiver Assembly.

RECORD OF FIELD MODIFICATIONS

Equipment Type			Serial No.
Service Bulletin Number	Made By	Date	Remarks

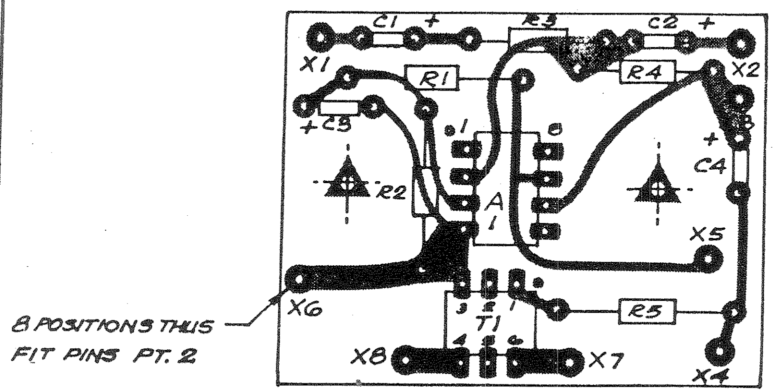
PARTS LIST

CIRCUIT REF.	PART	DESCRIPTION	QTY.	REMARKS
		CIRCUIT DIAGRAM THIS DWG.		
		ASSEMBLY " "		
	1	BOARD " "	1	
X1 - X8	2	PINS 'PRESTINCERT' L1598 BELLING + LEE	8	
A1	3	INTEGRATED CIRCUIT OP. AMP. AD741	1	8PIN D.I.L.
R1, 2	4	RESISTOR 100K 1/4 - 1/2W	2	
R3	5	" 4.7K "	1	
R4	6	" 390K "	1	
R5	7	" 560Ω "	1	
C1, 2 & 3	8	CAPACITOR 10μF 35V SOLID TANTALUM	3	'SOANAR' TAD
C4	9	" 100μF 35V " "	1	" "
T1	10	TRANSFORMER, LINE AUDIO, TYPE MG21	1	'SOANAR'
	11	I.C. SOCKET 8 PIN D.I.L.	1	
	12	I.C. SOCKET 6 " "	1	
	13	MOUNTING DETAILS. THIS DRG. SHEET 3	1	

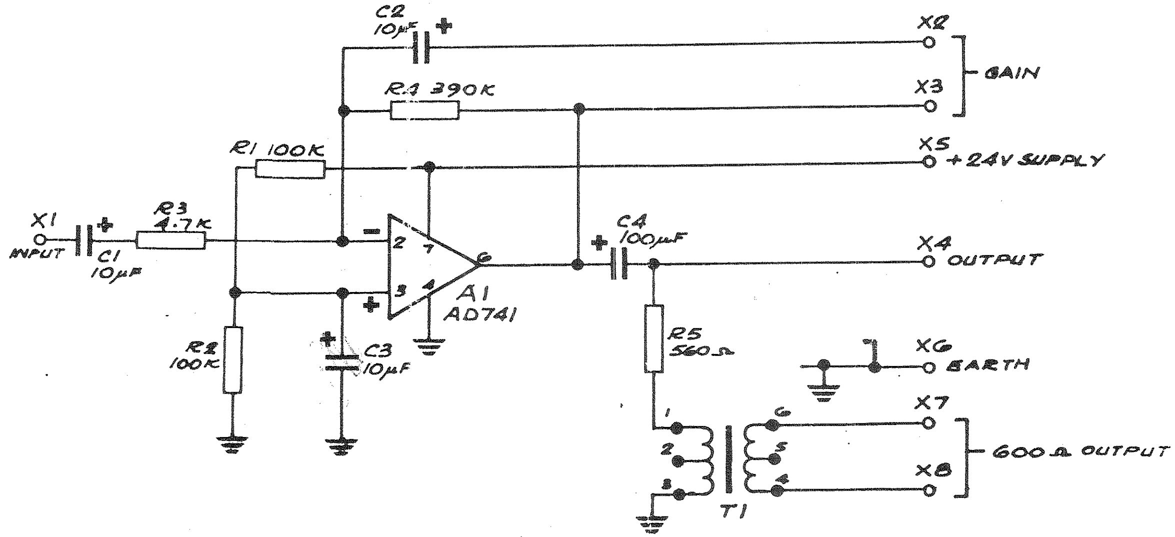


DETAILS
PRINTED BOARD (SOLDERING SIDE) - SCALE 2/1

MATERIAL:- 1.6mm THICK EPOXY BONDED FIBRE GLASS SHEET, 610 g/M² COPPER CLAD ONE SIDE ONLY.
FINISH:- CLEAN, ETCH, & TIN PLATE PATTERN.
NOTES:- 1. USE IN CONJUNCTION WITH SHT. 2 THIS DWG. (P.C. BOARD MASTER)
2. HOLES NOT DESIGNATED DRILL 1mm DIA.



BOARD ASSEMBLY - SCALE 2/1 -



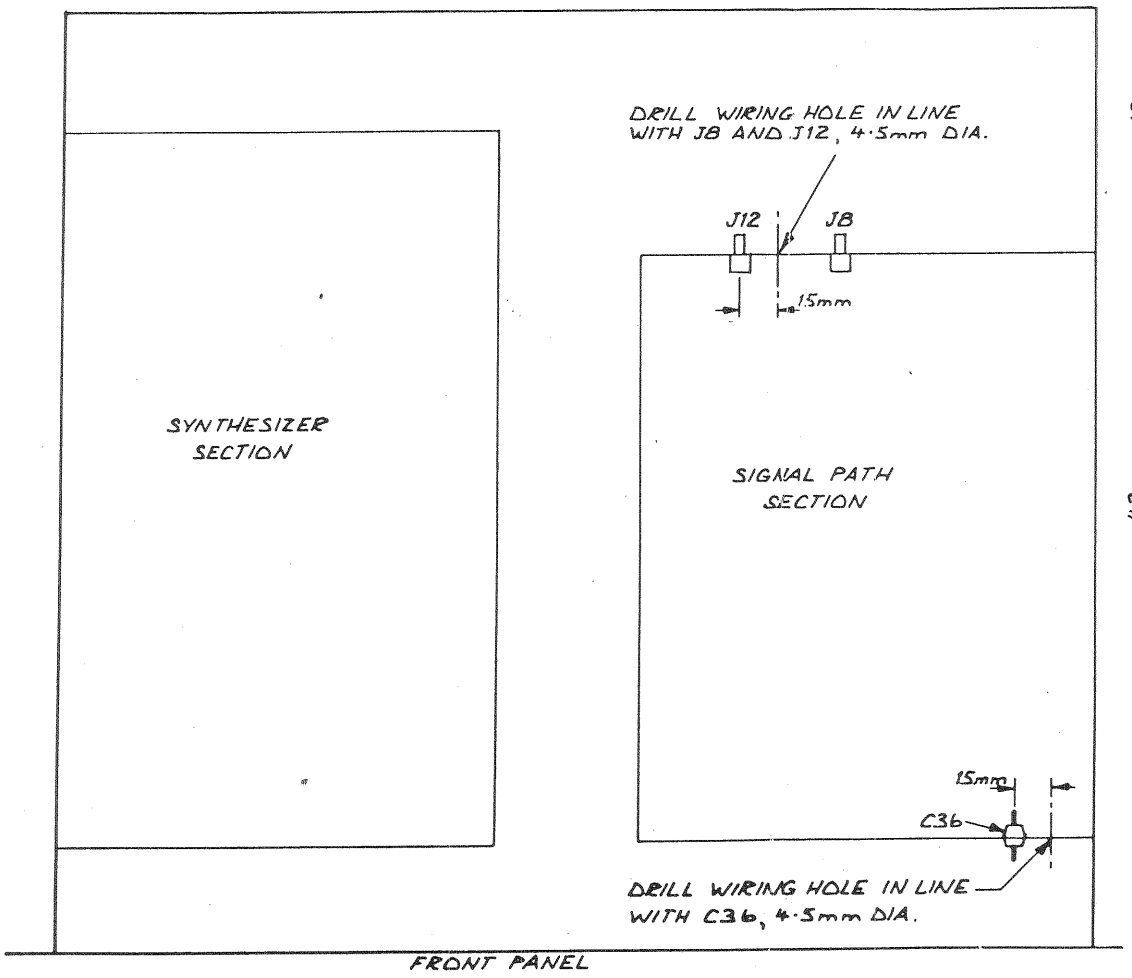
CIRCUIT DIAGRAM

OVERSEAS TELECOMMUNICATIONS COMMISSION (AUSTRALIA)	DRAWING NO.
MACKAY MARINE RECEIVERS 600 OHMS AUDIO LINE AMP. BOARD CIRCUIT, DETAILS & ASSEMBLY	CE-R57 SHEET 1 CONT'D.

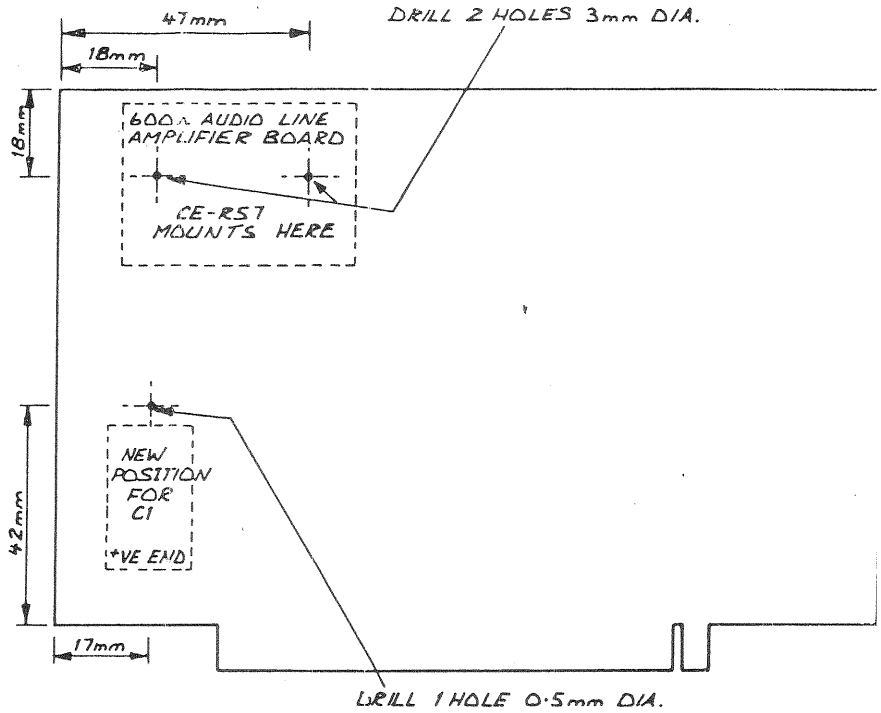
ISSUE	D.A.	CHANGES			DRN	CKD	APPD & DATE
1	11/6/86	ORIGINAL ISSUE	DRAFTING		D.W. 5/85	N.N.	K.R. 21-5-82

ISSUE	D.A.	CHANGES	DRN	CKD	APPD & DATE

ISSUE	D.A.	CHANGES	DRN	CKD	APPD & DATE
1	11353	ORIGINAL ISSUE DRAFTING	BJS	U.H.	A.D. 6.9.83



NOTE:- I.T.T. MACKAY MARINE RECEIVER 3020A - UNDERSIDE VIEW WITH COVERS REMOVED SHOWING DETAILS OF HOLE DRILLING IN CHASSIS.



I.T.T. MACKAY MARINE RECEIVER 3020A AUDIO AMPLIFIER BOARD - DETAILS FOR MOUNTING 600Ω AUDIO LINE AMPLIFIER BOARD AND RELOCATION CAPACITOR (C1).

PART 13 NOT TO SCALE

OVERSEAS TELECOMMUNICATIONS COMMISSION (AUSTRALIA)	DRAWING NO.
MACKAY MARINE RECEIVERS 600Ω AUDIO LINE AMPLIFIER BOARD MODIFICATIONS TO MACKAY MARINE RECEIVER 3020A FOR MOUNTING.	CE-R57 SHEET 3.