PTR2311

SYSTEM 4000

TECHNICAL MANUAL

FOR

TUNER, HF VEHICLE ANTENNA

PV 4330

TECHNICAL DESCRIPTION

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TUNER, HF, VEHICLE ANTENNA (HF ATU)

TECHNICAL DESCRIPTION

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INTRODUCTION

GENERAL

1. The Tuner, HF, Vehicle Antenna (HF ATU) shown at Figure 1, is a Microprocessor-controlled Antenna Tuning Unit for use in ground or vehicle-borne HF transceiver stations.

2. The HF ATU may be connected into the HF sub-system as follows:

   a. Between the vehicle antenna and the Amplifier, Radio Frequency, HF, 100W (HF PA).

   b. Between the vehicle antenna and the Filter, Bandpass, HF Cositing (CSF), if the HF PA is not fitted.

   c. Directly between the Receiver Transmitter, HF, (HF R/T) and the vehicle antenna if neither the HF PA nor HF CSF is fitted.

3. Operation of the HF ATU is fully automatic over its operating range of 2 to 30 MHz. The RF input power to the HF ATU is automatically reduced if the vehicle power supplies go low, and also if the HF ATU overheats or an unacceptable antenna mismatch occurs. The HF ATU operates from an unconditioned nominal 28 Vdc vehicle supply which is provide either directly by the HF R/T or, depending upon configuration, via the HF CSF or the HF PA.

4. The HF ATU is of modular construction and consists of six panel electronic circuits plus a number of chassis-mounted components. Provision for vehicle mounting is made via threaded holes located on flanges at the side of the HF ATU.

FIGURE 1 - TUNER, HF, VEHICLE ANTENNA

ARRANGEMENT OF EQUIPMENT

LAYOUT OF CONTROLS AND CONNECTORS

5. The layout of the HF ATU front panel is shown at Figure 2. Table 1 lists the functions of all connectors and charts. There are no manual controls.

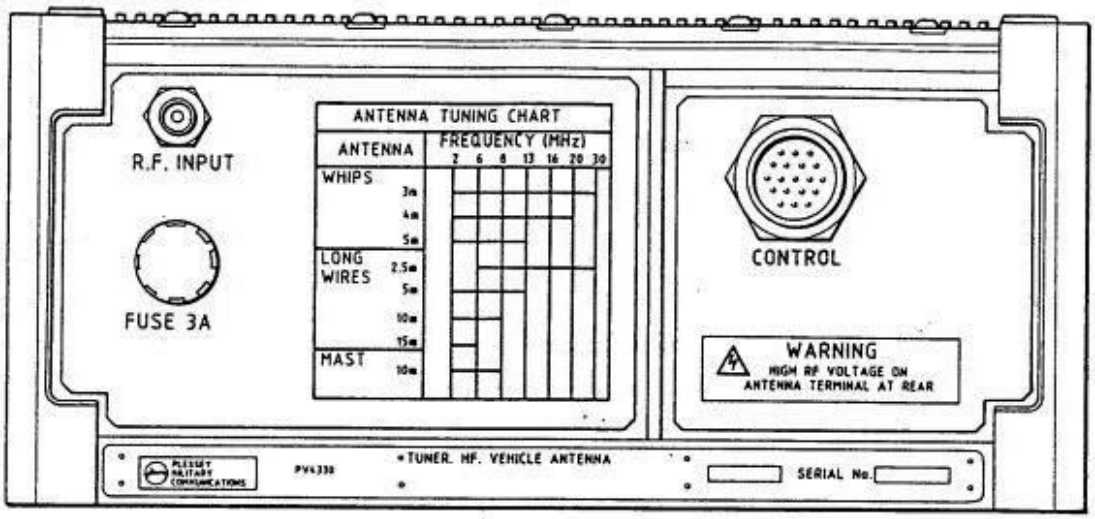

FIGURE 2 - HF ATU FRONT PANEL

TABLE 1 - FUNCTION OF CONNECTORS AND CHART

CONNECTOR OR CHART	FUNCTION
R.F. INPUT	RF input power from HF R/T, HF CSF or HF PA.
CONTROL	Power and control lines to/from HF R/T, HF CSF or HF PA.
ANTENNA TUNING CHART	Combinations of antennae and operating frequencies.
Screw terminal (at rear)	RF output to antenna.

LAYOUT OF EQUIPMENT

6. The HF ATU is constructed as a single four-side aluminium casting with a ribbed bulkhead, and has detachable top and bottom covers with panclimatic seals. The electrical components are mounted on threaded bosses and the equipment is kept dry internally by a desiccator capsule which is mounted on the rear panel.

7. The case contains six panel electronic circuits/assemblies, five being mounted in the upper and lower compartments, and one mounted on the chassis. Five power transistors in the lower compartment are mounted on the chassis via thermally transparent insulating washers.

8. The front of the casting is fitted with the R.F. INPUT and CONTROL connectors and a fuse; the rear of the casting carries the antenna connector with associated insulator, the desiccator, and an earth stud. All front panel designations are clearly marked on a blackened aluminium plate. Internal connections of removable items are made via plug/socket type connectors.

9. Two threaded holes (ISO Metric Coarse) on the flanges of the upper and lower surfaces of the case are available for attaching the HF PA to other HF equipments. All tapped holes are fitted with wire thread inserts.

PRINCIPLES OF OPERATION

GENERAL

10. As shown in the equipment block diagram at Figure 3, the HF ATU comprises the following modules:

a. Module 1 - Multiway Filter Board.

b. Module 2 - Power Supply Unit.

c. Module 3 - Microprocessor Board.

d. Module 4 - Detector Module.

e. Module 5 - RF Matching Board.

f. Module 6 - RF Matching Board.

Module 1 - Multiway Filter Board

11. Module 1 provides an LC filter and EMP (Electromagnetic Pulse) protection for each of the system control lines (except EARTH) used by the HF ATU.

Module 2 - Power Supply Unit

12. Module 2 provides regulated dc power supplies for Modules 3, 4, 5 and 6 from the unconditioned 28 V vehicle supply. System control signals are routed to/from Module 2 via Module 1.

Module 3 - Microprocessor Board

13. Module 3 contains the Microprocessor, control logic and buffering circuits which decode the various control signals from other equipments and determine the overall operation of the HF R/T. External system controls are fed to/from Module 3 via the equipment's front panel CONTROL connector and Module 1. Control signals to/from Module 3 control the operation of the tuning components on Modules 4, 5 and 6.

14. Module 3 is also responsible for distributing regulated dc voltage supplies from Module 2 to Modules 4, 5 and 6.

Module 4 - Detector Module

15. Module 4 contains detectors which are required by the Microprocessor on Module 3 during the HF ATU's tuning sequence. Module 4 also contains the fine tuning inductors and capacitors, plus their individual selection relays which are controlled by the Microprocessor on Module 3.

Module 5 - RF Matching Board

16. Module 5 contains the medium tuning inductances and the coarse tuning capacitors plus their individual selection relays. The relays are controlled by the Microprocessor on Module 3.

Module 6 - RF Matching Board

17. Module 6 contains the coarse tuning inductances and broad band capacitors plus their individual selection relays. The relays are controlled by the Microprocessor on Module 3. The RF power output to the antenna (via the rear panel) is also taken from this module.

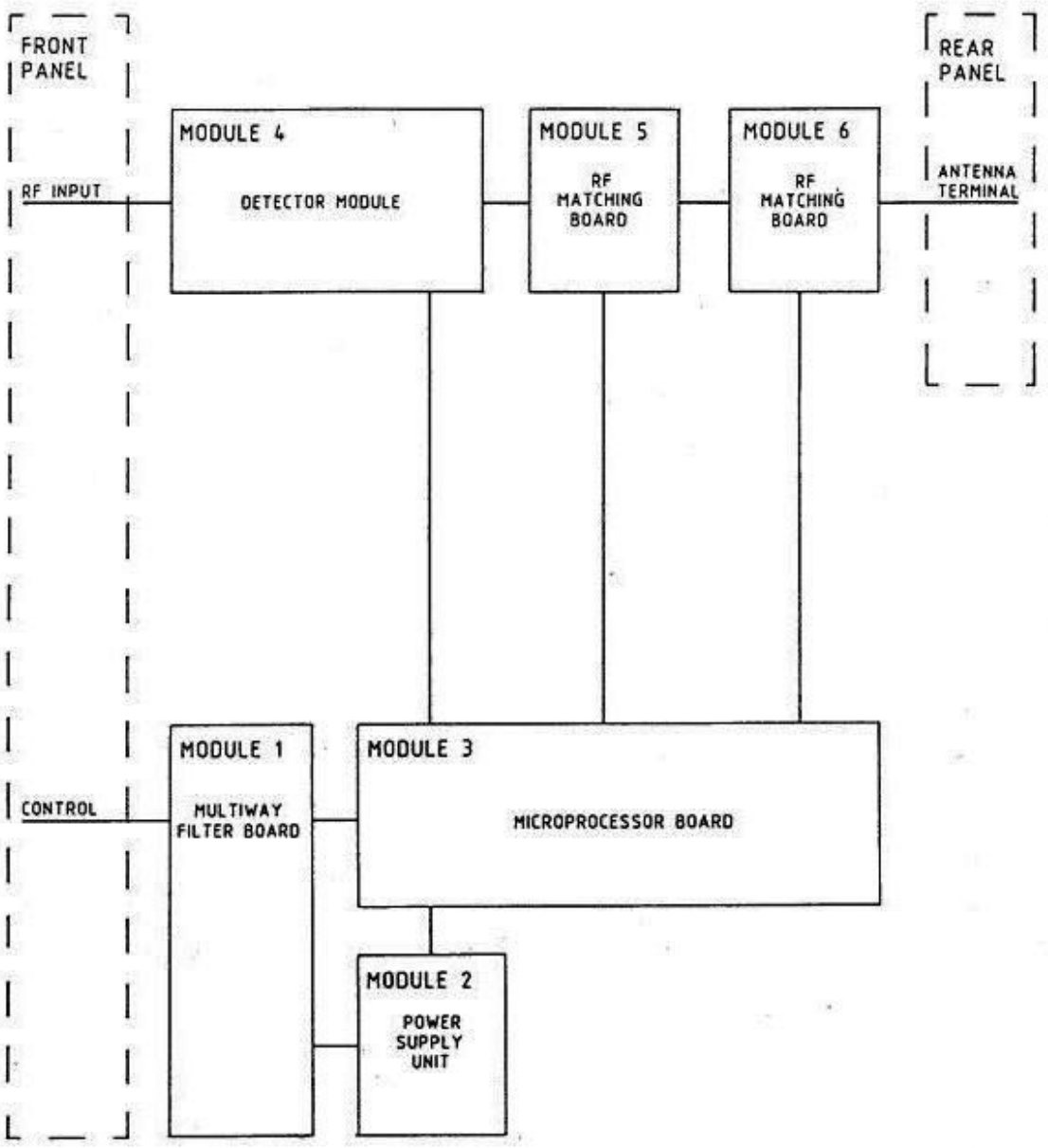

FIGURE 3 - HF ATU EQUIPMENT BLOCK DIAGRAM

FUNCTIONAL DESCRIPTION

18. The HF ATU's tuning sequence (tuning takes approximately 1.5 seconds) and subsequent quiescent operation are determined by the system control signals applied to the front panel CONTROL connector. A functional block diagram of the HF ATU is shown in Figure 4. The major functional elements within the equipment are as follows:

a. The detectors which monitor the transmission line.

b. The Network Tuning Inductors and Capacitors which are selected by the microprocessor to match the nominal 50 Ohm output impedance of the HF R/T, the HF PA or the HF CSF, to the impedance of the antenna.

c. The Microprocessor Control Circuits which control all aspects of the HF ATU operation.

19. The operation of relay 4RLA determines whether the RF Input is routed to the Network Tuning Inductors and Capacitors, or to the detector circuits. When the equipment is correctly tuned, 4RLA is energised and the transmit/receive path is through the VSWR Detector, 4RLA, the Network Tuning Inductors and Capacitors, to the antenna. With reference to Figure 4, 4RLA is shown in the de-energised state to connect the RF input to the detector circuits via 4RLB. Relay 4RLB, also shown in the de-energised state in Figure 4, determines whether the RF is applied to the Power Detector or the Phase and Conductance Detector. Both relays are controlled by the Microprocessor Control Circuits. 4RLA and 4RLB denote that relays RLA and RLB are housed on Module 4.

Tuning Sequence

20. When the HF R/T is initially switched on, or when its operating frequency changes, the HF R/T issues a RESET signal which causes all external units in the output path to prepare for new parameters. On receipt of a RESET signal from the HF R/T, the Microprocessor Control Circuits switch all previously selected tuning components out of circuit (shown as Bypass on Figure 4). With 4RLA energised, this effectively shorts the RF INPUT connector to the antenna. The Microprocessor then sets the system FAULT and READY lines low. READY, connected to the HF R/T via the CONTROL connector, will remain low until the tuning sequence is successfully completed.

21. When the next pressel operation sets the HF R/T to transmit, it informs the HF ATU by setting the Tx/Rx control line low. The RF Output from the HF R/T is an unmodulated 5 Watt tuning signal at the HF R/T's transmit frequency. On receipt of the Tx/Rx signal, the Microprocessor Control Circuits de-energise 4RLA (from its energised HF ATU 'tuned' position) and 4RLB is energised. This connects the RF tuning signal to the 50 Ohm Load and the Power Detector. The 50 Ohm Load is used to terminate the RF TUNE signal.

22. The output of the Power Detector is applied to the Microprocessor Control Circuits as a dc voltage proportional to the amplitude of the RF TUNE signal. With 4RLA de-energised, the antenna circuit is connected to the Antenna DC Resistance Detector via the Bypass Route in the Network Tuning Inductors and Capacitors.

23. If the CW tuning signal is not between 1 and 7 W, or the antenna dc resistance is less than 75 Ohms, the tuning sequence is aborted. When this occurs, the Microprocessor Control Circuits set FAULT high to signal the fault condition to the HF R/T.

24. If the tuning signal power and antenna dc resistance are within limits, the CW carrier frequency is measured and the resultant value used by the Microprocessor Control Circuits to latch in the initial tuning components. 4RLB is de-energised by the Microprocessor Control Circuits, and the combined impedance of the tuning circuit and the antenna is measured by the Phase and Conductance Detectors. The initial tuning circuit is then amended as required by adding/deleting tuning components. This iterative process of measurement and amendment is repeated until an impedance value of approximately 50 Ohms (20 milli-Siemens conductance) is achieved with the reactance component of the impedance tending towards zero.

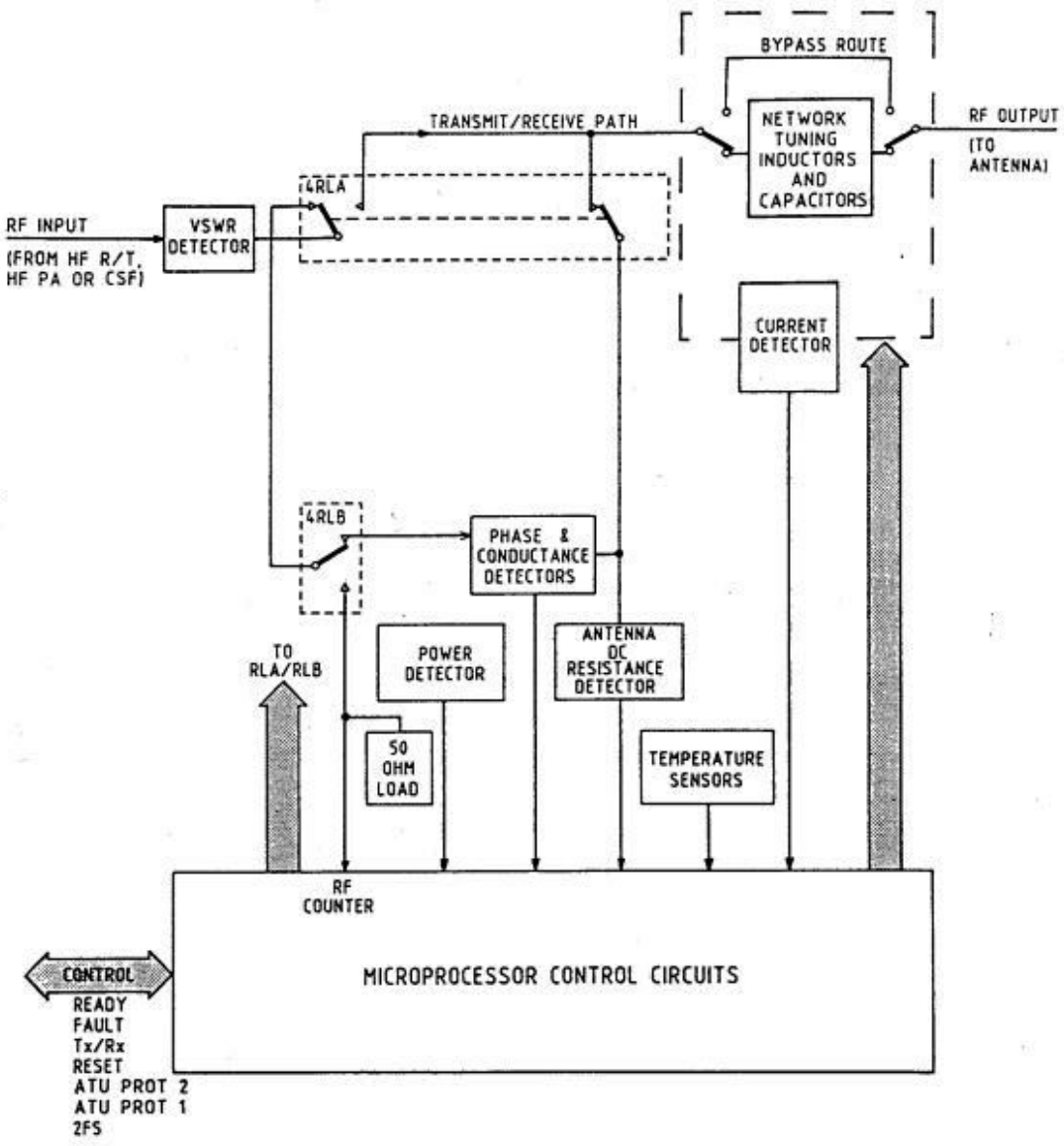

FIGURE 4 - HF ATU FUNCTIONAL BLOCK DIAGRAM

25. The Microprocessor Control Circuits then measure the VSWR from the VSWR Detector to determine if the tuning process has been successful. If a forward to reverse voltage standing wave ratio of 3:1 (or better) is found, the equipment is correctly tuned. A ratio greater than 3:1 indicates the equipment is not correctly tuned; in this case, the Microprocessor Control Circuits set the FAULT line active high to inform the HF R/T that HF ATU tuning has failed.

26. When the tuning sequence is successfully completed, the HF ATU informs the HF R/T by setting the READY line active high. 4RLA is then energised by the Microprocessor Control Circuits to connect the RF input through the matched tuned circuit to the antenna.

2FS

27. In the 2FS mode of operation, the HF R/T receives on one frequency and transmits on another. To conform to this requirement, the transmit and receive signal paths through the HF ATU are different. The transmit path follows the normal operating path through the tuned inductors and capacitors, but on receive all the tuning components are switched out of circuit and the data regarding the component configuration put into memory.

28. Because the tuning inductors are 'switched out' by short circuiting, the receive path is a direct connection between the antenna and the RF INPUT connector. When switching from receive to transmit, the tuned circuit component data is retrieved from memory and the components switched back in.

Protection Circuits

29. The Microprocessor Control Circuits generate ATU PROT 1 and ATU PROT 2 system control signals to instigate a reduction in the RF input power to the HF ATU. A combination of ATU PROT 1 and ATU PROT 2 logic levels instigating different reductions in input power under the following conditions:

a. When excessive currents flowing in the network tuning components are detected by the Current Detector.

b. When excessive temperatures are detected by the Temperature Sensors on the HF ATU chassis.

c. Poor VSWR (the VSWR Detector is always in circuit when the HF R/T is transmitting).

d. When a low supply voltage is identified by the Microprocessor Control Circuits.

MICROPROCESSOR PROGRAM CONTROL

30. The operation of the HF ATU is controlled and monitored by Microprocessor software stored on Module 3. As shown in Figure 5, the Microprocessor system comprises a Microprocessor, a Non-Volatile Memory and a number of Input/Output Ports.

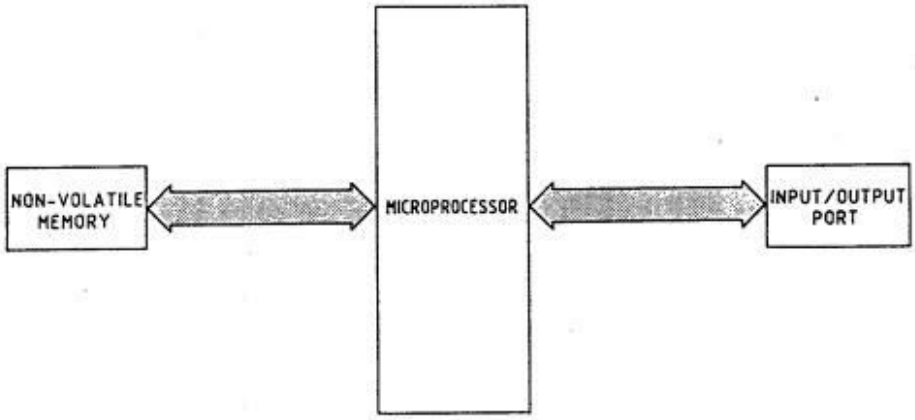

FIGURE 5 - MICROPROCESSOR SYSTEM BASIC BLOCK DIAGRAM

31. The term Non-Volatile Memory means the contents of the memory will not be lost when power to the system is removed. This type of memory is used to provide permanent storage for the sequence of instructions and data that constitute the Microprocessor's program. The HF ATU uses an Erasable Programmable Read Only Memory (EPROM) as the Non-Volatile Memory device, in which the program data is made 'permanent' by applying an overvoltage (about 25 V) to its control gate. Once this gate has been charged, the only method of erasing the data is by exposure to ultraviolet light.

32. The Microprocessor is a single integrated circuit which executes the program instructions and reacts to events from external devices. Various registers in the Microprocessor have specific roles and carry out the following actions:

a. Hold instructions currently under execution.

b. Perform logic and arithmetical functions.

c. Hold input and output data, addresses and status information.

33. Small amounts of volatile Random Access Memory (RAM) are used to hold transient results produced during processing, such as intermediate results produced from arithmetic operations.

34. The Input/Output Ports enable the Microprocessor to communicate with external units. A detailed description of the ports is given in the detailed description of Module 3.

35. When the Microprocessor is switched on, the start point of the program in memory is addressed by the Microprocessor to fetch its first instruction. The Microprocessor then executes each sequential element of the program, using each instruction to process the program's requirements. Instructions and data in the HF ATU's Microprocessor system are made up of combinations of '1's and '0's to form a byte (8 bits). In physical terms, the program, with instructions of one, two or three bytes, appears as shown in Figure 6; the ones and zeros contain the information which instructs the Microprocessor on what action to take next.

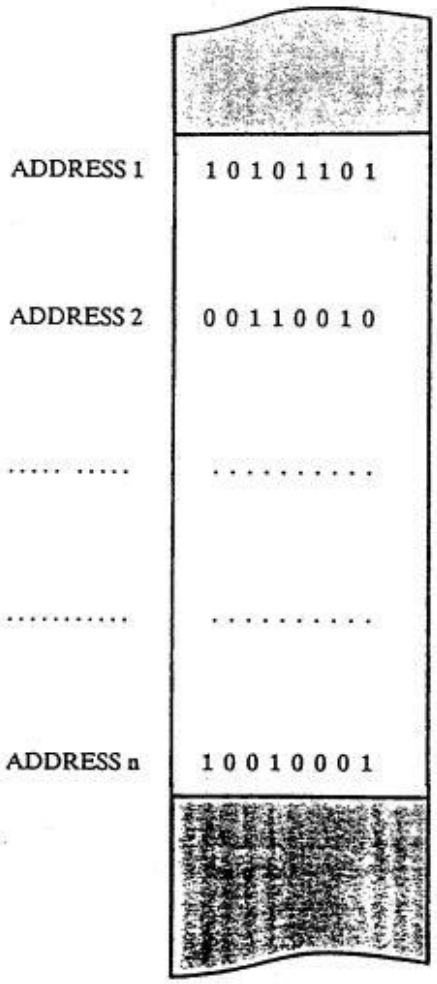

FIGURE 6 - MICROPROCESSOR MEMORY STRUCTURE

36. The Microprocessor communicates with its memory and input/output devices using an address bus, a bi-directional data bus and a control bus. The address bus is used by the Microprocessor to select a specific memory location in a memory device. The data bus enables data to be transferred to and from the Microprocessor and may act as input or output, but not at the same time. The control bus consists of several data lines which synchronise and co-ordinate the Microprocessor's actions.

DETAILED TECHNICAL DESCRIPTION

GENERAL

37. This detailed technical description is organised as a general description of how the HF ATU operates, followed by a detailed circuit description of each module. Figure 1001 supports this general description by identifying both the functional circuits within each module and the main connections made between modules. To avoid too much information on one diagram, the power supplies are dealt with separately.

38. The HF ATU determines its operating condition at any time by examining its inputs (see Table 2).

TABLE 2 - HF ATU FRONT PANEL CONTROL INPUTS

INPUT	CONNECTOR	DEFINITION
RESET	1PL1-G	Flag input 1-0-1 pulse from HF R/T, indicating either HF R/T switch-on, a frequency change, a change of antenna or the transition from Tx to Rx in 2FS mode.
Tx/Rx	1PL1-F	'0' or '1' flag from HF R/T indicating the HF R/T transmit/receive status; '1' for receive, '0' for transmit.
SYSTEM ON	1PL1-L	'1' flag from HF R/T indicating it is fitted and powered up.
2FS	1PL1- M	'0' or '1' flag from HF R/T indicating the HF R/T mode of operation; '0' for 2FS, '1' for normal. 2FS is set to '0' after the first pressel operation after selecting 2FS mode.

39. The output signals from the HF ATU to the HF R/T and HF PA (when fitted) are shown in Table 3.

TABLE 3 - HF ATU FRONT PANEL CONTROL OUTPUTS

INPUT	CONNECTOR	DEFINITION
READY	1PL1-A	'0' or '1' level flag from HF ATU; used with FAULT to determine status. '0' indicates HF ATU tuning or fault if FAULT is '1'; '1' indicates HF ATU is ready.
FAULT	1PL1-B	'0' or '1' level flag from HF ATU; used with READY to determine status . '1' indicates a fault; '0' indicates no fault.
ATU PRESENT	1PL1-D	'1' flag indicates that an HF ATU is fitted and switched on.
ATU PROT 1	1PL1-S	'0' or '1' level flag used with ATU PROT 2 to turn down the power output of the HF PA.
ATU PROT 2	1PL1-J	'0' or '1' level flag used with ATU PROT 1 to turn down the power output of the HF PA.

Note: throughout the circuit descriptions, the logic signal levels are defined as follows:

Logic High ('1') - the voltage level is more positive than 0 Volts and is equivalent to a logic 1.

Logic Low ('0') - the voltage level is at 0 Volts and is equivalent to a logic 0.

Active High - when the logic level is at logic 1, the circuit function that the level is controlling is enabled.

Active Low - when the logic level is at logic 0, the circuit function that the level is controlling is enabled.

40. With reference to Figure 1001, the operation of the HF ATU can be sub-divided into the following:

a. RESET from the HF R/T.

b. Transmit Following RESET.

c. RF Power and Antenna Resistance Measurement.

d. Initial Component Selection.

e. Tuning Sequence.

f. Turndown Protection Circuits.

g. 2FS.

h. Power Supplies.

i. BITE.

RESET from HF R/T

41. When the HF R/T and the HF ATU are initially switched on, or when the HF R/T changes frequency, a RESET pulse is sent from the HF R/T to all its associated equipments.

Note: RESET also occurs at each Tx/Rx transition during 2FS mode.

42. With reference to Figure 1001, the RESET pulse is applied to the HF ATU at PL1-G. From there it is fed to the Clock Oscillator Circuits and the Microprocessor's Input Port 1 on Module 3 via 1PL1-G, 1PL2-5 and 3PL2-4. The RESET signal starts the Microprocessor's clock, and is then latched from Input Port 1 onto the Data Bus and the program stored in EPROM is executed.

43. The HF ATU program begins by the microprocessor sending control logic signals, via the Data Bus and the Output Ports and Driver Circuits, to switch all the tuning components on Modules 4, 5 and 6 out of circuit. This effectively connects the RF input and antenna output.

44. If 2FS is high ('1') at 3PL2-6, normal mode is identified and the microprocessor outputs a '0' on the READY and FAULT lines. This indicates to the HF R/T that the HF ATU is now waiting for an unmodulated 5 W tuning signal from which to select its initial tuning components. READY is output from the Microprocessor's Output Port 1 via 3PL2-1, 1PL2-10, 1PL1-A and PL1-A; FAULT is output from the Microprocessor's Output Port 1 via 3PL2-2, 1PL2-11, 1PL1-B and PL1-B. The Clock Oscillator Circuit is then stopped by a programmed output from Output Port 1.

45. If 2FS is low ('0') at 3PL2-6, signifying 2FS mode, the HF ATU software prepares to switch the tuned components in and out of circuit during the HF R/T transmission and reception cycles. In receive mode, the Microprocessor (via the Output Ports and Driver Circuits) sends the appropriate control signals to the relays on Modules 4, 5 and 6 to select the Bypass Route. The Microprocessor then switches the clock off by a program output from Output Port 1. When the Tx/Rx line changes to a '0' (transmit mode), the clock is re-started and the Microprocessor re-issues the appropriate tuning component data to the selection relays on Modules 4, 5 and 6.

Transmit Following RESET

46. On the next pressel operation following a RESET, Tx/Rx goes to '0' (transmit mode). On receipt of the Tx/Rx signal at 3PL2-3 (via PL1-F, 1PL1-F and 1PL2-3), the Clock Oscillator Circuit is started again and the Tx/Rx signal latched onto the Data Bus via the Input Port 1. The RF input at SK1 is now an unmodulated 5 W tune signal at the HF R/T's operating frequency.

47. The Microprocessor processes the transmit following RESET by setting DET RELAY high to remove the 0 V (via the Output Ports and Driver Circuits, 3PL5-16 and 4PL2-11) from detector relay 4RLA (Module 4). This causes 4RLA to de-energise and switch the RF input from the transmit/receive path to the detectors. At the same time, the 50 OHMS RELAY line is set low to energise 4RLB (via the Output Ports and Driver Circuits, 3PL5-13 and 4PL2-14) to disconnect the RF from the Phase and Conductance Detectors, and route it to the Power Detector and the RF Counter via 4PL2-25.

48. Finally, the Microprocessor, via Output Port 1, applies a 0 V PSU CONTROL signal to the power supply unit on Module 2 (via 3PL1-3 and 2PL6-6) to enable the +5 V (SWD) and +10 V (SWD) regulators. These regulated outputs are used on Modules 3 and 4 during the HF ATU's tuning sequence.

RF Power and Antenna DC Resistance Measurement

49. If the RF input power to the HF ATU is not between 1 and 7 W, or the antenna dc resistance is less than 75 Ohms, a '1' is output on 4PL2-7 WINDOW and routed (via 3PL5-20) to the Control Flag Selection Multiplexer on Module 3. The output of the multiplexer is routed directly to the Microprocessor under program control.

50. If a fault condition exists ('1' on 4PL2-7), the Microprocessor outputs a signal to the Output Ports and Driver Circuits which results in a '0' at 3PL5-16 and 4PL2-11. This '0' energises detector relay 4RLA which disconnects the RF tune signal from the detectors. To signal the fault condition to the HF R/T, the Microprocessor sets FAULT high (via Output Port 1, 3PL2-2, 1PL2-11, 1PL1-B and PL1-B) and READY low (via Output Port 1, 3PL2-1, 1PL2-10 and 1PL1-A). This combination of '1' and '0' informs the HF R/T of a fault condition and the HF ATU aborts its tuning sequence.

51. If the RF power and antenna dc resistance checks are satisfactory, the HF ATU software proceeds to the initial component selection procedure.

Initial Component Selection

52. An RF output is taken from the Power Detector circuit on Module 4 and fed, via 4PL2-25 RF COUNTER and 3PL5-2, to the RF counter on Module 3. The RF Counter produces a data output representing the RF tune signal's frequency which is applied to the Microprocessor via Input Port 2.

53. After evaluating the frequency of the RF carrier, the software (via the Output Ports and Driver Circuits) inserts components from the following groups into the RF circuit path:

a. Series inductors on Modules 4, 5 and 6 which are not self-resonant at the RF carrier frequency.

b. The line shortening capacitors (LSC) on Module 5.

c. The broad-banding capacitors (BBC) on Module 6.

54. The initial selection of components is determined by the RF carrier frequency, and is listed in Table 4.

TABLE 4 - INITIAL COMPONENT SELECTION

FREQUENCY RANGE (MHZ)	SERIES INDUCTORS	LSC	BBC
1.5 - 2.9	L1 - L13	-	BBC1 and 2
3.0 - 3.4	L2 - L13	-	BBC1 and 2
3.5 - 4.5	L3 - L13	-	BBC1 and 2
4.6 - 6.7	L4 - L13	-	BBC1 and 2
6.8 - 8.1	L5 - L13	-	BBC1 and 2
8.2 - 11.1	L5 - L13	LSC1	BBC1 and 2
11.2 - 13.9	L6 - L13	LSC1	BBC1 and 2
14.0 - 15.5	L6 - L13	LSC1	BBC1
15.6 - 17.0	L6 - L13	LSC1 and 2	BBC1
18.0 - 23.6	L7 - L13	LSC1 and 2	BBC1
23.7 - 24.0	L7 - L13	LSC1	BBC1
25.0 - 27.5	L8 - L13	LSC1	BBC1
27.6 - 28.0	L8 - L13	-	BBC1
29.0 - 30.0	L10 - L13	-	BBC1

55. After the initial selection, further component changes may be required to achieve optimum matching.

Tuning Sequence

56. The Tuning Sequence uses the Phase and Conductance Detectors on Module 4 to monitor the resistive, capacitive and inductive components of the impedance presented by the matching network. Tuning is an iterative process comprising the following actions under software control:

a. Components are added or subtracted to the tuning circuits on Modules 4, 5 and 6.

b. The detector outputs, monitoring the change in impedance, are sent to the Microprocessor for analysis and further action.

c. If further component selections are required, the actions at 56.a are repeated; if the equipment is now correctly tuned, the iteration ends.

57. The Phase Detector on Module 4 is connected to Module 3 via 4PL2-9 PHASE and 3PL5-18. The Conductance Detector on Module 4 is connected to Module 3 via 4PL2-10 CONDUCTANCE and 3PL5-17. The resultant analogue dc voltages on 3PL5-18 and 3PL5-17 are applied to the Analogue to Digital Converter, whose digital output is latched onto the Data Bus under Microprocessor control.

58. The impedance of the matching network (formed by the tuning components) is initially made inductive because the HF ATU cannot tune to a capacitive load. Conversely, at some operating frequencies, the impedance of the matching network may be too inductive to effect a successful tune. Too much inductance is compensated for by inserting line shortening capacitors in series with the inductors.

59. Under program control, the inductive impedance is systematically reduced by switching inductors out of circuit. After each inductor is removed, the output of the Conductance Detector is read by the Microprocessor until the output of the Analogue to Digital Converter is +2.5 V. If this value cannot be achieved, broadband capacitors are inserted and the tuning sequence repeated. The 2.5 V equates to a network resistive component of 50 Ohms (equal to a conductance of 20 milli-Siemens).

60. At this stage in the tuning sequence, the matching network impedance now contains a known resistive component of 50 Ohms and an inductive component. To reduce the impedance to a purely resistive component, shunt capacitors on Modules 4 and 5 are switched into the network as required. After each capacitor is inserted, the output of the Analogue to Digital Converter is read. When the output of the Analogue to Digital Converter is +2.5 V, the inductive and capacitive reactances are equal in magnitude, and being in anti-phase, cancel out. Theoretically, the matching network impedance now contains only a resistive component. In practice, however, it is not possible to remove the reactive components completely, but only reduce them to an acceptable level. Allowance for this is made in the firmware program.

61. On completion of the tuning sequence, the +5 V (SWD) and +10 V (SWD) regulators in Module 2 are switched off by the Microprocessor (via Output Port 1) putting a '1' on 3PL1-3 PSU CONTROL. 4RLA is now energised by a '0' program output (via the Output Ports and Driver Circuits, 3PL5-16 and 4PL2-11) to switch the RF input from the detectors to the transmit/receive path and the tuning circuitry.

62. The output of the VSWR Detector on Module 4 is now monitored by the Microprocessor via the Control Flag Selection Multiplexer on Module 3 (via 4PL2-8 and 3PL5-19). The operation of this circuit is such that a VSWR of 3:1 or better sets the detector output to the multiplexer to a '1'. Under program control, the multiplexer output is read by the Microprocessor, and if the VSWR is better than 3:1, the software considers the HF ATU correctly tuned.

63. To signal a successful completion of its tune sequence, the Microprocessor sets the READY output at PL1-A to a '1' (via Output Port 1, 3PL2-1, 1PL2-10 and 1PL1-A). The combination of a '1' on READY (PL1-A) and a '0' on FAULT (PL1-B) signals a successful tune to the HF R/T.

64. If the VSWR is worse than 3:1, 4PL2-8 becomes a '0' and FAULT is taken to '1' by the Microprocessor. With READY at '0', this combination signals an unsuccessful tune to the HF R/T.

ATU Protection Signals

65. The HF ATU can instigate a reduction in its RF input power (from either the HF PA or HF R/T) by a combination of the ATU PROT 1 and ATU PROT 2 control signals. ATU PROT 1 is supplied by Module 3 on 3PL2-7, and applied to PL1-S via 1PL2-4. ATU PROT 2 is generated from Module 3 on 3PL2-5, and applied to Module 1 on 1PL2-7 for output on PL1-J.

66. The combinational effect of the various logic levels on ATU PROT 1 and ATU PROT 2 is shown in Table 5.

TABLE 5 - EFFECTS OF ENABLING ATU PROT 1 AND ATU PROT 2

ATU PROT 1 (1PL1-S)	ATU PROT 2 (1PL1-J)	EFFECT
'0'	'0'	Normal operation.
'1'	'0'	Instructs the system to reduce the input power from the HF PA to 50 W.
'0'	'1'	The output of the HF R/T is reduced to 1.25 W, although subsequently the power output may be increased by the HF R/T operator. The HF PA is switched to bypass.
'1'	'1'	The HF PA is switched to the bypass state, but signals PA PRESENT from the HF PA to the HR R/T. The HF R/T power output is held at 1.25 W.

67. The ATU PROT signals are generated in the following circumstances:

a. Chassis temperatures exceed 100 deg C.

b. Currents exceeding 7 A exist in the tuned circuits in Module 4.

c. VSWR greater than 3:1.

d. A system supply voltage of less than +19.5 V.

Temperature.

68. If the operating temperature on the HF ATU chassis exceeds 100 deg C, the bi-metallic strips mounted on the chassis open and remove the 0 V from 3PL3-2 on Module 3. This results in the turndown sensing circuit setting ATU PROT 1 on PL1-S to '1' and ATU PROT 2 on PL1-J to '0'. The effect of this combination is detailed in Table 5.

Current.

69. If the circulating currents in the tuned circuits of Module 4 exceed 7 A, a '1' is output on 4PL2-5 from the Current Detector and applied to the turndown sensing circuits via 3PL5-22. If after 2 seconds the input on 3PL5-22 is still a '1', ATU PROT 1 is taken active high ('1') and ATU PROT 2 is held at '0'. If after a further 2 seconds the currents are still high, ATU PROT 2 becomes active high and ATU PROT 1 is taken to '0'. If, after six seconds have elapsed, 3PL5-22 is still '1', ATU PROT 1 and ATU PROT 2 both become '1'. The effect of these combinations is detailed in Table 5.

VSWR.

70. If the VSWR becomes greater than 3:1, the output of the VSWR Detector (Module 4) will put a '0' on 4PL2-8 and 3PL5-19. This has the following effects:

a. Sets ATU PROT 1 to '1' by applying the output from a NAND gate to the turndown sensing circuits. When the VSWR and Tx/Rx inputs to the NAND gate are both '0' (during transmit and a poor VSWR), a '1' is output from the gate, and ATU PROT 1 is set by the protection circuit. ATU PROT 2 is held at '0'. The output of the NAND gate also starts the Microprocessor Clock Oscillator.

b. Sets the VSWR flag on the Control Flag Selection Multiplexer.

71. On receipt of the oscillator clock pulses, the Microprocessor begins to execute the firmware program, and the Control Flag Selection Multiplexer is examined under program control. A '0' on the VSWR flag causes FAULT 3PL2-2 to be set to '1' by the Microprocessor, and with READY 3PL2-1 held at '0', a fault condition is flagged to the HF R/T.

System Supply.

72. If the System Supply to Module 2 at 2PL2-1,2 drops below + 19.5 V, ATU PROT 1 is taken active high by the action of the Low Voltage Detector on Module 3. ATU PROT 2 is held at '0'. The result of this combination is detailed in Table 5.

2FS

73. In the 2FS mode of operation, the HF R/T receives and transmits on two different frequencies. To avoid any unnecessary insertion loss in the receive mode, all previously selected network tuning components in the HF ATU are switched out of circuit to present a direct path between the RF INPUT at SK1 on the front panel and the HF ATU output on Module 6. The data on the transmit tuned circuit configuration is held in RAM, and when the HF R/T is returned to the transmit mode, the data is retrieved, allowing the original tuning components to be switched back into circuit.

74. To inform the Microprocessor (Module 3) that the HF R/T is in the 2FS mode, 1PL1-M 2FS (Module 1) is taken to '0' by the HF R/T and applied to the Control Flag Selection Multiplexer on Module 3 3PL2-6 via 1PL2-9.

75. In the 2FS mode, a RESET signal ('0') is output from the HF R/T to the HF ATU on each application of the Tx/Rx signal. The RESET is generated at the trailing edge of the low to high transition (HF R/T changing from transmit to receive) of each Tx/Rx signal, and applied to the Microprocessor via 3PL2-4. The Microprocessor then puts the HF ATU in the bypass condition (all selected components switched out of circuit). The next Tx/Rx signal (HF R/T transmit) takes the Tx/Rx signal from high to low and the network tuning components are switched back in circuit.

76. If a change of frequency is required when the HF R/T is operating in the 2FS mode, then 2FS is taken to '1', and remains at '1' until the tuning is completed, when it is then taken back to '0'.

Power Supplies (Figure 7)

77. A power supply interconnection diagram is shown at Figure 7. The 28 Vdc supply for the HF ATU is routed from the front panel CONTROL connector to Module 1 (1PL1-C,N), through Low-pass Filters to 1PL2-1,2 and out to 2PL2-1,2 on Module 2. From here, it passes directly to 2PL5-1,2 and out to the protection devices diode D1 and the front panel fuse FS1, before returning to Module 2 at 2PL3-1,2.

78. From 2PL3-1,2, the 28 Vdc is routed to the 19 V regulator, which is enabled if 10 V (from the HF R/T) is present on 2PL2-4 (SYSTEM ON). A 10 V signal (ATU PRESENT) is then routed from the 19 V regulator to the HF R/T via 2PL2-3, 1PL2-12, 1PL1-D and the CONTROL connector on the HF ATU front panel.

79. The +19 V regulator supplies the +5 V, +5 V (SWD) and +10 V (SWD) regulator circuits. The outputs of all the four regulators on Module 2 are applied to Module 3, which acts as a distribution point for the voltage rails of Modules 4, 5 and 6. The +5 V (SWD) and +10 V (SWD) regulators are switched on and off by the application of the PSU CONTROL signal (from Module 3) on 2PL6-6.

80. Distribution of the regulated voltage supplies is as follows:

a. +19 V:- Provides a 19 V rail for Module 3. This rail also supplies power for a +12 V regulator.

b. +12 V:- Derives from the 19 V rail and supplies the reference voltage for the power and current detectors on Module 4.

c. +10 V (SWD):- Provides switchable power for the phase, conductance and dc resistance measuring output comparators.

d. +5 V (SWD):- Provides switchable power for the RF counter and the A to D converter input circuits.

e. +5 V:- General use (CMOS devices, pull-up resistors etc).

BITE

81. The HF ATU contains a software program which enables the RAM and EPROM on Module 3 to be tested. The program runs automatically when the system is powered up, or may be initiated by disconnecting 4PL2 from Module 4 when the HF ATU is in operation. This action removes the 0 V line from the Control Flag Selection Multiplexer.

82. When the system is powered up, a successful RAM and EPROM test is indicated by LED D10 being illuminated. If the test is initiated by 4PL2 being removed, then the no fault condition is shown by D10 flashing once every second. LED D10 is mounted on Module 3 and can only be viewed with the HF ATU cover removed, i.e. during maintenance or fault finding.

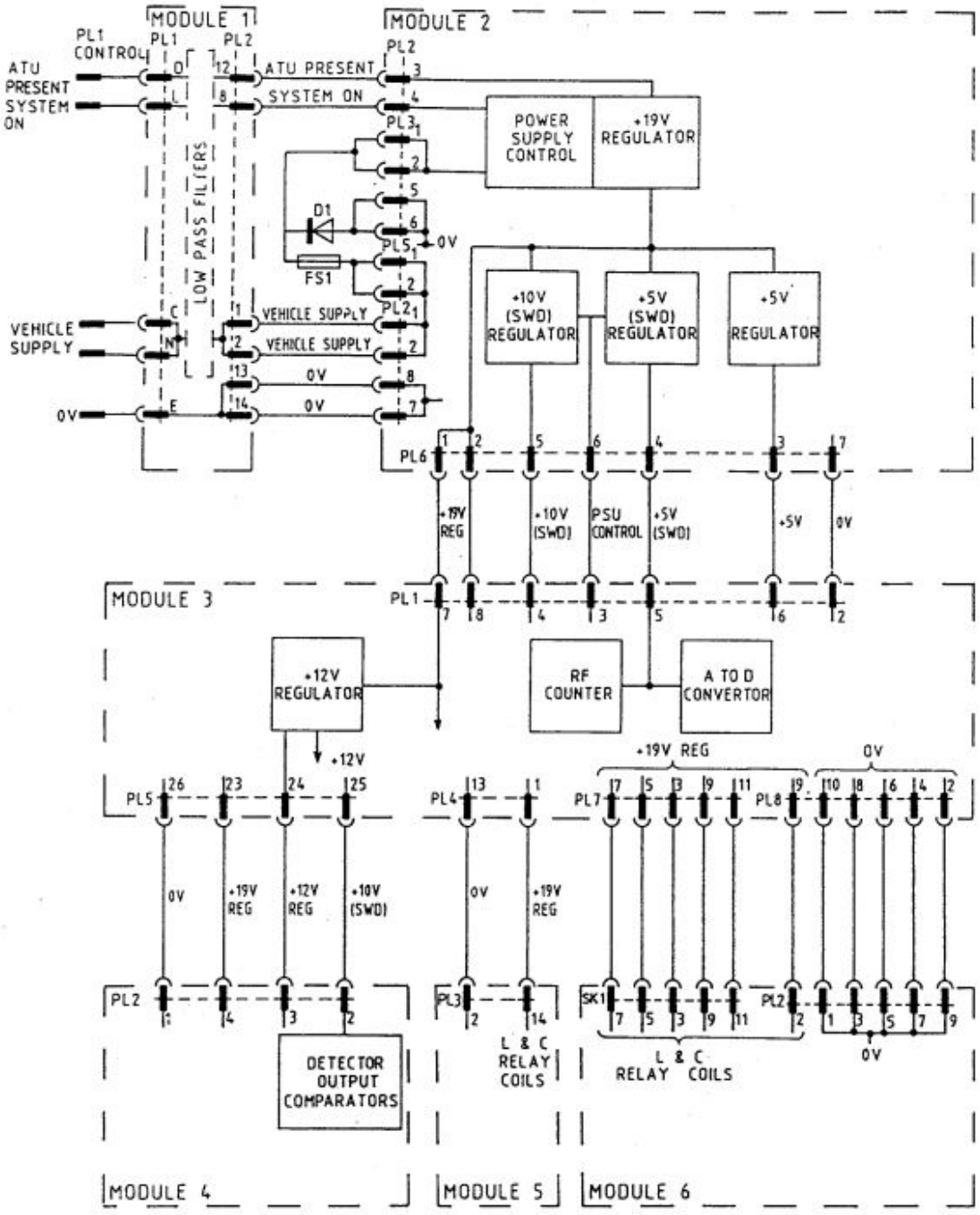

FIGURE 7 - POWER SUPPLY INTERCONNECTION DIAGRAM

MODULE 1 - MULTIWAY FILTER BOARD

General

83. Module 1 is a panel electronic circuit mounted on the rear of the front panel control plug PL1, and provides low-pass filtering on each of the plug's control lines.

Circuit Description

84. The circuitry of Module 1 is shown at Figure 1002 and comprises nine identical Low-pass Filters for logic signals, one Low-pass Filter (with higher value zener diode) for the vehicle power supply, and one non-filtered through connection for the earth line.

85. Each filter comprises a Ferrite Bead inductor, a 10nF Capacitor and a Zener Diode, the latter acting as a transient absorption diode to give electromagnetic pulse protection. The Zener Diode in the 28 V supply line is a back-to-back diode and acts as a clipping diode. A typical Low-pass Filter is shown at Figure 8.

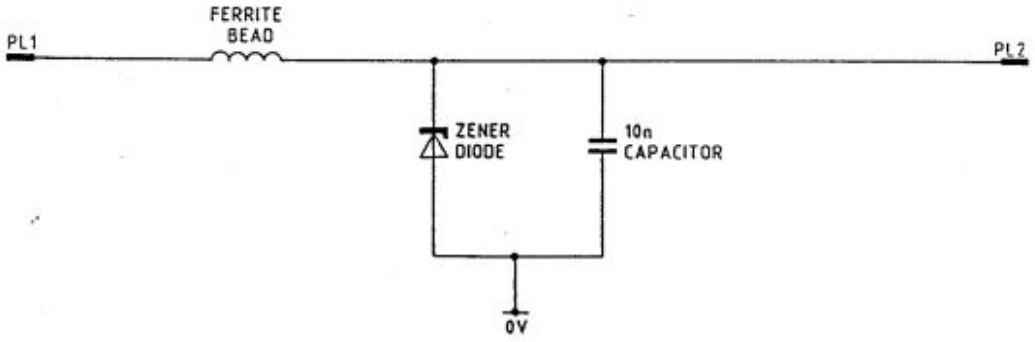

FIGURE 8 - TYPICAL LOW-PASS FILTER

MODULE 2 - POWER SUPPLY UNIT

General

86. Module 2 converts the nominal 28 V external system supply into regulated dc outputs of +19 V, +5 V, +5 V (SWD) and +10 V (SWD). To reduce current drain and unnecessary interference when the unit is not tuning, the switchable 5 V (SWD) and 10 V (SWD) regulated outputs are switched off by a PSU CONTROL signal from Module 3.

87. A functional block diagram of Module 2 is shown in Figure 9 and a detailed circuit diagram is shown in Figure 1003. With reference to Figure 9, Module 2 comprises the following functional circuit blocks:

a. Power Supply Control and +19 V Regulator Circuits.

b. +5 V Regulator Circuit.

c. +5 V (SWD) Regulator Circuit.

d. +10 V (SWD) Regulator Circuit.

88. Module 2 is activated by a +10 V SYSTEM ON control signal from the HF R/T. To indicate the presence of the HF ATU in the HF R/T's output path, an active high (10 V) ATU PRESENT signal is sent to the HF R/T from the +19 V regulator circuit.

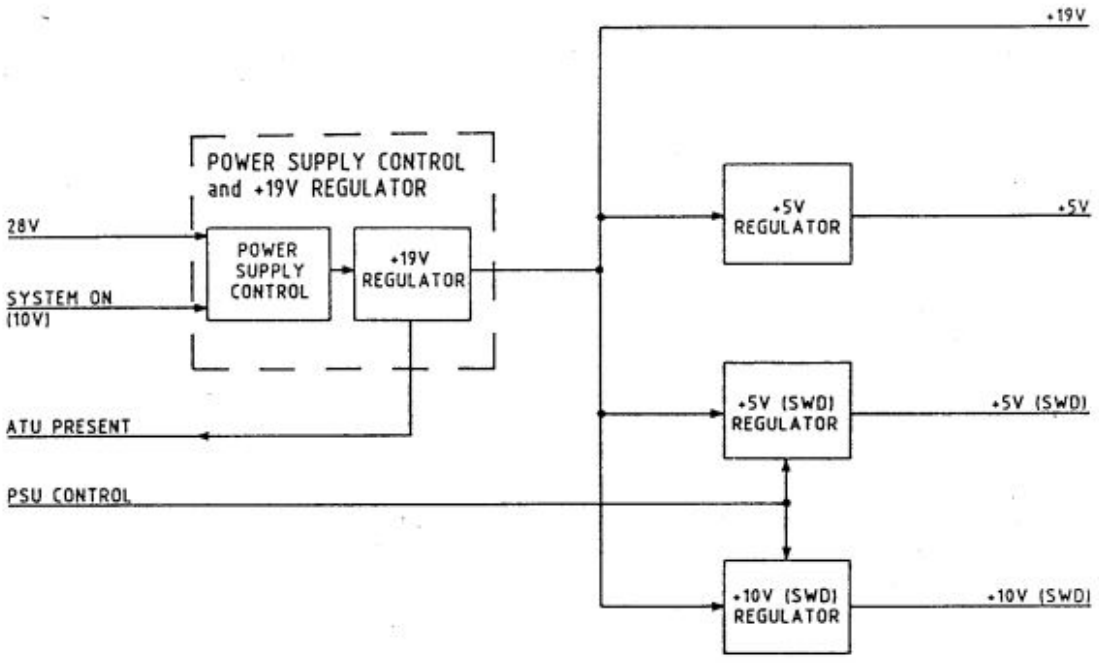

FIGURE 9 - MODULE 2 FUNCTIONAL BLOCK DIAGRAM

Power Supply Control and + 19 V Regulator Circuits

Power Supply Control. (Figure 10, Figure 1003)

89. The nominal 28 Vdc supply enters Module 2 at 2PL2-1,2 and leaves at 2PL5-1,2. From here, it is fed to 2PL3-1,2 and the 19 V Regulator Circuit via the reverse polarity protection circuit formed by D1 and FS1. Components L1, C1 and C2 form a low-pass filter to remove any RF present on the 28 V supply. R1 and R2 damp the inductance of L1 which may cause the 19 V Regulator Circuit to oscillate.

90. The Power Supply Control and 19 V Regulator Circuits are activated by the presence of the nominal 28 Vdc supply and a + 10 V SYSTEM ON control signal from the HF R/T. With the HF R/T powered up, the SYSTEM ON control signal is applied to the gate of TR3 via 2PL2-4. Resistor R7 in the gate circuit of TR3 provides current limiting with capacitor C3 decoupling high frequencies. R8 ensures TR3 is off in the absence of a 10 V SYSTEM ON signal, and also prevents static building up on TR3 when it is switched off.

91. TR3 is an N channel Metal Oxide Semiconductor Field Effect Transistor (MOSFET) which, in this configuration, acts as a digital switch to switch on/off TR4. With its source grounded, TR3 is turned on by the positive potential on its gate. Therefore, with a nominal 28 V on TR3 drain and approximately 5 V at TR3 gate, TR3 is turned on which, in turn, causes TR4 to switch on.

92. The action of switching TR4 on causes the 19 V regulator TR8 to be switched on via TR5, TR6 and TR7.

+ 19 V Regulator Circuit. (Figure 10, Figure 1003)

93. The 19 V Regulator Circuit is formed by TR8 and its associated components. When TR4 is switched on by TR3, avalanche current flows through D4 and the junction of R11 and R12 is taken to 3.3 V. This forward biases the base/emitter junction of TR5. TR5 is switched on, and the resultant collector current causes a voltage drop across R13, switching on TR6.

94. When TR6 switches on, the resultant drop in its collector potential is passed to TR7 (via R15), causing TR7 to switch on. This results in the 28 V at TR7 emitter being passed to TR7 collector. From the external connections at 2PL1-2 and 2PL1-3, the 28 V at TR7 collector switches on TR8 and the 28 V input is effectively passed from the collector of TR8 to its emitter.

95. Transistors TR5, TR6, TR7 and TR8, and their associated components, form a regulator control amplifier circuit to regulate the output of the 19 V regulator. This circuit operates by varying the gain of transistors TR5, TR6, TR7 and TR8 to compensate for variations in output voltage level.

96. Any voltage fluctuation in the 19 V rail (TR8 emitter) will result in a change in the voltage on TR5 base which is derived from the potential divider R17, R18 and R19. TR5 forms a voltage comparator with a reference voltage supplied by zener diode D4. With its emitter held constant by the reference voltage from D4, TR5 forward bias will be varied and this will be reflected in a change to the forward bias on TR6 via the voltage drop across R13. The current drive to TR7 and TR8 will therefore be varied so that a rise in the voltage on TR8 emitter will result in a drop in the base current drive to TR8, thus bringing the voltage rail back to 19 V. R14 and R15 provide the bias voltage for TR7 and C6 stabilises the circuit to prevent oscillations.

97. If the vehicle supply rises above 36 V, current flows through zener diode D2 and resistors R5 and R9, resulting in TR2 being turned on. This places 0 V on TR6 base which removes the current drive to TR7 and therefore turns TR8 off.

98. The 10 V ATU PRESENT signal is taken from the anode of the zener diode D5 and passed to PL2-3 via the decoupling network formed by R43 and C19.

99. The 19 V regulated supply is filtered by C8 and C9 and fed out on PL6-1 and PL6-2; LED D6 illuminates when this voltage is present.

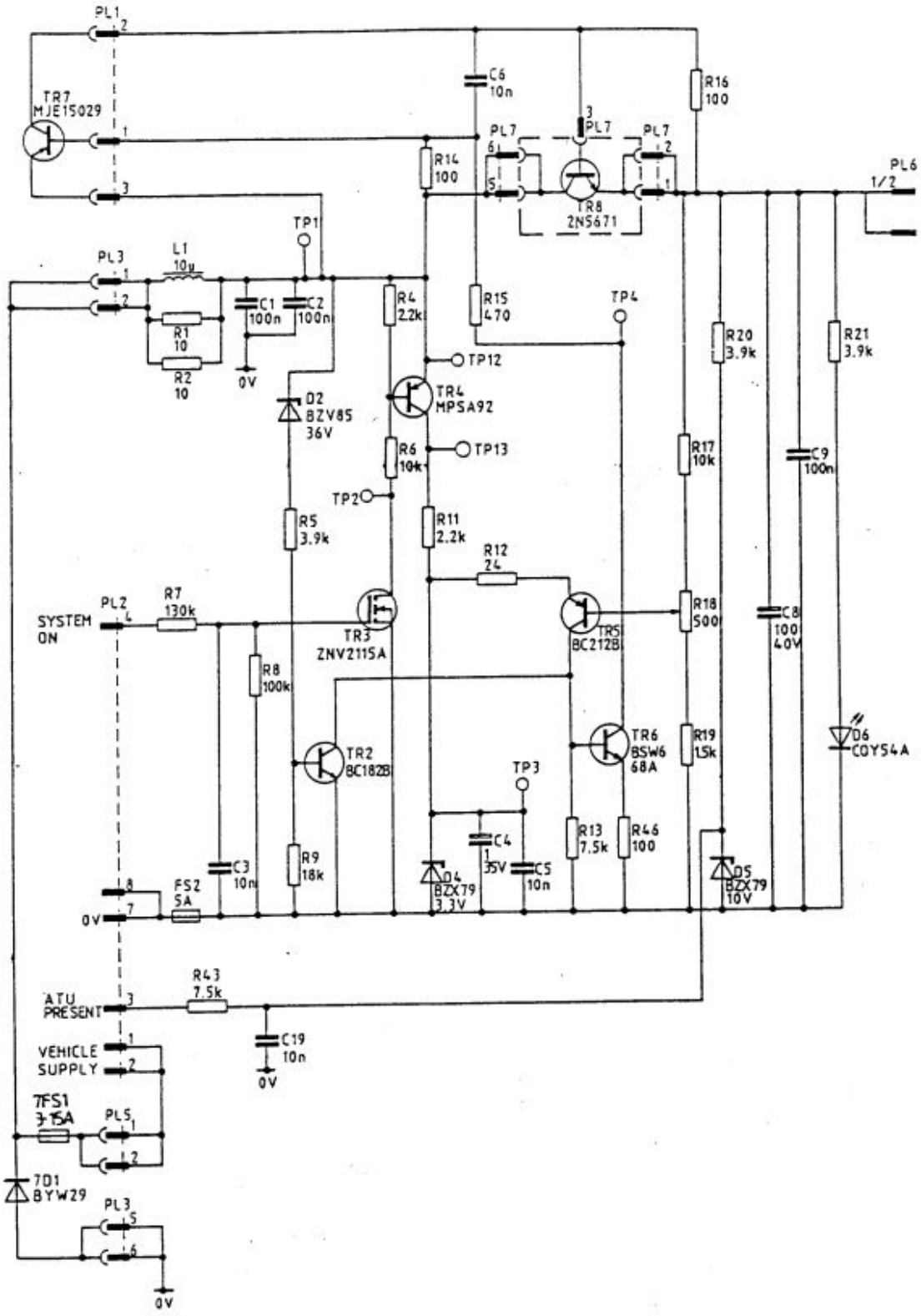

FIGURE 10 - POWER SUPPLY CONTROL AND + 19 V REGULATOR CIRCUITS

+5 V Regulator Circuit (Figure 11, Figure 1003)

100. The 5 V regulator is formed by the Voltage Regulator IC1 and its associated components. The voltage supply to the input of IC1-2 is derived from the 19 V regulated output via link LK2. At the input to IC1, L2 provides protection against excessive current surges (nuclear hardening) and C10 provides decoupling.

101. The regulated 5 V output at IC1-1 is taken via the current sensing resistor R22 to the base of the heat sink mounted transistor 7TR9. With the collector of 7TR9 at 19 V from 2PL4-2, the 5 V output is taken from Module 2 at 2PL6-3 via R24 and the base/emitter junction of 7TR9.

102. The voltage drop across R22 is applied to IC1-8 to keep the internal current regulator transistor in a determined state.

103. When IC1 is used in this configuration, current limiting is performed by TR10 and its associated components. If the output current from the regulator increases above a pre-determined level, the voltage drop across R24 switches on TR10. Because of the connection between TR10's collector and IC1-7 (INH), the switching on of TR10 will cause the regulator's output to be turned down. The action of this current limiting circuit is such that an excessive voltage drop across R24 (high regulator output) will switch off IC1, thereby setting the regulator's output to 0 V.

104. The regulator reference voltage applied to IC1-6 is obtained from the junction of the resistors R25 and R26. C12 provides frequency compensation for the regulator and C11 decouples the reference voltage. A visual indication of the presence of the +5 V supply on 2PL6-3 is provided by the LED D7; R27 limits the current to D7.

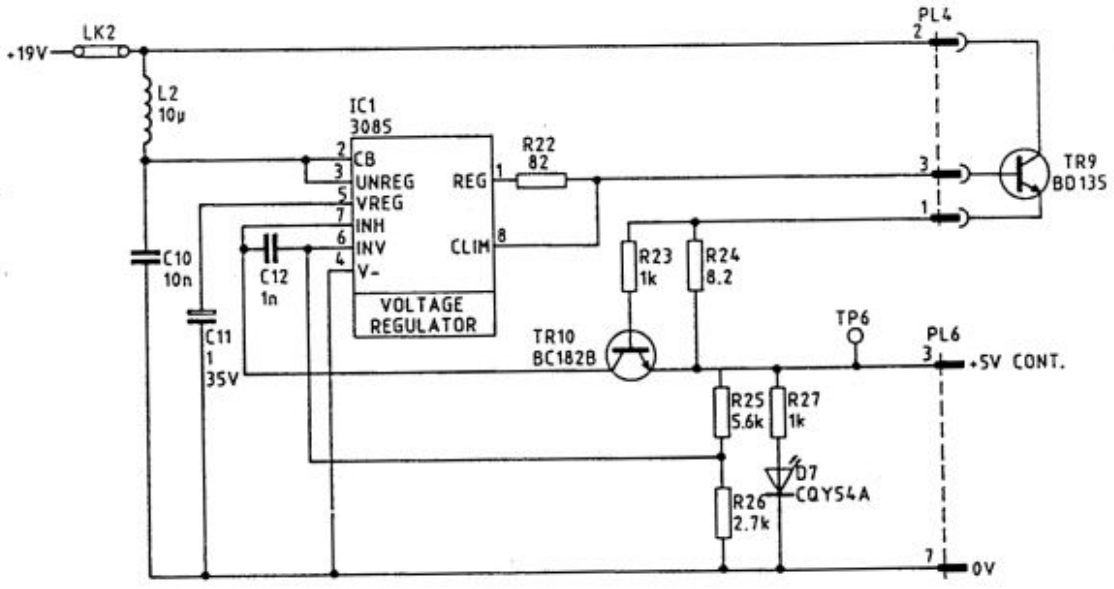

FIGURE 11 - +5 V REGULATOR CIRCUIT

+5 V (SWD) Regulator Circuit (Figure 12, Figure 1003)

105. The action of the switched +5 V (SWD) Regulator Circuit is identical to the non-switched Regulator Circuit already described, but with the addition of a delay circuit and a PSU CONTROL switching circuit.

Delay Circuit.

106. At initial switch on, application of the 5 V (SWD) supply is delayed until the +5 V continuous supply is established. This prevents an input to the frequency counter CMOS gates on Module 3 forward biasing the gates before the 5 V VCC is present. The delay circuit is provided by C20, R44, R45, D10 and TR17.

107. When the 19 V rail rises to its stable state, the rail voltage is initially developed across R44 with C20 acting as a short circuit. TR17 base emitter junction is forward biased and its collector is taken towards 0 V. This is applied to IC2-7 (INH) to hold the regulator off. As C20 charges up, the voltage across R44 drops, eventually turning off TR17 and therefore allowing the regulator to conduct.

108. When the system supply is switched off, the 19 V rail falls rapidly to 0 V. This causes the voltage at the junction of R44 and R45 to drop to -19 V. Under these conditions, D10 will become forward biased, effectively short circuiting the base emitter junction of TR17, which would otherwise be destroyed by this large reverse bias applied to it.

Switching Circuit.

109. The +5 V (SWD) supply is turned on by an active low (0 V) PSU CONTROL signal supplied by the microprocessor on Module 3 via 2PL6-6. The on/off switching control circuit is provided by D9, R41, R34 and TR13.

110. When the regulator is to be switched off, the PSU CONTROL line (2PL6-6) is set high (18-21 V). This causes avalanche current to flow in D9 and TR13 is biased on by R41 and R34. TR13 collector is taken towards 0 V and this is applied to IC2-7 (INH), turning the regulator off. In order to switch the regulator on, the PSU CONTROL line is taken low, removing the 18-21 V from D9 anode and therefore turning TR13 off.

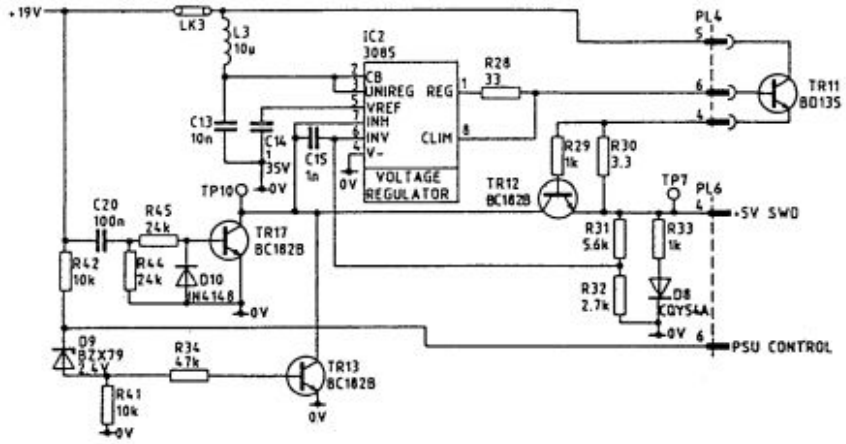

FIGURE 12 - +5 V SWITCHED REGULATOR CIRCUITS

+10 V (SWD) Regulator Circuit (Figure 1003)

111. The action of the +10 V (SWD) Regulator Circuit is identical to the 5 V (SWD) circuit already described. The switching action is again controlled by the PSU CONTROL line with TR16 being switched on and off in conjunction with TR13 on the 5 V (SWD) regulator. The regulated voltage output is applied to 2PL6-5.

MODULE 3 - MICROPROCESSOR BOARD

General

112. Module 3 contains the Microprocessor and control circuits which control the overall operation of the HF ATU, in accordance with the various control and RF signals received at its inputs from associated HF equipments. Under control of software stored in non-volatile EPROM memory, the Microprocessor selects the impedance matching inductors and capacitors within the HF ATU. These components are selected by the Microprocessor evaluating data applied to it from the detectors in Module 4.

113. A functional block diagram of Module 3 is shown at Figure 13 and a detailed circuit diagram is shown in Figure 1004. With reference to Figure 13, Module 3 comprises the following functional circuit blocks:

a. Microprocessor and Program Memory Circuits.

b. Power-Up Reset.

c. Clock.

d. Clock Start.

e. Clock Stop.

f. RESET and Tx/Rx Inputs.

g. Clear RESET Line.

h. Control Flag Selection Multiplexer.

i. Frequency Counter.

j. Analogue to Digital Converter.

k. D-Type Latches.

l. Output Port Signals.

m. Input Port Signals.

n. Output Driver Circuits.

o. Low Voltage Detector.

p. Starting Disturbance Detector.

q. ATU Protection Circuits.

r. ATU PROT 1/ATU PROT 2 Output Circuits.

s. Voltage Supply Protection.

t. PSU Control Switching.

u. BITE RAM/ROM Tests.

114. Various protection circuits and low voltage detectors are used within Module 3 to regulate the input power, or close down the Microprocessor, in the event of a fault. With reference to the technical descriptions of this module, a '1' is 5 V CMOS logic 1 signal (4.5 - 5.2 V) and a '0' is 0 V CMOS logic 0 signal (0 - 0.5 V).

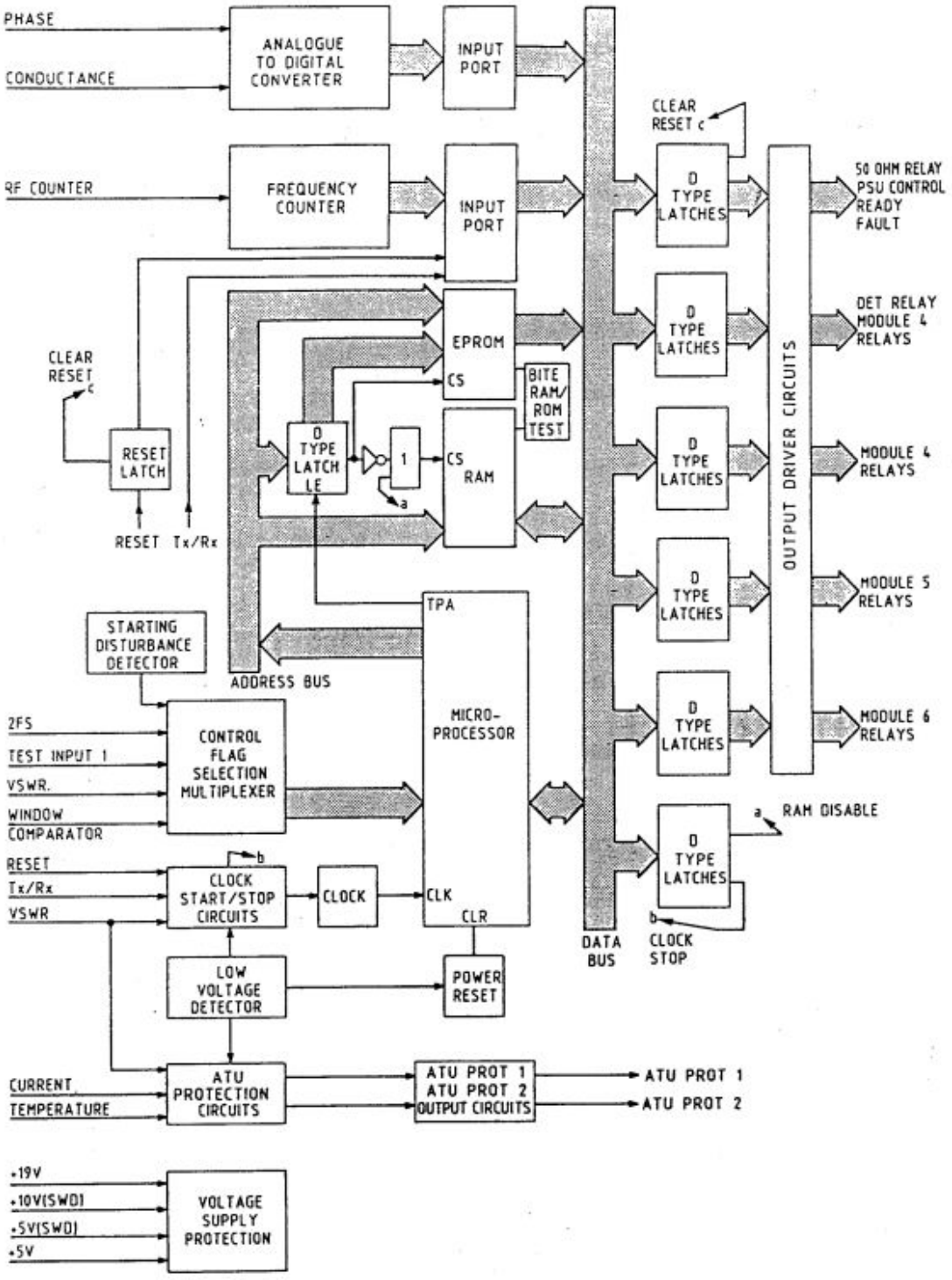

FIGURE 13 - MODULE 3 FUNCTIONAL BLOCK DIAGRAM

Module 3 Inputs. (Figure 1004)

115. Because of the complexity of this module, the functions of all inputs to the microprocessor circuits are detailed below in Table 6.

TABLE 6 - MODULE 3 INPUT FUNCTIONS

INPUT	CONNECTOR	FUNCTION
RF COUNTER	3PL5-2	Conveys the RF carrier from Module 4 to the frequency counter.
ANALOGUE PHASE	3PL5-18	Conveys the output of the phase detector on Module 4 to the analogue to digital converter.
ANALOGUE COND	3PL5-17	Conveys the output of the conductance detector on Module 4 to the analogue to digital converter.
VSWR	3PL5-19	Indicates the presence of a VSWR fault detected by the VSWR detector on Module 4.
Tx/Rx	3PL2-3	Indicates to the Microprocessor the operational state of the HF R/T, i.e. receive or transmit.
RESET	3PL2-4	Signal from the HF R/T indicating to the microprocessor that a tune sequence is imminent.
2FS	3PL2-6	Signal from the HF R/T indicating either normal or two frequency simplex mode.
TEST INPUT 1	3PL5-3	Normally hard-wired to 0 V in Module 4 to set the microprocessor to the normal mode; when disconnected at 4PL2 sets up self-test mode.
TEST INPUT 2	3PL2-11	Not used (Figure 1004).
WINDOW COMPARATOR	3PL5-20	Indicates that the RF power or antenna resistance measured in Module 4 is faulty.
TEMP 1, TEMP 2, TEMP 3, RETURN	3PL3-2,3 3PL6-2,3 3PL5-1 3PL3-4/PL6-4	These lines signal the temperature sensing circuit that the maximum permissible temperature has been exceeded.
CURRENT TRIP	3PL5-22	Indicates to the current sensing circuit that the circulating currents in Module 4 are excessive.
+19 V	3PL1-7,8	+19 V regulated supply from Module 2.
+10 V (SWD)	3PL1-4	Switched +10 V regulated supply from Module 2.
+5 V (SWD)	3PL1-5	Switched +5 V regulated supply from Module 2.
5 V	3PL1-6	+5 V regulated supply from Module 2.

Module 3 Outputs. (Figure 1004)

116. The functions of the main outputs from Module 3 are detailed below in Table 7. All other outputs from Module 3 which are not specified in Table 7 are drives to relays on Modules 4, 5 and 6.

TABLE 7 - MODULE 3 OUTPUT FUNCTIONS

OUTPUT	CONNECTOR	FUNCTION
DET OFFSET VOLT	3PL5-21	Outputs a fixed voltage of 2.5 V to act as a reference for the phase and conductance detectors on Module 4.
50 OHMS RELAY	3PL5-13	Controls the 50 Ohm relay on Module 4.
PSU CONTROL	3PL1-3	Controls the operation of the 5 V (SWD) and 10 V (SWD) supplies in Module 2
TEST OUT	3PL2-9	Not used.
READY	3PL2-1	Indicates to the HF R/T that the HF ATU has successfully tuned.
FAULT	3PL2-2	Indicates to the HF R/T that tuning has been unsuccessful.
DET RELAY	3PL5-16	Controls the detector relays in Module 4.
ATU PROT 1	3PL2-7	Used with ATU PROT 2 to control the system output power.
ATU PROT 2	3PL2-5	Used with ATU PROT 1 to control the system output power.
+19 V OUT	3PL5-23 3PL4-1 3PL8-9 3PL7-3,5,7,9,11	19 V supply to other modules.
+10 V (SWD)	3PL5-25	Switched 10 V supply to Module 4.
+12 V	3PL5-24	12 V supply to Module 4.

Microprocessor and Program Memory Circuits (Figure 14, Figure 1004)

117. The Microprocessor and associated memory circuits enable the HF ATU to process the program instructions and data held in EPROM and RAM. A basic block diagram of the Microprocessor and memory circuits is shown in Figure 14.

118. The Microprocessor IC24 is an RCA CDP1802 8-bit register-orientated device with the capability of addressing up to 256 bytes of memory.

119. To retain the program when the system supply is removed, a non-volatile EPROM device IC22 is used. IC22 is a 27C32 low power CMOS device which is organised as 4096 x 8 bits (4K). RAM device IC21, organised as 32 x 8 bits, is used to retain data during a brief system supply interruption.

120. To extend the Microprocessor's memory addressing capability beyond 256 bytes, a CMOS D type 8-bit latch IC16 is used as an interim address store. This device, together with the NAND Schmitt trigger IC35D and the OR gate IC48A, also provides the necessary switching logic to enable IC21 when required. A second input to IC48A from the low voltage detector circuit is used to inhibit IC21 during low supply voltage conditions.

121. To allow all 4K of EPROM memory to be accessed, the first Microprocessor read instruction cycle outputs the high order address bits (A8 to A11) and the IC22 Chip Enable (CE) signal onto the address bus. These signals are then clocked into latch IC16 by the timing pulse TPA. On the next read instruction cycle, the low order address bits (A0 to A7) are output on the address bus and therefore onto IC22's A0 to A7 inputs. With the CE already applied to IC22 by the latch, and the full 12-bit address available to IC22, memory data is placed on the data bus (D0-D7) by the Microprocessor setting MRD active low. With reference to Figure 1004, IC29 is a jumper pack wired across the data bus, used only during fault finding, and IC28 is a resistor pull-up pack on the data bus.

Note: when required, the Microprocessor writes data to RAM device IC21 by a low transition on MWR after the address lines have stabilized.

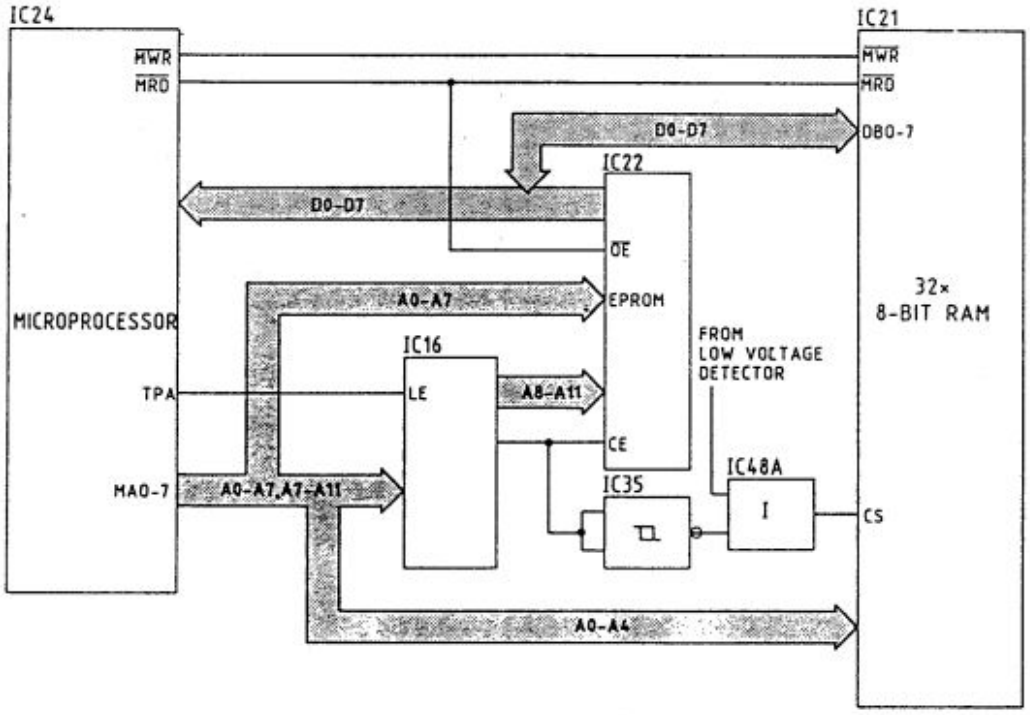

FIGURE 14 - MICROPROCESSOR AND MEMORY BASIC BLOCK DIAGRAM

Power-up Reset Circuit (Figure 15, Figure 1004)

122. When the system supply is switched on, it is necessary for the Microprocessor IC24 to be initialised to a predetermined state. This is achieved by holding the Microprocessor's CLR input (IC24-3) low immediately after VCC (5 V) has been applied to the Microprocessor. With IC24-2 (WAIT) hard-wired high and IC24-3 (CLR) held low, the microprocessor is forced into a reset state. During reset, all registers are cleared, the Microprocessor's Interrupt Enable is set, and '0's are placed on the data bus lines.

123. The Power-up Reset Circuit is shown in Figure 15. With the system supply above 19.5 V, the output at IC17A-1 is a '1' (see low voltage detector circuit description). This '1' is applied to R25 which results in C26 starting to charge up. For the time the voltage on IC35B-4,5 is below the '1' threshold (3.5 V), the NAND output at IC35B-6 is a '1'. This '1' is then inverted by NAND gate IC35A to present a '0' to the Microprocessor's CLR input (IC24-3).

124. The '0' from IC35A-3 is held on IC24-3, forcing the Microprocessor into a reset state. When C26 has charged above 3.5 V, the '0' on CLR (IC24-3) is removed and the CPU resumes normal operation. In the next cycle after a reset state, the Microprocessor fetches the contents of memory location 0000 and begins to execute the firmware program.

125. If the output of the Low Voltage Detector should become '0' due to a drop in the system supply below 19.5 V, it is necessary to hold the '1' on IC24-3 (CLR) until a signal has been output on the data bus to turn off the clock oscillator. This delay is achieved by allowing C26 to discharge through the forward biased diode D7 and R141. CLR will therefore not fall to '0' until C26 has discharged below 1.5 V.

126. An output is taken from IC35B-6 to the reset input of the binary counter used in the current sensing detector. After initial system switch on, the transient '1' on IC35B-6 resets the counter to zero.

127. The transient '0' on IC24-3 is also used as an input to the Clock Start Circuit to provide clock pulses to the Microprocessor during reset.

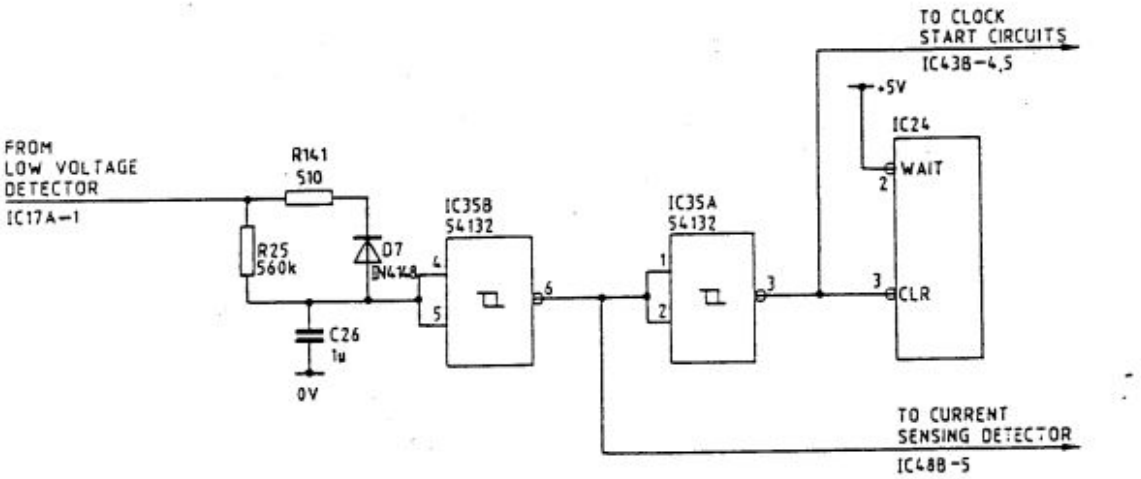

FIGURE 15 - POWER-UP RESET CIRCUIT

Clock Circuit (Figure 16, Figure 1004)

128. The Microprocessor operates from an external clock input of 1.4 MHz applied to its CLK input connector (IC24-1). The clock oscillator comprises the crystal XL1 and its associated components C4, C3, R14, and IC32C.

129. The Clock Circuits are switched on and off by a control signal from the Clock Start/Stop Circuits applied to IC32C-9. A '1' output from IC1-2 will switch the crystal oscillator on; a '0' output from IC1-2 will switch it off.

130. A gating circuit formed by R16, C5, IC33C and IC33B is employed to provide a gating pulse to IC33A. This circuit has a 25 ms delay created by R16 and C5 which allows the crystal oscillator to stabilise before clock pulses are applied to the Microprocessor via IC32D and IC33A.

131. With a '1' on the NAND gate IC32C-9, the crystal oscillator will be switched on and an inverted oscillator output will appear on IC32C-10. The '1' at IC32C-9 is also passed to IC33C-9 and the CR circuit formed by R16 and C5, the voltage across R16 taking approximately 25 ms to charge C5. When the voltage across C5 exceeds 3.5 V, the gating signal will be inverted by IC33C and IC33B, and passed to the gating device IC33A-2.

132. The oscillator output is inverted by IC32C and IC32D, and 'clocked' through IC33A by the delayed gating signal and applied to IC24-1. R14 ensures linearity across IC32C.

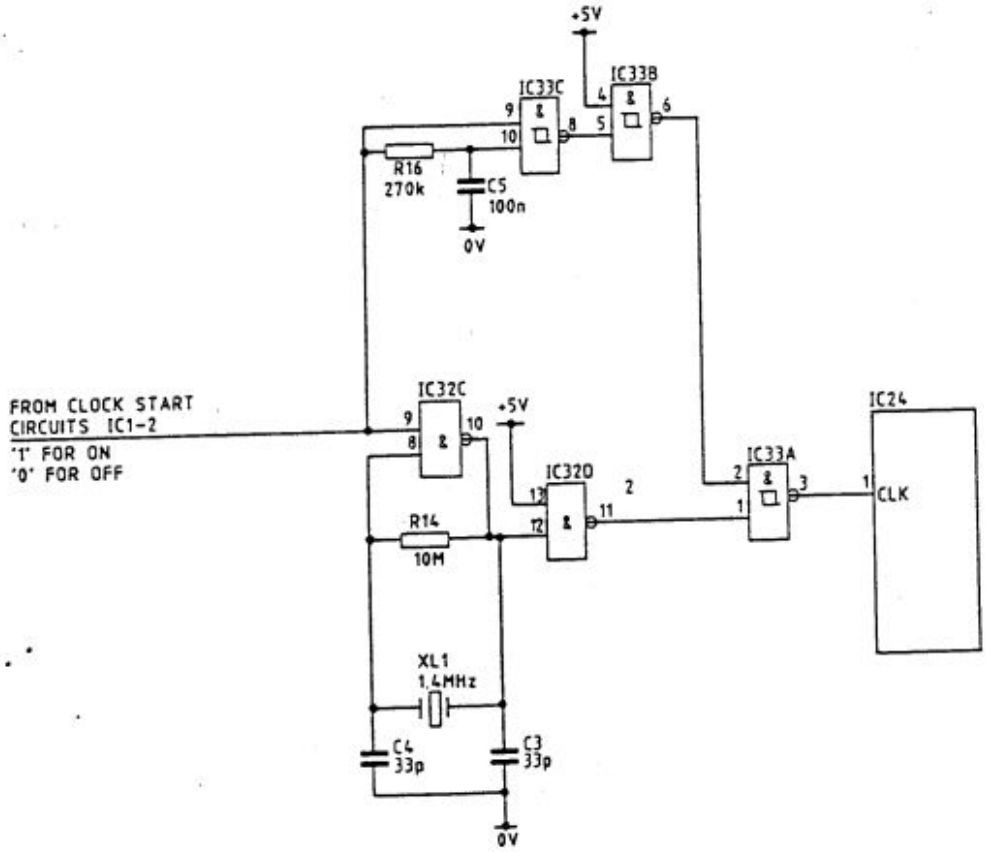

FIGURE 16 - CLOCK CIRCUIT

Clock Start Circuit (Figure 17, Figure 18, Figure 1004)

133. The Clock Start Circuit starts the microprocessor clock in the following circumstances:

a. Upon receipt of an active low (transmit) Tx/Rx control signal from the HF R/T at 3PL2-3.

b. Upon receipt of a RESET pulse from the HF R/T at 3PL2-4.

c. Upon receipt of an active low VSWR fault signal from Module 4 at 3PL5-19. In this case, Tx/Rx must also be low (transmit mode).

d. Upon receipt of a '0' from the Power-up Reset Circuit (IC35A-3).

134. The clock start circuit operates by sending an active '1' to the control gate of the clock circuit (IC32C-9) to start the microprocessor clock. With reference to the logic diagram Figure 17, the Clock Start Circuit accepts a '0' input from the three external inputs VSWR, Tx/Rx and RESET, or from the Power-up Reset Circuit (IC35A-3).

135. As shown in Figure 17, each input signal is inverted to form a wired OR configuration with all inputs independently capable of starting the clock, with the exception of VSWR which must have Tx/Rx present.

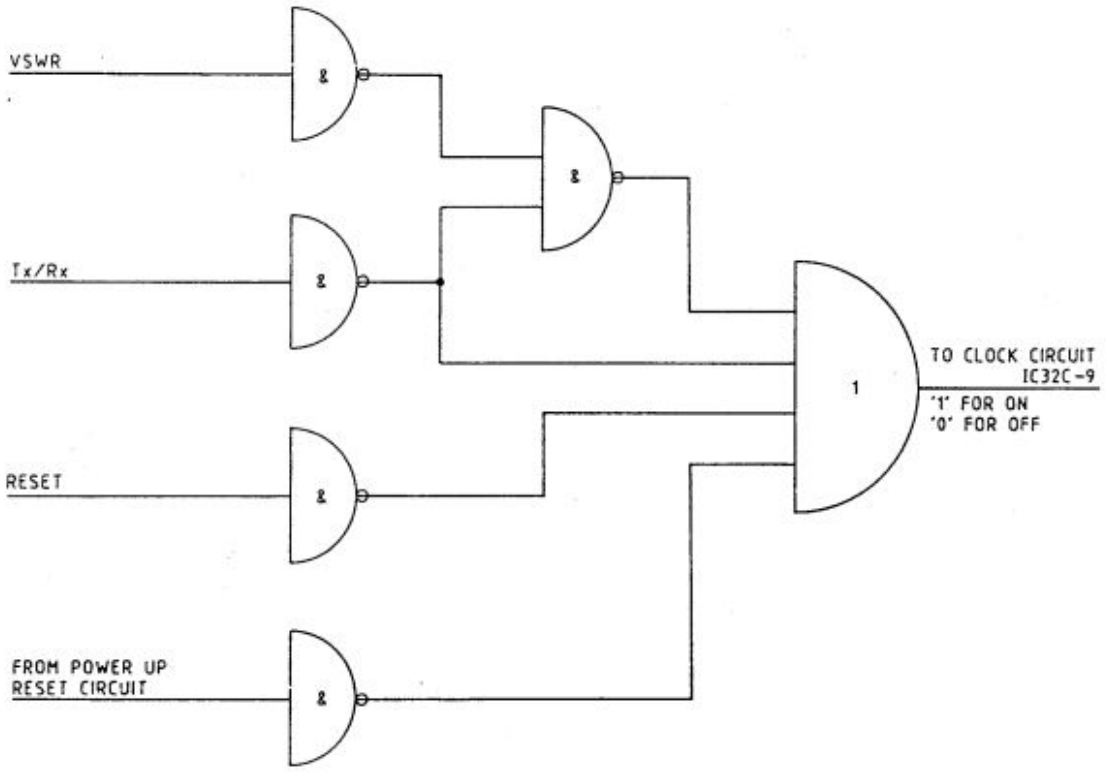

FIGURE 17 - CLOCK START LOGIC DIAGRAM

136. With reference to the circuit diagram at Figure 18, the output of the wired OR gate formed by D23, D24, D25 and D32 is passed to the bi-lateral switch IC5C.

137. The switch is closed by a '1' applied to IC5-6 from the Low Voltage Detector (IC17A-1), which will hold this line at '1' as long as the system supply is above 19.5 V. R103 acts as a 0 V pull down resistor for the CMOS device IC1.

138. A '1' on IC5C-8 will be passed through the bi-lateral switch and applied to IC1-4, a NOR implementation R-S latch triggered by changing logic levels on its R and S inputs. With a '1' applied to the S0 input (IC1-4) and a '0' provided by the Clock Stop Circuit (IC48C-8) on the R0 input (IC1-3), the Q0 output (IC1-2) will go to '1', thus switching on the Clock Circuit.

139. A '1' from the Clock Stop Circuit at the RO input and a '0' on the SO input will reset the QO output to '0', thus switching the clock off.

140. The circuit action of the various input signals to the wired OR gate is described in the following sub-paragraphs.

Tx/Rx and RESET. (Figure 18, Figure 1004)

141. The Tx/Rx and RESET circuits convert the current sink Tx/Rx and RESET inputs at 3PL2-3 and 3PL2-4 respectively into 5 V (logic 1) or 0 V (logic 0) CMOS format. The action of these two circuits is identical and therefore only the Tx/Rx input is described.

142. With an active low (less than 0.5 V) applied to PL2-3, D1 becomes forward biased and current flows through the biasing resistors R1 and R27, turning the inverting buffer TR2 on. TR2 collector is taken high and, with D24 forward biased, a '1' is applied to IC5C-8. This '1' is then passed through the IC5C and IC1 to provide a '1' to switch the Clock Circuit on.

VSWR. (Figure 18, Figure 1004)

143. An active low on PL5-19 will be inverted by IC34E and the resultant '1' applied to the gating device IC52A-1. The output of IC52A-3 will only be '0' when Tx/Rx and VSWR are active low simultaneously. The '0' on IC52A-3 is inverted by IC52D and the '1' on IC52D-11 will forward bias D25, applying a '1' to IC5C-8.

144. An output is taken from IC52A-3 to the ATU Protection Circuits (IC52B-4,5) to reduce the input power to the unit in the event of a VSWR fault.

Power-up Clock Start. (Figure 18, Figure 1004)

145. When the system supply is switched on, a logic '0' is taken from the Power-up Reset Circuit (IC35A-3) and applied via the current limiting resistor R139 to IC43B-4,5. The '0' is inverted by IC43B and the resultant '1' on IC43B-6 forward biases D32, placing a '1' on IC5C-8. This circuit provides clock pulses to the microprocessor during its reset state.

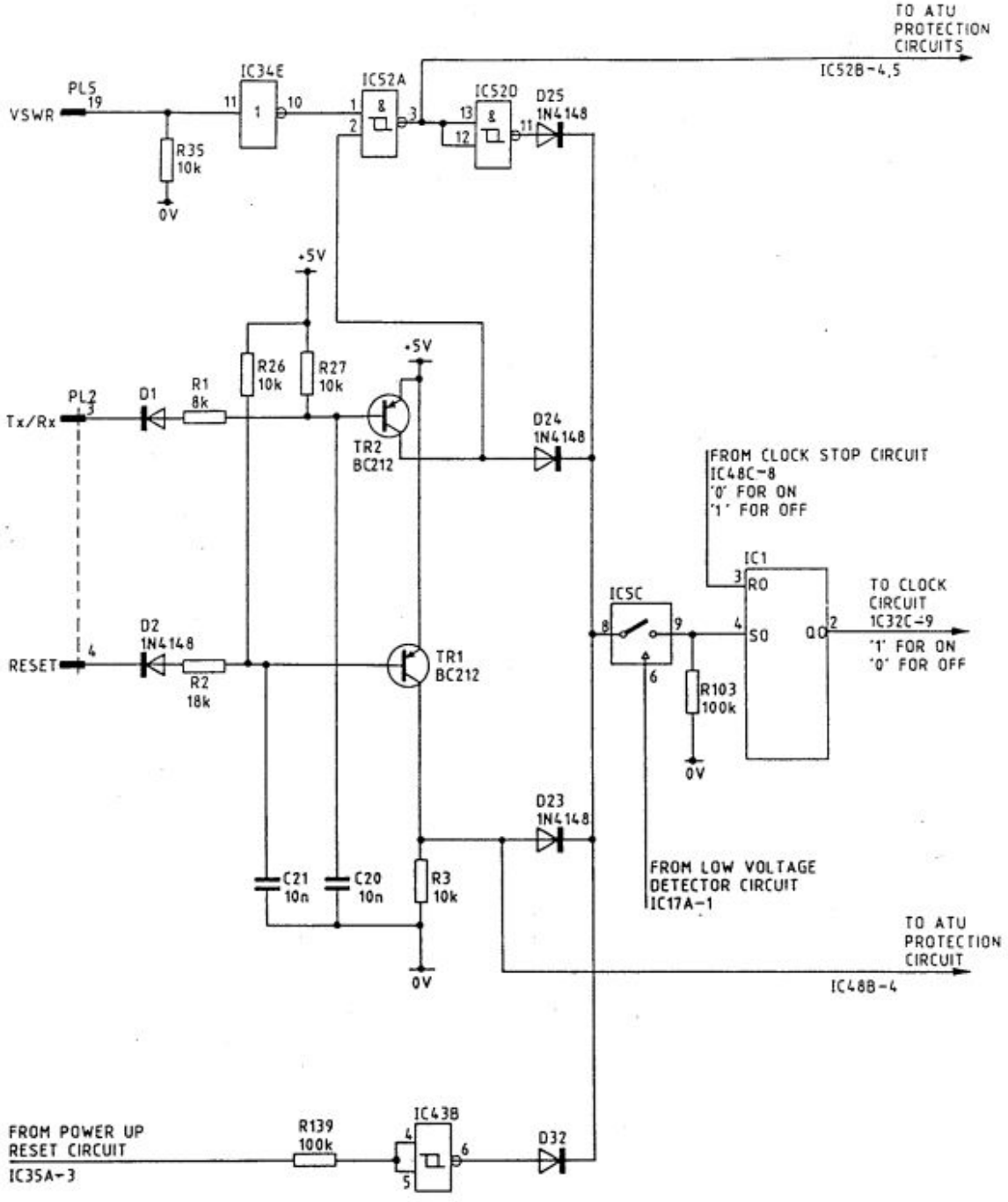

FIGURE 18 - CLOCK START CIRCUIT

Clock Stop Circuit (Figure 19, Figure 1004)

146. To reduce interference, the Microprocessor clock is switched off by the Microprocessor during the following conditions:

a. When no Microprocessor action is required.

b. During receive under normal and 2FS modes of operation.

c. When a system supply failure is detected.

147. The Clock Stop Circuit switches the Microprocessor clock off by sending a '1' to the RO input of IC1-3 (see clock start circuit description). With reference to Figure 19, IC8 and its associated components provide a '1' output at IC48C-8 for conditions a. and b. above; IC46 and its associated components generate a '1' output at IC48C-8 for condition c.

148. The operation of the two functional circuits (IC8 and IC46) is identical and therefore only the operation of IC8 and its associated components is described.

149. The Q2 output of the D-Type Latch IC8-6 is taken low ('0') by a low clocked through the latch from the data bus line D5. This low is differentiated by R49 and C60, and the resultant '0' inverted by the buffer IC18A and applied to the OR gate IC48C-9. The resultant '1' on IC48C-8 is passed via R125 to the clock start circuit to stop the clock oscillator.

150. When C60 has been charged above the CMOS threshold of 3.5 V by R49 and the +5 V supply, IC18A-3 becomes '0'. This is applied to the clock start circuit via IC48C, and enables the clock oscillator to be switched on, when required, by the clock start circuit. R125 provides current limit protection for the CMOS input to IC1 in the clock start circuit. Diode D8 prevents the input at IC18A-1,2 rising above 5 V when IC8-6 goes to a '1', i.e. 5 V at IC8-6 plus 5 V across C60.

151. The Output Enable (OE) of IC46-1 is active low and hard wired to 0 V. The output at IC46-5 is therefore always enabled and available to the Microprocessor for clock oscillator control. IC8 is prevented from stopping the clock oscillator during low voltage conditions, because its OE pin is connected to the Low Voltage Detector. This detector outputs a '1' during low voltage supply conditions.

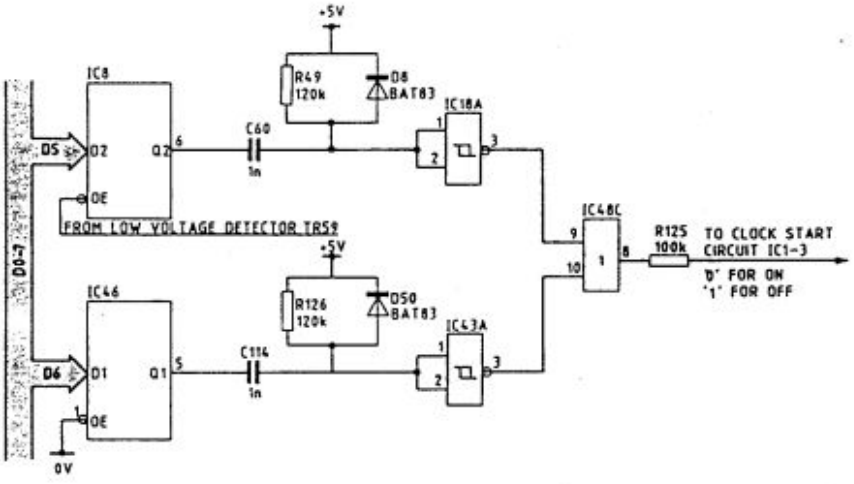

FIGURE 19 - CLOCK STOP CIRCUIT

RESET and Tx/Rx Input Circuits (Figure 20, Figure 1004)

152. An HF ATU tuning sequence is initiated by the Microprocessor upon receipt of a RESET pulse followed by the Tx/Rx line going active low (transmit mode). The circuit responsible for applying the RESET and Tx/Rx inputs to the Microprocessor IC24 is shown in Figure 20. The RESET and Tx/Rx inputs (TR1 and TR2 respectively) are described in the clock start circuit description.

153. With reference to Figures 20 and Figure 1004, an active low RESET pulse generates a '1' on TR1 collector which is applied to the S1 input of the RS latch IC1-6. This sets the latch and the Q1 output at IC1-9 becomes a '1'. This '1' is then applied to the input port IC25-22, the input being latched into the port by the application of the timing pulse TPB. Finally, the RESET is clocked onto the data bus by the Microprocessor setting its MRD (IC24-7) and N1 (IC24-18) lines to a '1'.

154. The active low Tx/Rx pulse generates a '1' on TR2 collector which is fed to IC25-20 and then clocked through onto D6 of the data bus by the same timing mechanism as the RESET pulse.

155. From the data bus, the RESET and Tx/Rx signals are read by the Microprocessor.

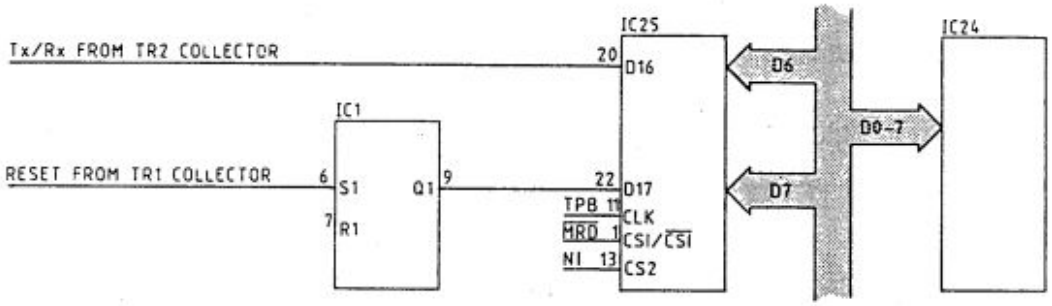

FIGURE 20 - RESET AND Tx/Rx INPUT CIRCUITS

Clear Reset Circuit (Figure 21, Figure 1004)

156. The internal architecture of the RS latch IC1 will hold its Q1 output at '1', masking any further RESET signals, until it is reset by a '1' applied to its R1 input. The circuit shown in Figure 21 issues a reset pulse to IC1-7 which will take the Q1 output at IC1-9 to '0'. This clears the RESET input to the Microprocessor made via input port IC25.

157. The Q5 output of IC8-15 is taken low ('0') by a low clocked through the D-Type Latch from the data bus line D2. This low is differentiated by R17 and C6 and the resultant '0' inverted by the buffer IC18C and applied to IC1-7, resetting the RS latch. When C6 has been charged above the CMOS threshold of 3.5 V by R17 and the +5 V supply, IC18C-8 becomes '0'. This allows the RS latch to be set by the next application of a RESET pulse.

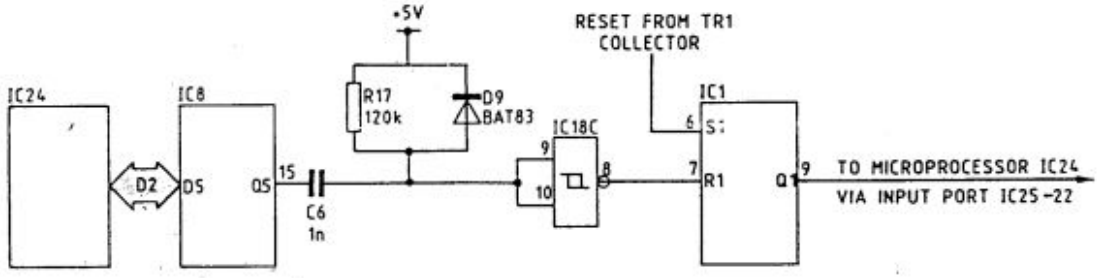

FIGURE 21 - CLEAR RESET CIRCUIT

Control Flag Selection Multiplexer Circuit (Figure 22, Figure 23, Figure 1004)

158. During the execution of the HF ATU program, control information is required by the Microprocessor on modes of operation and fault status. This information, listed in Table 8, is made available on the six input lines to the flag selection multiplexer IC37.

TABLE 8 - MULTIPLEXER FLAG INPUTS

INPUT	FUNCTION
TEST INPUT 1	This input is held active low by 4PL2 on Module 4. In this state the Microprocessor is in the normal mode of operation. When 4PL2 is removed the ROM and RAM self-test is initiated.
VSWR	An active low input flags the presence of a fault on the VSWR line.
WINDOW COMPARATOR	An active low input flags that the RF power is outside the 1 - 7 W limits, or that the antenna dc resistance to ground is less than 75 Ohms.
TEST INPUT 2	Not used.
2FS	An active low 2FS input flags the Microprocessor that the HF R/T is in the 2FS mode.
STARTING DISTURBANCE	Indicates if a system supply failure has lasted longer than 1 second. Longer than 1 second = '0'; less than 1 second = '1'.

159. As shown in the functional diagram Figure 22, the control information is grouped into two sets of three, the required group being selected by a logic '1' or '0' on the A, B and C control inputs. The output from the multiplexer is taken to the Microprocessor flag inputs EF1, EF2 and EF3.

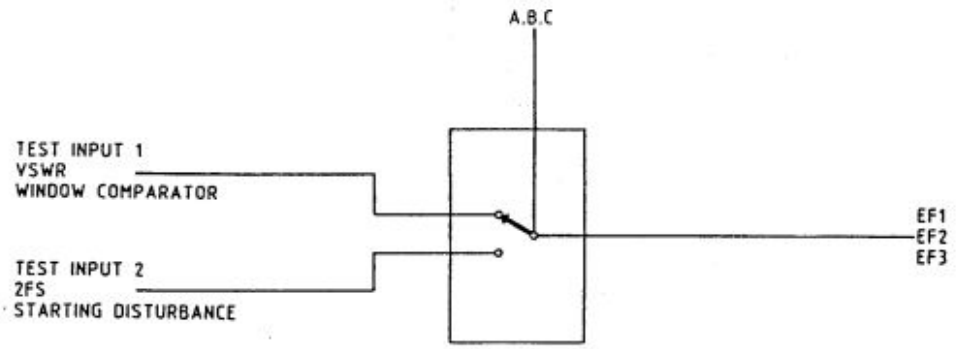

FIGURE 22 - MULTIPLEXER FUNCTIONAL DIAGRAM

160. The control inputs A, B and C on IC37-11, 10 and 9 are wired together and activated by a '1' or '0' placed on the Data Bus line D7. This signal is clocked through the D-Type Latch IC9, and then buffered and inverted by IC18B and applied to IC37.

161. Depending on the logic level applied to the control inputs, the required group is selected and fed to the output pins IC37-14, 15 and 4. This information is now available to the Microprocessor IC24 for program interpretation on EF1, EF2 and EF3.

162. When the A, B and C control inputs are at a '0', the TEST INPUT 1, VSWR and WINDOW COMPARATOR inputs are output on EF1, EF2 and EF3 respectively; when A, B and C are at '1', TEST INPUT 2, 2FS and STARTING DISTURBANCE are output on EF1, EF2 and EF3 respectively.

163. With reference to Figure 23, TR3 and its associated components convert the 2FS current sink signal into CMOS format before input to IC37. A low on PL2-6 forward biases D3 and current flows through R30 and R29. TR3 is now turned on by the drop in voltage at its base and TR3 collector goes high. This applies a '1' to IC37-2. D3 protects the circuits from any high external voltages which may be applied to the input.

164. R98 (TEST INPUT 2)and R34 (TEST INPUT 1) are +5 V pull up resistors and R35 (VSWR), R36 (WINDOW COMPARATOR) and R33 (2FS) are 0 V pull down resistors.

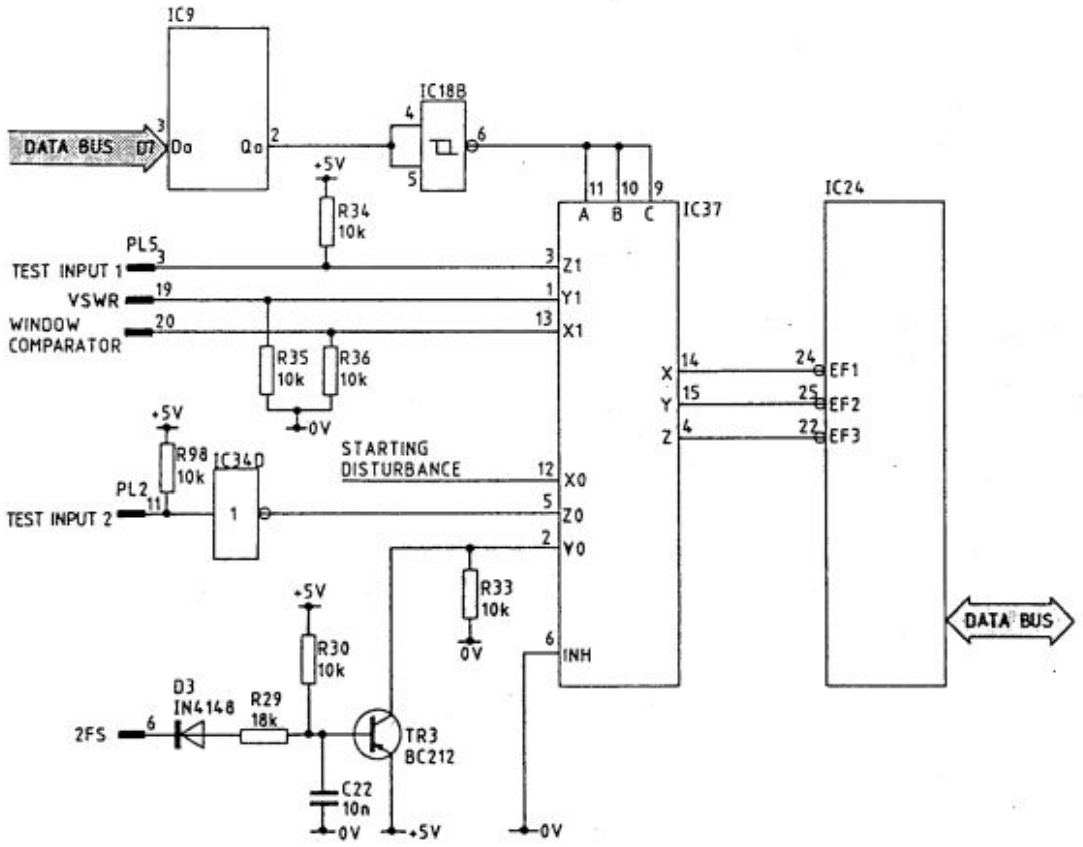

FIGURE 23 - CONTROL MULTIPLEXER CIRCUIT

Frequency Counter Circuit (Figure 24, Figure 1004)

165. The Frequency Counter Circuit is used to calculate the frequency of the HF R/T carrier transmission. On the basis of this calculation, the initial HF ATU's line shortening capacitance, broad band capacitance and series inductors are selected by the Microprocessor and inserted into the RF output path.

166. The Frequency Counter operates for a 16 Microsecond period over the frequency range 1.5 to 30 MHz. Frequency determination is in 500 kHz steps, resulting in one or more of the binary outputs of the frequency Counter Circuit changing for a frequency change of 500 kHz or more.

167. If 3PL2-2 FAULT has not been set after the completion of the antenna dc resistance and power detector checks (no fault condition), the switched +5 V (SWD) and +10 V (SWD) regulators are enabled. This applies +5 V to the binary counter IC3 and the RF input Schmitt triggers IC2C and IC2D. The resultant circuit actions detailed in the following paragraphs are initiated by the firmware program under Microprocessor control.

168. The D-type output latch IC8 outputs the following logic levels:

a. A '0' on IC8-9 (Q3); this is applied to the binary counter IC3-13 (CLR) to inhibit IC3 count. When the '0' is removed, the 16 Microsecond count period is initiated.

b. A '0' on IC8-15 (Q5); this is applied to the reset pin of the 12-bit binary counter IC19-11 via the buffer IC18D. This sets IC19's Q outputs to '0'.

c. A '1' on IC8-2 (Q0); this turns on the darlington transistor TR6 which takes 3PL5-13 towards 0 V. This energises RLB in Module 4 which applies the RF input from the HF R/T to the counter input circuit IC2C-10 via RF COUNTER 3PL5-2.

169. The RF input is connected to IC3-8 via the Schmitt triggers IC2C and IC2D which are enabled by the +5V (SWD) regulator supply. These devices convert the RF input into a square wave signal required to drive IC3 CLK1 input. R18 and R19 set the bias on IC2C to the mid-point of its operating range to give a 1:1 mark space ratio for the RF input. C7 provides a dc block and C8 is a decoupling capacitor.

170. With IC3-5 (QA) connected to IC3-6 (CLK2), the counter behaves as a divide by sixteen circuit, one pulse being produced at IC3-12 (QD) for every sixteen pulses applied to CLK1. The QD output is taken via the level changer TR4 to the CLK input of IC19-10. TR4 is required to interface the QD output of the TTL device IC3 with the CLK input of the CMOS device IC19.

171. IC19 acts as a conventional ripple binary counter, with a 6-bit parallel output produced at Q0 to Q5. As an example of the circuit action, an RF input at 3PL5-2 of 2 MHz will input 32 cycles to IC3-8 (CLK1) over the 16 Microsecond period. The divide by sixteen counter IC3 will therefore output two clock pulses to IC19-10, leaving IC19's Q outputs with the following binary values:

$$Q0 = 0, Q1 = 1, Q2 = 0, Q3 = 0, Q4 = 0, Q5 = 0$$

172. After 16 Microseconds, IC8-2,9 are taken low and RLB in Module 4 is de-energised, thus removing the RF input to the frequency counter circuit. The 6-bit parallel output from IC19 is latched into the input port IC25 by the application of the TPB timing pulse from the Microprocessor. When the Microprocessor requires to read the latched data, MRD and the device selection line N1 are taken high and the frequency count is placed on the data bus.

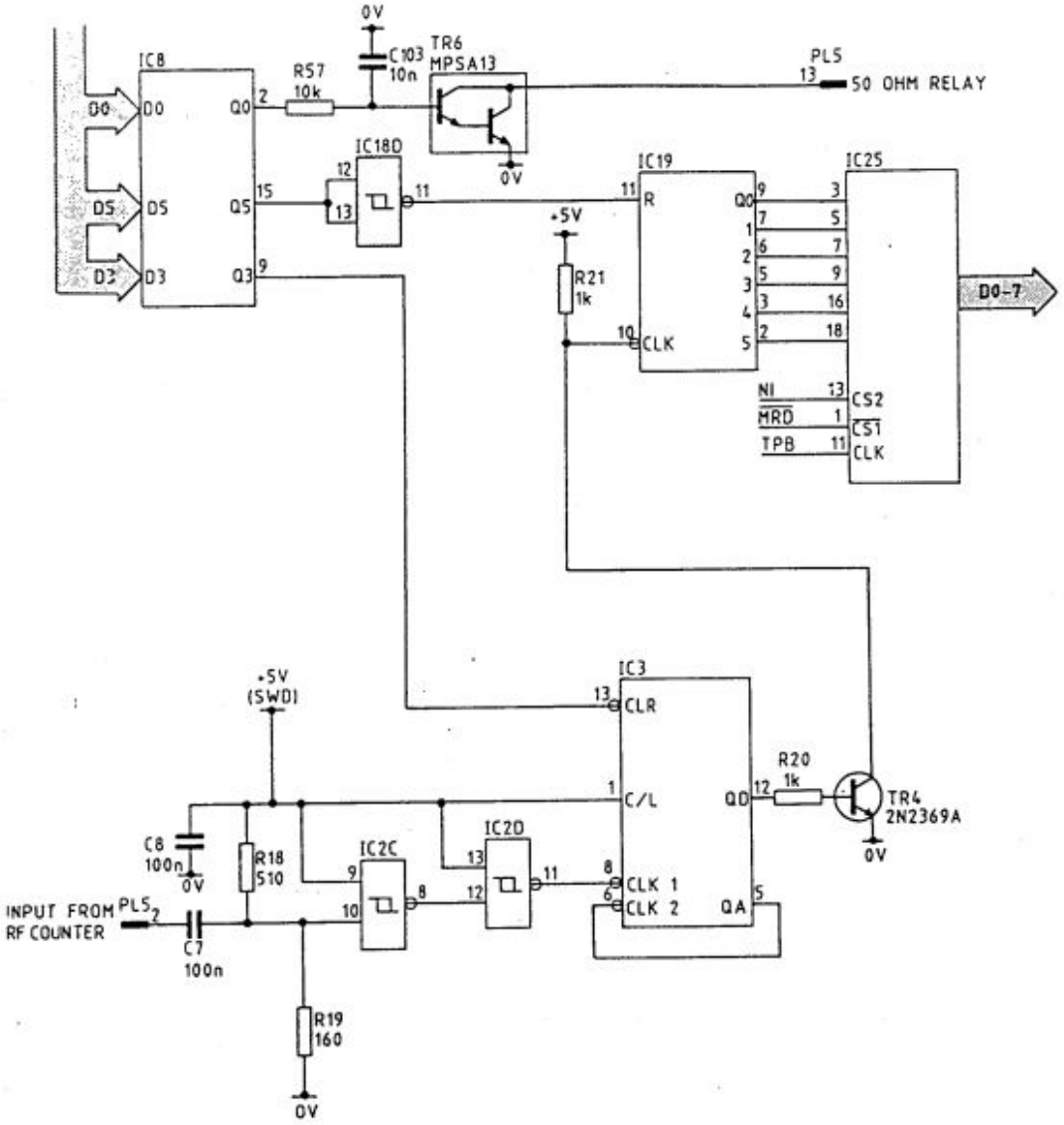

FIGURE 24 - FREQUENCY COUNTER CIRCUIT

Analogue to Digital Converter Circuits (Figure 25, Figure 1004)

173. The Analogue to Digital (A to D) Converter Circuit shown in Figure 25 converts the analogue conductance or phase detector dc outputs from Module 4 into a digital value suitable for input to the Microprocessor. This is required during the HF ATU's component selection process to enable the Microprocessor software to select components and determine when the unit is correctly tuned.

174. In principle, the circuit operates by comparing the Analogue Phase or Conductance dc input with a dc reference voltage. To tune the unit, the Microprocessor introduces or removes tuning components until the analogue input from both comparators is 2.5 V, indicating the unit is correctly tuned. This is represented digitally as an equal number of '1's and '0's in the resultant binary word.

175. The analogue input is determined by the action of the DETECTOR SELECT line which is under program control. A '1' on this line will close IC5B to select the ANALOGUE COND input from PL5-17; a '0' will be inverted by IC52C and the resultant '1' will close IC5A to select the ANALOGUE PHASE input from PL5-18. R137 and R138 are current limiters.

176. The binary outputs to the Microprocessor, via input port IC26, are obtained from the eight comparators contained in IC6 and IC7, all of which share a common non-inverting input. The inverting inputs are connected to points on a potentiometer chain consisting of R55, the resistors in IC36 and R56. With a '0' on the A/D RESOLUTION SELECT line, R55 and R56 are shorted out by IC20A and IC20C, and the +5 V (SWD) connected across the eight resistors making up IC36.

177. The eight comparators receive dc reference inputs incremented in 0.625 mV steps with a mid-point of 2.5 V. The DETECTOR OFFSET voltage is obtained from this mid-point via the switch IC20D and the buffer amplifier IC4A. R140 and C115 provide decoupling. This voltage is used in Module 4 to set the reference level at which the 'crossover' points of the phase and conductance detection occur.

178. Application of an analogue input voltage of between 0 V and 5 V to the comparator's non-inverting terminals sets to '1' the output of those comparators which have a reference level lower than that of the applied analogue input. An example of the output obtained is shown in Table 9. In this example, R55 and R56 are shorted out.

TABLE 9 - EXAMPLE OF COMPARATOR COARSE DETERMINATION

	IC7 PIN				IC6 PIN			
ANALOGUE INPUT	14	13	2	1	14	13	2	1
Greater than 0.625 V	1	0	0	0	0	0	0	0
Greater than 1.250 V	1	1	0	0	0	0	0	0
Greater than 1.875 V	1	1	1	0	0	0	0	0
Greater than 2.500 V	1	1	1	1	0	0	0	0
Greater than 3.125 V	1	1	1	1	1	0	0	0
Greater than 3.750 V	1	1	1	1	1	1	0	0
Greater than 4.375 V	1	1	1	1	1	1	1	0
Greater than 5.000 V	1	1	1	1	1	1	1	1

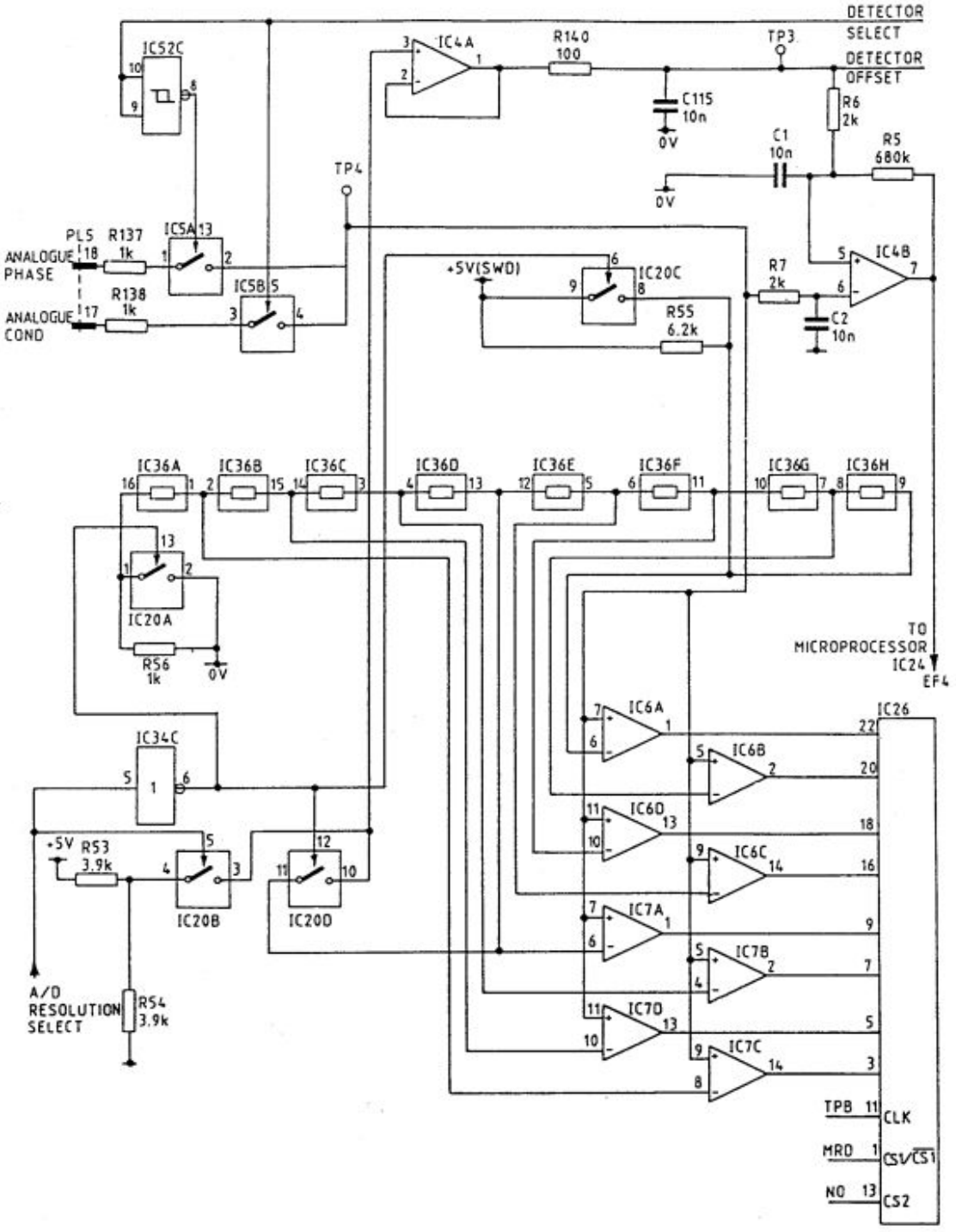

FIGURE 25 - ANALOGUE TO DIGITAL CONVERTER CIRCUIT

179. Table 9 illustrates a coarse determination of the phase or conductance analogue input, with the input ranging from 0.625 V up to 5.000 V. After each step, the program introduces or removes components to achieve an equal number of '1's and '0's at the comparator's outputs, indicating an analogue input of 2.5 V.

180. As shown in Table 9, it is possible to generate an equal number of '1's and '0's with an analogue input of between 2.500 V and 3.125 V. When tuning to frequencies less than 3 MHz, closer definition is required because of the change in impedance presented by the network components below this frequency. This is achieved by the Microprocessor placing a '1' on the A/D RESOLUTION SELECT line. This is inverted by IC34C and the resultant '0' opens IC20A and IC20C. R55 and R56 are now placed in the potentiometer chain, with a consequent change in the stepped dc reference voltage levels.

181. The voltage steps shown in Table 10 are now 123 mV instead of 625 mV, with a lowest point of 681 mV. Under these conditions, the levels determined by coarse adjustment are fine tuned and components switched in accordingly.

TABLE 10 - EXAMPLE OF COMPARATOR FINE DETERMINATION

	IC7 PIN				IC6 PIN			
	14	13	2	1	14	13	2	1
ANALOGUE INPUTS								
Greater than 0.681 V	1	0	0	0	0	0	0	0
Greater than 0.804 V	1	1	0	0	0	0	0	0
Greater than 0.927 V	1	1	1	0	0	0	0	0
Greater than 1.050 V	1	1	1	1	0	0	0	0
Greater than 1.170 V	1	1	1	1	1	0	0	0
Greater than 1.293 V	1	1	1	1	1	1	0	0
Greater than 1.416 V	1	1	1	1	1	1	1	0
Greater than 1.539 V	1	1	1	1	1	1	1	1

182. The mid-point has now changed to 1.050 V and is unsuitable for use as the DETECTOR OFFSET crossover voltage. The '1' on the A/D RESOLUTION SELECT line therefore opens IC20D and closes IC20B, bringing the voltage divider R53 and R54 into circuit. The resultant +2.5 V is applied to the DETECTOR OFFSET line via the buffer IC4A.

183. The output of the comparators is clocked into the 8 Bit I/O Port IC26 by the Microprocessor timing pulse TPB. The data is read from the port onto the data bus by the Microprocessor placing a '1' on the device selection line N0 and MRD.

provided by the voltage comparator IC4B which has a 2.5 V reference voltage applied to pin 5 via the DETECTOR OFFSET line and the selected analogue input applied to pin 6.

185. The output at IC4B-7 is applied to the Microprocessor IC24-21 (EF4), and depending on the level of the DETECTOR SELECT line, the logic level on EF4 can be interpreted as shown in Table 11.

TABLE 11 - INTERPRETATION OF EF4 ABOVE 5 MHZ

	DETECTOR SELECT AT '0' (ANALOGUE PHASE INPUT)	DETECTOR SELECT AT '1' (ANALOGUE COND INPUT)
EF4 OUTPUT	'0' = Capacitive	'0' = Inside Conductance Circle (less than 20 m Siemens)
	'1' = Inductive	'1' = Outside Conductance Circle (greater than 20 m Siemens)

D-Type Latches (Figure 1004)

186. Interfacing between the Microprocessor's data bus and the external modules is provided by the tri-state D-Type Latch output ports IC8 to IC12. These latches allow expansion of the data bus and also isolate the bus (and therefore the Microprocessor) from any interference caused by the driven external module circuits.

187. The logic levels on all D inputs will be transferred to the Q outputs when a '0' is applied to the Latch Enable (LE) pin 11. If LE is a '1' then the input and output are isolated from each other. When the Output Enable (OE) is at '1', the Q outputs become a high impedance and the action of the latch is suspended until OE is taken to a '0'.

Output D-Type Latch Decoder Circuit. (Figure 26, Figure 1004)

188. When data is placed on the data bus, it is available to all D-Type Latches simultaneously. Therefore, in order to select a particular latch, each latch must be individually addressable. The output latches on the Microprocessor module are used to drive system control signals and component selection relays. A latch address allows individual relays to be driven under Microprocessor control, resulting in single component insertion.

189. Addressing of the five output latches is carried out by the Microprocessor IC24 placing a 3-bit BCD device selection code on its N0, N1 and N2 outputs. This 3-bit code is decoded by the BCD to decimal decoder IC27, clocked through a three input AND gate by timing pulses and applied to the LE input of the required latch. The truth table of the BCD to Decimal decoder is shown in Table 12. The D input is wired to 0 V and therefore has no effect on the truth table and is not included.

TABLE 12 - BCD TO DECIMAL TRUTH TABLE

INPUTS			OUTPUTS							
A	B	C	Q0	Q1	Q2	Q3	Q4	Q5	Q6	Q7
0	0	0	0	1	1	1	1	1	1	1
0	0	1	1	0	1	1	1	1	1	1
0	1	0	1	1	0	1	1	1	1	1
0	1	1	1	1	1	0	1	1	1	1
1	0	0	1	1	1	1	0	1	1	1
1	0	1	1	1	1	1	1	0	1	1
1	1	0	1	1	1	1	1	1	0	1
1	1	1	1	1	1	1	1	1	1	0

190. As an example from Table 12 with A = 1, B = 0 and C = 0, the Q4 output is taken to '0'. This is then clocked through IC30B and IC11 is enabled.

191. The latch selection code is output on IC24-19,18 and 17 and applied to the A, B and C inputs of IC27-10, 13 and 12 respectively. Depending on the code, a '0' is output on one of the Q outputs (Q1 to Q6) and passed to one of the three-input AND gates IC31 or IC30.

192. The '0' is clocked through the selected AND gate by the simultaneous application of the timing pulse TPB and memory read command MRD. The resultant '0' output is then passed to the required output latch pin 11. The MRD Pulse generated by IC24 is a '0' and is therefore inverted by IC35D to provide a '1' at IC30 and IC31.

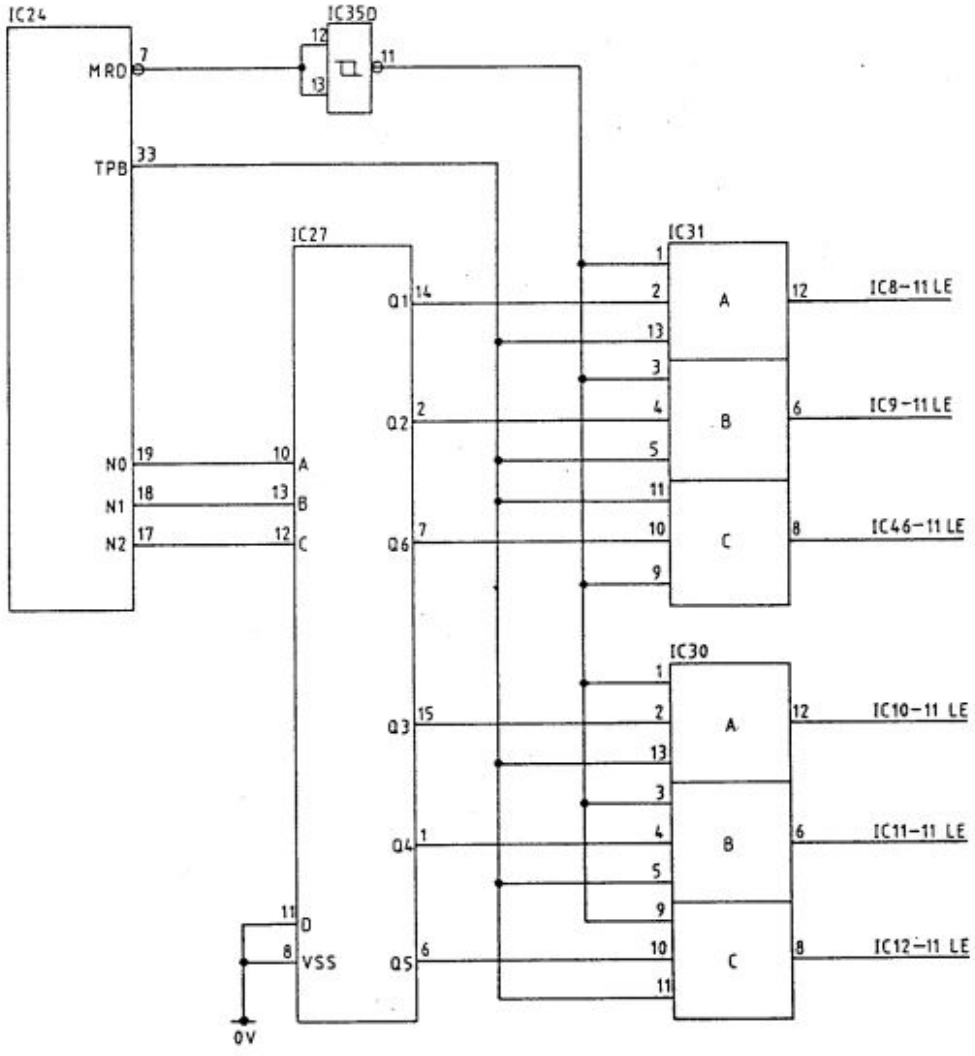

FIGURE 26 - OUTPUT D-TYPE LATCH DECODER CIRCUIT

Output Port Signals (Figure 1004)

193. The D-Type Latches IC8 to IC12 and the reset latch IC46 are used under Microprocessor control to enable the following:

a. The switching of internal control signals.

b. The driver circuits for the HF ATU system control signals.

c. The driver circuits for the component selection relays.

194. The functions of the Q logic outputs of each latch are shown in Table 13.

TABLE 13 - D TYPE LATCH Q OUTPUT FUNCTIONS

			IC8				
Q0	Q1	Q2	Q3	Q4	Q5	Q6	Q7
50 R RELAY 0 = Out 1 = In	Cond/Phase 0 = Phase 1 = Cond	Clock Cntrl 0 = Reset 1 = On	Freq Count 0 = CLR 1 = Enable	PSU CONTROL 0 = Off 1 = On	Clear RESET 0 = Clear 1 = On	READY 0 = No 1 = Yes	FAULT 0 = No 1 = Yes
			IC9				
Q0	Q1	Q2	Q3	Q4	Q5	Q6	Q7
FLAG SELECT 0 = Norm 1 = Alt	BITE LED 0 = Off 1 = On	Not Used	DET RELAY 0 = In 1 = Out	L10 0 = In 1 = Out	L11 0 = In 1 = Out	L12 0 = In 1 = Out	L13 0 = In 1 = Out
			IC10				
Q0	Q1	Q2	Q3	Q4	Q5	Q6	Q7
A/D RES SEL 0 = High 1 = Low	C3 0 = Out 1 = In	C4 0 = Out 1 = In	C5 0 = Out 1 = In	C6 0 = Out 1 = In	C7 0 = Out 1 = In	C8 0 = Out 1 = In	C9 0 = Out 1 = In
			IC11				
Q0	Q1	Q2	Q3	Q4	Q5	Q6	Q7
LSC1 0 = In 1 = Out	LSC2 0 = In 1 = Out	L6 0 = in 1 = Out	L7 0 = In 1 = Out	L8 0 = In 1 = Out	L9 0 = In 1 = Out	C1 0 = Out 1 = In	C2 0 = Out 1 = In
			IC12				
Q0	Q1	Q2	Q3	Q4	Q5	Q6	Q7
BBC2 0 = In 1 = Out	BBC1 0 = In 1 = Out	L5 0 = Out 1 = In	L4 0 = In 1 = Out	L3 0 = In 1 = Out	L2/L4 See Para 304	L2/L1 See Para 304	L1 0 = Out 1 = In
			IC46				
Q0	Q1	Q2	Q3	Q4	Q5	Q6	Q7
RAM Select 0 = Reset 1 = Set	Clock Cntrl 0 = Disable 1 = Enable	Not Used	Not Used	Not Used	Not Used	Not Used	Not Used

Input Port Signals (Figure 1004)

195. The Input Ports IC25 and IC26 are used to take the outputs of the A to D converter and frequency counter circuits and place them on the data bus under Microprocessor control. Table 14 gives the function of the input port's 'DI' pins.

TABLE 14 - INPUT PORT PIN FUNCTIONS

IC25							
DI0 Frequency Counter Bit 0	DI1 Frequency Counter Bit 1	DI2 Frequency Counter Bit 2	DI3 Frequency Counter Bit 3	DI4 Frequency Counter Bit 4	DI5 Frequency Counter Bit 5	DI6 Tx/Rx 0 = Rx 1 = Tx	DI7 RESET 0 = Normal 1 = RESET
IC26							
DI0 Output A/D Converter Bit 0	DI1 Output A/D Converter Bit 1	DI2 Output A/D Converter Bit 2	DI3 Output A/D Converter Bit 3	DI4 Output A/D Converter Bit 4	DI5 Output A/D Converter Bit 5	DI6 Output A/D Converter Bit 6	D17 Output A/D Converter Bit 7

D-Type Latch Output Driver Circuits

196. To provide the necessary current drive, the outputs of the D-Type Latches IC8 - IC12 and IC46 are passed to three types of driver circuits, the type of circuit used reflecting the current requirement of the next stage. An example of each of the three driver types is given in the following sub-paragraphs.

System Control Signal Driver Circuit. (Figure 27, Figure 1004)

197. The System Control Signal Driver circuits identify TR7 with TR8 and TR9, TR10 with TR11 and TR12, and TR13 with TR14 and TR15. With reference to Figure 27, this circuit description explains the operation of TR13, TR14, TR15 and their associated components.

198. A '1' applied to TR13 base via the decoupling components R52 and C102 will turn TR13 on. This causes a drop in the voltage on TR13 collector which reverse biases the base emitter junction of TR15, turning it off. This sets the FAULT output at PL2-2 high, indicating a fault to the HF R/T. The FAULT output at TR15 collector is decoupled by C106.

199. The driver circuits for the system control signals are designed to withstand 30 V being applied across their output pins with the output transistor turned on. A '0' applied to TR13 base will turn the transistor off, allowing its collector to go high and turning on TR15. The resultant voltage drop across R41 caused by TR15 emitter current will turn TR14 on, reducing the forward bias to TR15. The circuit action is therefore a non-saturating switch with a stabilizing point determined by the value of R41.

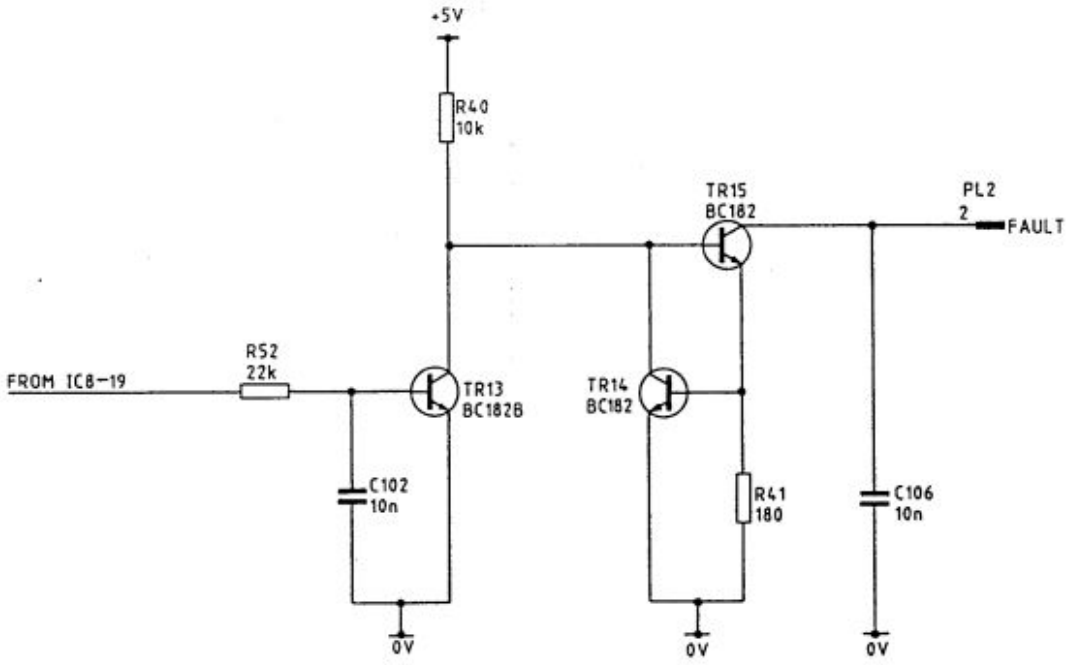

FIGURE 27 - SYSTEM CONTROL SIGNAL DRIVER CIRCUIT

High Current Driver Circuits. (Figure 28, Figure 1004)

200. The High Current Driver Circuits provide a high drive current to operate the component selection relays on Module 6. These circuits identify TR41 with TR46, TR42 with TR47, TR43 with TR48, TR44 with TR49 and TR45 with TR50. With reference to Figure 28, this circuit description describes the operation of TR45, TR50 and their associated components.

201. The action of the circuit is identical to the system control signal driver circuit, without the control transistor TR14. The high drive current is provided by the large current transistors TR45 and TR50. D15 is a relay coil diode designed to prevent induced voltages from building up to a high value when the relay is switched off; D15 is across RLH which is mounted on Module 6.

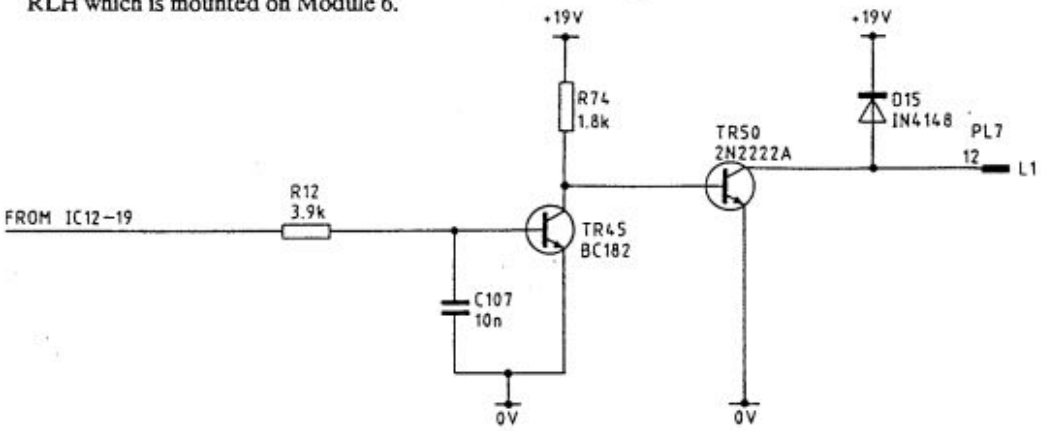

FIGURE 28 - HIGH CURRENT DRIVER CIRCUITS

Darlington Pair Drive Circuit. (Figure 29, Figure 1004)

202. The Darlington Pair Drive Circuits identify TR5, TR6, TR18, TR19 and TR23 to TR40. With reference to Figure 29, this circuit description describes the operation of TR6 and its associated components.

203. TR6 is turned on by a '1' applied via the decoupling components R57 and C103. With reference to Figure 29, TR(w) acts as a common collector amplifier. In operation, an increase in TR(w) base current is followed by an increase in base current to TR(x). Because the emitter current of TR(w) is nearly equal to its collector current, a large current amplification takes place. The overall current gain is practically equal to the product of the individual transistor current gains.

204. The Darlington Pair Drive Circuits used with IC11 (TR30 - TR37) utilise a 33 Ohm current limiting resistor between the transistor collectors and the Module's output connectors.

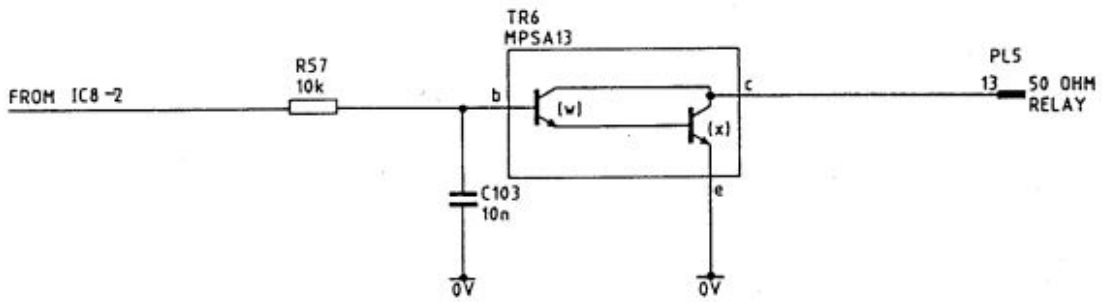

FIGURE 29 - DARLINGTON PAIR DRIVE CIRCUIT

Low Voltage Detector Circuit (Figure 30, Figure 1004)

205. The Low Voltage Detector Circuit enables the Microprocessor module to initiate an orderly close down procedure if the system supply drops below 19.5 V. With reference to Figure 30, the operational amplifier IC17A acts as a voltage comparator by comparing the voltage on IC17A-3 with the voltage on IC17A-2. The voltage on IC17A-3 is derived from the +19 V regulator supply via the potential divider R61, R62 and R63. The voltage on IC17A-2 is derived from the +12 V regulated supply via R64. The +12 V supply is generated on Module 3 and is derived from the +19 V supply.

206. When the system supply is greater than +19.5 V, the voltage at IC17A-3 will be greater than the voltage IC17A-2 and the comparator output on IC17A-1 will be a '1'. If the system supply falls below +19.5 V, the +19 V regulator output will drop below 17.5 V, causing the voltage inputs to IC17A to become equal and the output at IC17A-1 to become '0'. R65 provides positive feedback to give rapid switching and R82 provides current limit protection.

207. A '0' output at IC17A-1 has the following effects:

a. ATU PROT 1 is taken high (see ATU PROT 1 circuit description).

b. ATU PROT 2 is taken high (see ATU PROT 2 circuit description).

c. The 8-bit RAM chip IC21 is disabled and the Microprocessor clock is stopped (see ATU protection circuit description).

d. The clock start circuit is disabled (see clock start circuit description).

e. The D-Type Latch output ports (IC8 - IC12, IC46) are tri-stated. A tri-state logic device is a device whose output can be in one of three states: a logical '0' with a low impedance path to ground; a logical '1' with a low impedance path to the positive supply rail; and a high impedance state in which the output is effectively floating and has no effect on the bus lines

f. The Microprocessor (IC24-3) CLR is set to '0' by the power-up reset circuit (see Power-up Reset Circuit description).

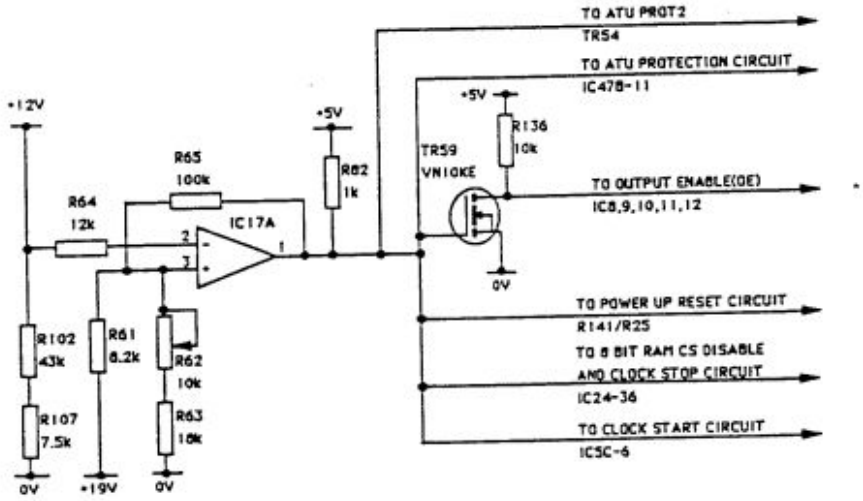

FIGURE 30 - LOW VOLTAGE DETECTOR CIRCUIT

D-Type Output Enable (OE). (Figure 30, Figure 1004)

208. The voltage controlled JUGFET TR59 is turned off by the '0' applied to its gate from IC17A-1 via R82. The '0' at TR59 gate takes the drain towards +5 V by R136, resulting in the OE of the D-Type Latches being taken high. Hence, IC8, IC9, IC10, IC11 and IC12 are tri-stated, preventing any component selection relays from being driven and therefore connecting the bypass route through the equipment.

8-Bit Ram Chip Disable and Clock Stop Circuit. (Figure 31)

209. A '0' applied to IC24-36 (INT) from IC17A-1 causes the microprocessor to output a '0' on the Data Bus lines D6 and D7. The D6 and D7 outputs are passed through the D-Type Latch IC46 onto the Q1 and Q0 outputs of IC46, resulting in the following circuit actions:

a. The '0' output on IC46-2 (Q0) is applied to the gate of the MOSFET TR58. With a resultant reduction in the drain current, IC48A-2 is taken high through R58 and an inhibiting '1' is placed on the CS input to the 32 x 8-bit RAM IC21-15. This prevents inaccurate data being written to RAM during low voltage supply conditions.

b. The '0' output on IC46-5 (Q1) is applied to the clock stop circuit. The action of this circuit is described in the clock stop circuit description.

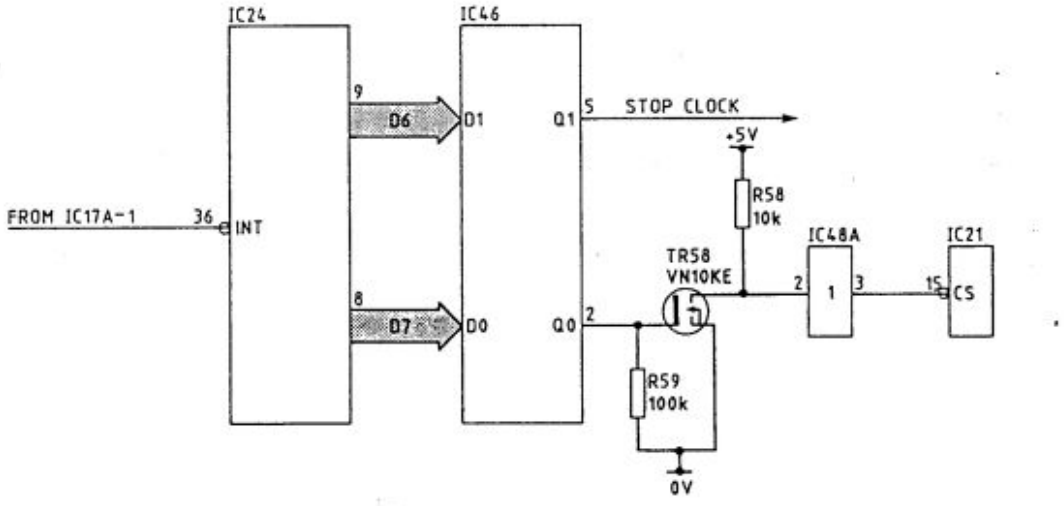

FIGURE 31 - 8-BIT RAM DISABLE AND CLOCK STOP CIRCUIT

Starting Disturbance Detector (Figure 32, Figure 1004)

210. A drop in the system supply caused by interference, e.g. vehicle starter motors, is usually short in duration and supply levels are quickly restored. The disturbance detector is designed to give an indication if the supply interruption has lasted for less than 1 second. This allows the Microprocessor to determine if the HF ATU requires retuning.

211. The starting disturbance detector is formed by the voltage comparator IC44B and its associated components, and the CR circuit consisting of R101, C14 and C15. The voltage inputs to IC44B are applied to IC44B-6 from the +12 V regulator supply and potential divider R102 and R107, and to IC44B-5 from the +5 V regulator, R104 and the buffer amplifier IC44A.

212. Under normal operating conditions, with the voltage on IC44B-5 greater than the voltage on IC44B-6, the output on IC44B-7 will be a '1'. When a supply interruption occurs, the +5 V regulator output drops and IC44B output remains a '1' for the length of time it takes C14 and C15 to discharge. This takes approximately 1 second. The output of the disturbance detector is fed via the current limiter R106 to the control input multiplexer (IC37-12) for evaluation by the Microprocessor.

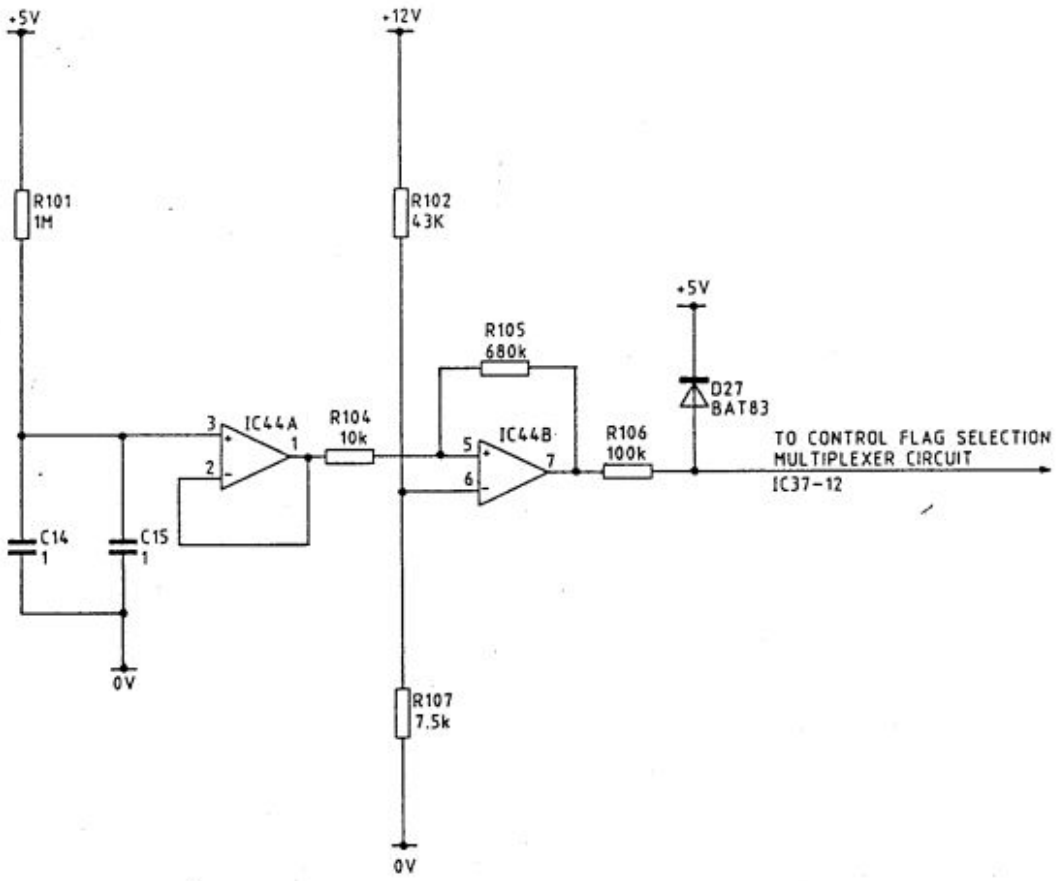

FIGURE 32 - STARTING DISTURBANCE DETECTOR CIRCUIT

ATU Protection Circuits (Figure 33, Figure 1004)

213. The ATU Protection Circuits provide the system ATU PROT 1 and ATU PROT 2 control logic signals which reduce the input power to the HF ATU under the following conditions:

a. The circulating currents at the bottom end of the matching network in Module 4 exceed 7 Amps.

b. The temperature on the chassis exceeds 100 deg C.

c. The VSWR is greater than 3:1.

d. The system supply drops below +19.5 V.

214. With reference to the logic diagram shown in Figure 33, a '1' on any of the four inputs to the OR gate IC47B will set ATU PROT 1 active high. As shown in Figure 30, a '1' from the Low Voltage Detector Circuit will also set ATU PROT 2 active high. If, after 2 seconds of ATU PROT 1 being operated by the Current Sensing Circuit, no reduction in the circulating currents are detected, ATU PROT 2 is set active high and ATU PROT 1 set low. If, after a further 2 seconds, the circulating currents are still too high, ATU PROT 2 and ATU PROT 1 are both set active high.

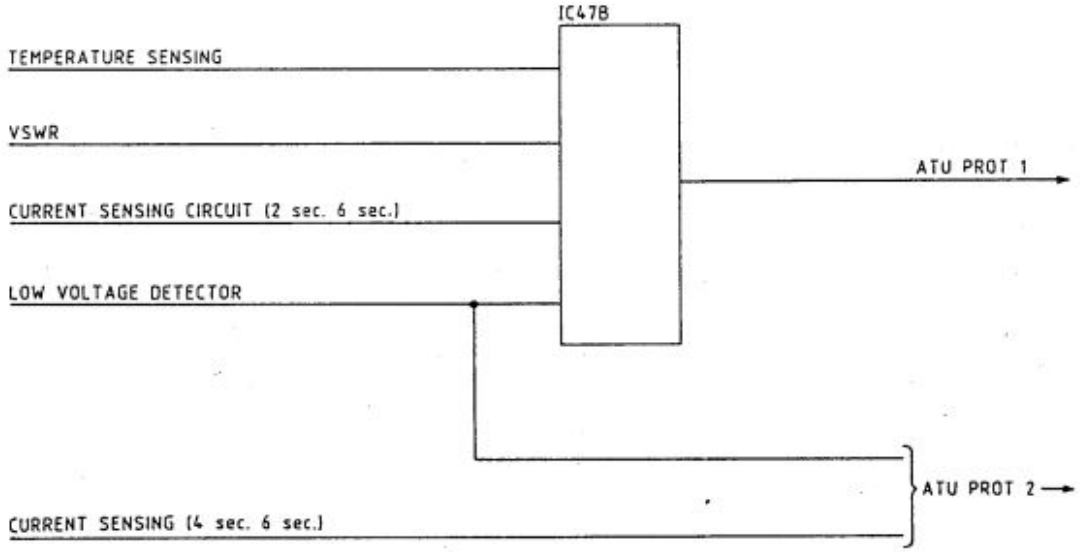

FIGURE 33 - ATU PROT 1/ATU PROT 2 LOGIC DIAGRAM

Temperature Sensing Input Circuit. (Figure 34, Figure 1004)

215. Temperature Sensing is achieved by bi-metallic strip sensors placed on the chassis, these indicate when the temperature in the equipment has risen above 100 deg C. The sensors operate above 100 deg C and remove 0 V from PL3-2 (TEMP1). Removal of the 0 V at PL3-2 takes the input high through R84 being connected to 19 V. This is clamped to +5 V by D19 and passed as a '1' to IC47B-9, resulting in ATU PROT 1 being set active high.

216. When the temperature has dropped below 100 deg C, the TEMP 1 input to PL3-2 is restored to 0 V and the ATU PROT 1 is set low.

VSWR Input Circuit. (Figure 34, Figure 1004)

217. An active low signal from the VSWR detector circuit on Module 4 at PL5-19 (VSWR greater than 3:1) will cause a '0' on IC52B-4,5 via IC34E and IC52A. The resultant '1' on IC52B-6 is applied to the OR gate IC47B-12 and ATU PROT 1 is set active high. R120 and C56 decouple the input to IC52-B.

Low Volts Detector Input Circuit. (Figure 34, Figure 1004)

218. When the system supply drops below 19.5 V, a '0' from the Low Voltage Detector IC17A-1 is applied to IC34C-13 where it is inverted to apply a '1' to the OR gate IC47B-11. This results in ATU PROT 1 being set active high.

Current Sensing Circuit. (Figure 34, Figure 1004)

219. The Current Sensing Circuit utilises a 12-bit binary counter (IC45) to introduce time delays associated with power reductions caused by high circulating currents. The counter is clocked by a 500 Hz oscillator formed by IC33D, R89 and C34. The oscillator is enabled by a high CURRENT TRIP signal from the current sensing detectors in Module 4.

220. If the circulating currents in Module 4 exceed 7 Amps, the CURRENT TRIP input at PL5-22 is taken high. Any low frequencies present are removed by R97 and C32 and the line is clamped to 5 V by D16. The high at PL5-22 produces a '1' on IC33D-12, resulting in the oscillator being switched on.

221. The 500 Hz oscillator output is fed by the NAND gate IC32A to the clock input of the 12-bit binary counter IC45-10. When IC45 is reset by the Master Reset or Power Reset to IC48B, '0's are placed on the output lines of IC45 (Q0 to Q11). The '0's on Q10 and Q11 place a '1' on NAND gate IC32B-4 which is fed to IC32A-2 to gate the 500 Hz clock through to IC45-10.

222. If after 2 seconds, the circulating currents are still high, the Q10 output of IC45 will have been clocked by the 500 Hz oscillator to reach a '1'. This is fed to the OR gate IC47B-10, the resultant '1' at IC47B-13 taking ATU PROT 1 active high and therefore reducing the input power. With the Q10 output now at a '1' and Q11 at '0', the resultant '1' output of NAND gate IC32B-6 maintains a '1' at IC32A-2, so allowing the clock input to IC45-10.

223. If two more seconds elapse (four in total) and the clock is still enabled by the presence of excess currents, then Q11 will become '1' and ATU PROT 2 will become active high, further reducing the input power. At this time, Q10 will be '0' and therefore ATU PROT 1 will not be active high. With the Q10 output now at a '0' and Q11 at '1', the resultant '1' output of NAND gate IC32B-4 maintains a '1' at IC32A-2, so allowing the clock input to IC45.

224. If the circulating currents are still too high after a further two seconds (six in total), Q10 and Q11 will have '1's on their outputs. This sets ATU PROT 1 and ATU PROT 2 active high which forces the HF R/T's output power to 1.25 W. With the Q10 and Q11 outputs of IC45 now at '1', the resultant '0' output of NAND gate IC32B-4 disables the input at IC32A, thus preventing further clock inputs to IC45.

225. To ensure IC45 is reset to clear all Q outputs, reset pulses are generated when the system supply is first applied, and whenever a RESET pulse is generated by the HF R/T. Resets are applied to IC48B from the reset input circuit and the power on reset circuit. The output is taken from IC48B-6 to IC45-11 (R) via the current limiting resistor R87.

226. Normal operating conditions may only be restored by a system RESET pulse and the subsequent re-tune sequence when the circulating currents have dropped below 7 Amps.

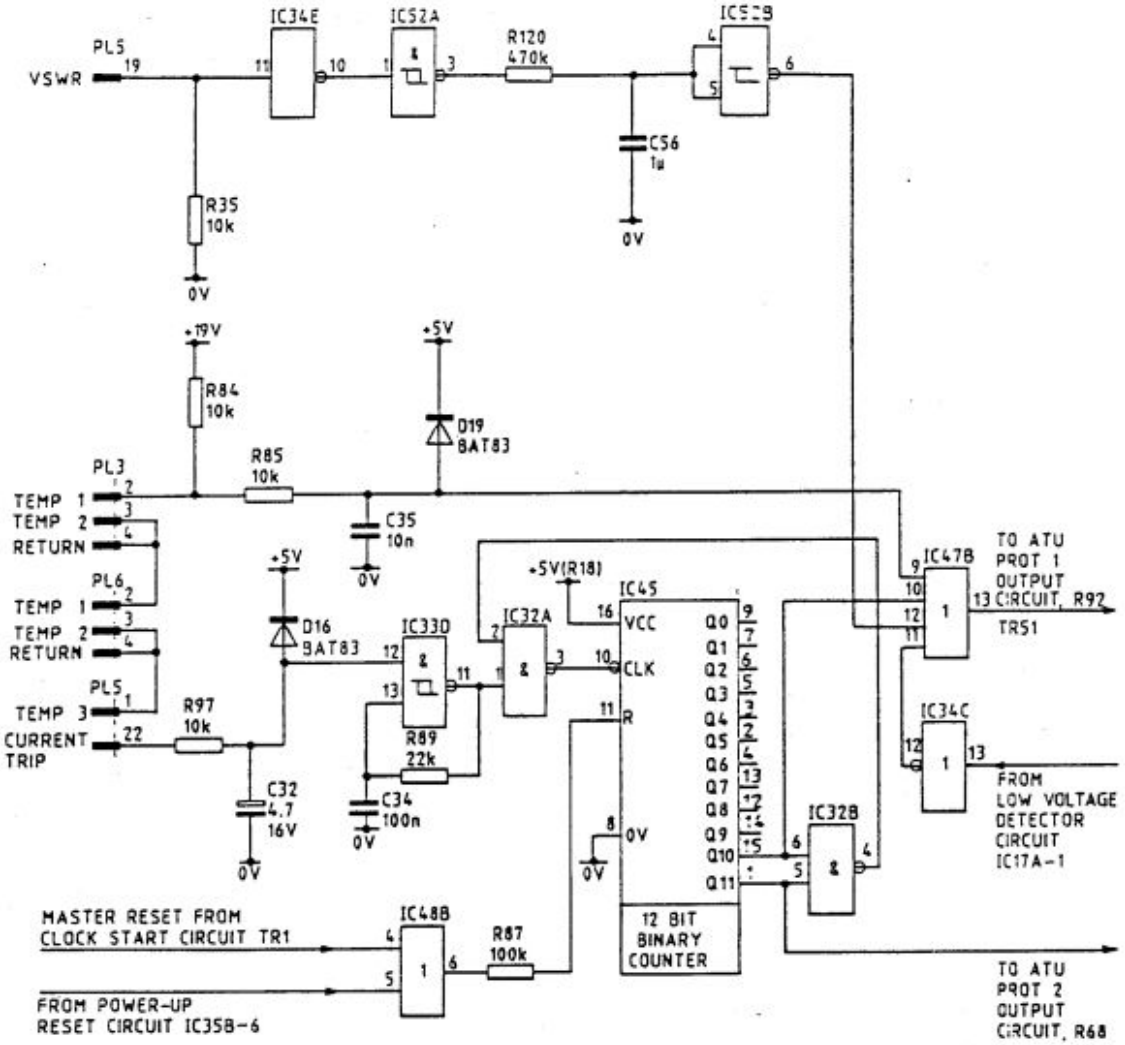

FIGURE 34 - ATU PROTECTION CIRCUITS

ATU PROT 1/ATU PROT 2 Output Circuits (Figure 1004)

ATU PROT 1. (Figure 35)

227. A '1' applied to TR51 base from the ATU protection circuit (IC47B-13) generates an active high ATU PROT 1 control signal output at PL2-7. Under normal operating conditions, the circuit shown in Figure 35 acts as a constant current sink to hold the ATU PROT 1 output at PL2-7 to not more than +0.5 V. The circuit operates by the base emitter voltage of TR52 being held constant by the base emitter bias of TR53 developed across R94. Any increase in current through TR52 will increase the forward bias on TR53. This will reduce the forward bias on TR52, thereby reducing the current flowing through TR53.

228. A '1' output from IC47B-13 will turn on TR51, causing a drop in the voltage at TR52 base. This will turn off TR52, removing the current sink to set ATU PROT 1 active high.

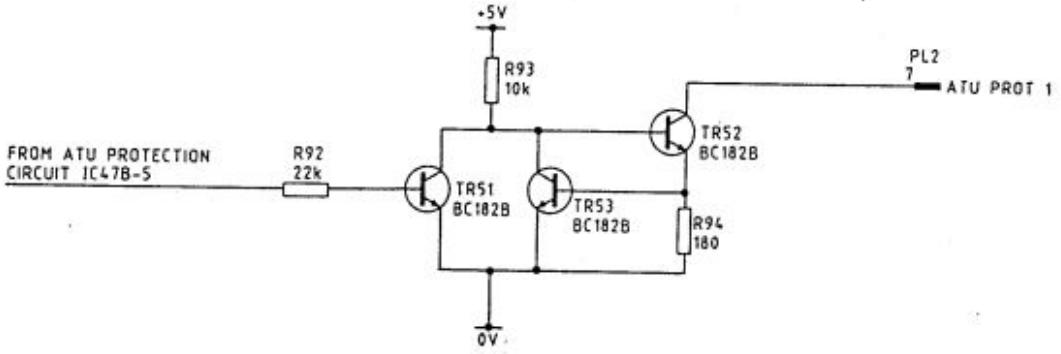

FIGURE 35 - ATU PROT 1 OUTPUT CIRCUIT

ATU PROT 2. (Figure 36)

229. A '1' applied to TR57 from the ATU protection circuit (IC32B-5) generates an active high ATU PROT 2 control signal output at PL2-5. The '1' at R68 will turn TR57 on, taking TR57 collector towards 0 V. This will bias off TR54 taking its collector high. With TR54 biased off, its collector voltage is reduced from the 19 V VCC (via R69) to 10 V by the zener diode D20. The output at TR54 collector provides the active high ATU PROT 2 control signal at PL2-5 via the current limiter R70.

230. An active high ATU PROT 2 output will also be produced by TR54 being biased off from a '0' applied via R71 from the Low Voltage Detector Circuit.

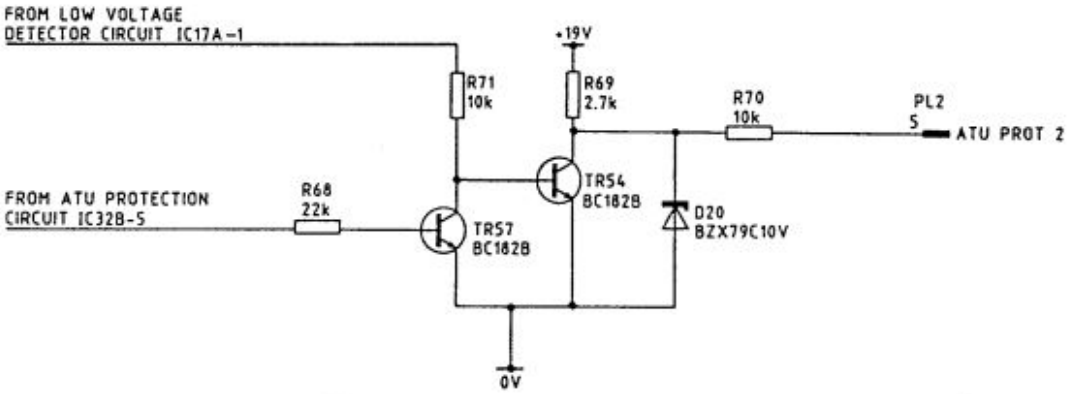

FIGURE 36 - ATU PROT 2 OUTPUT CIRCUIT

Voltage Supply Protection Circuits (Figure 1004)

231. Various protection circuits are used to protect the voltage supplies which are distributed by Module 3 to other HF ATU modules.

232. The +5 V (SWD), +10 V (SWD) and +5 V rails, applied at PL1-5, 4 and 6 respectively, are protected against voltage fluctuations by the zener diodes D31, D29 and D28.

233. Inductors L1 to L4 and L7 provide protection against high currents caused by a nuclear flash. Thyristor TH1 clamps the 5 V rail to 0 V when its gate is taken positive by the nuclear photon effect.

234. When the supply 5 V rail drops momentarily, it is necessary to hold VDD to certain CMOS devices for up to 1 second. This is achieved by C37 which is charged up through the schottky diode D26. To detect if a CMOS device starts to draw excessive current, a 10 Ohm resistor is placed in series with VDD as an aid to identifying faulty devices.

PSU Control Switching (Figure 1004)

235. In order to reduce current consumption and interference, the +5 V (SWD) and +10 V (SWD) regulators in Module 2 are switched on when a Tx/Rx pulse is received, and turned off after the tuning sequence has been completed.

236. The switching is initiated by the output control line PSU CONTROL at PL1-3. The operation of PSU CONTROL output circuit identifying IC8 and TR5 is described in the D-Type Latch output driver circuit description. When the regulators are switched off, the voltage supply is removed from the following circuits:

a. The output buffer on the phase and conductance detectors in Module 4.

b. The WINDOW comparator in Module 4.

c. The RF input circuits to the binary counter.

d. The A to D converter reference voltage chain.

BITE RAM/ROM Tests (Figure 37, Figure 1004)

237. The RAM and ROM contained in IC21 and IC22 respectively are tested when the system supply is turned on. The test sequence may also be initiated by removing 3PL2; in both instances, the test routine is the same. The no fault condition will be indicated by LED D10 as shown in Table 15.

TABLE 15 - BITE RAM/ROM TEST PASS INDICATION

TEST	LED D10
Initial switch on	Permanently on
Disconnecting 3PL2	Flashing every 1s

238. The drive circuit associated with illuminating LED D10 is shown in Figure 37. In operation, a '1' applied to TR16 base from IC9-5 will forward bias TR16 taking its collector towards 0 V. This will forward bias and therefore illuminate D10. R47 limits the current through D10; IC13A and C93 provide decoupling.

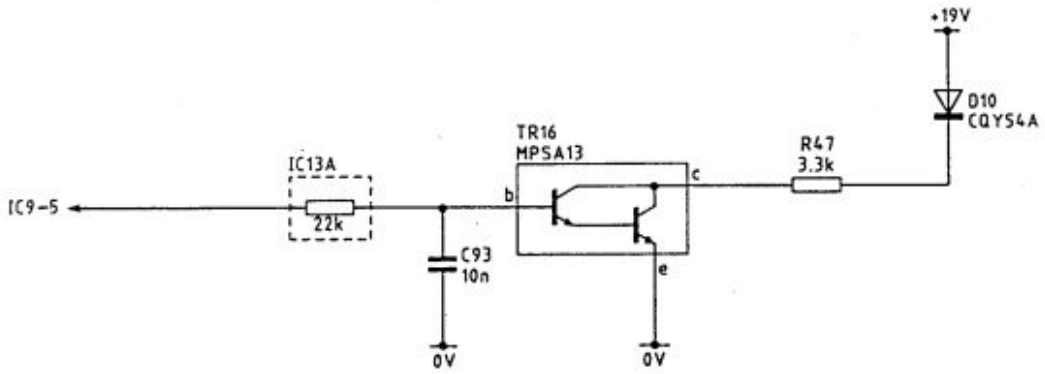

FIGURE 37 - LED D10 DRIVER CIRCUIT

RAM Test. (Figure 1004)

239. The RAM is tested by addressing a location and then writing eight words in succession to that location, starting with '00000001'. In each successive word, the high bit is moved one bit to the left so that every bit of a location has its value changed. After every write, the data is read back and compared with its originating word. If the two words are not the same, 3PL2-2 FAULT is taken active high. This process is then repeated for each location.

ROM Test. (Figure 1004)

240. When the program resident in ROM is first assembled, a checksum is calculated and then blown into ROM address 0FFF. When a ROM test is initiated, the Microprocessor creates its own ROM checksum and then compares this with the value in address 0FFF. If the two checksums are not the same, 3PL2-2 FAULT is taken active high.

MODULE 4 - DETECTOR MODULE

General

241. Module 4 houses a section of the HF ATU tuning components, plus six detectors which provide data for analysis by the Microprocessor on Module 3. This data enables the Microprocessor to select the components required to tune the HF ATU. The selection of the tuning components (series inductors and shunt capacitors) is achieved by relays which, when energised by a control signal from the Microprocessor, switch in or out the relevant components as required. The RF output from the tuned circuit is routed to Module 5.

242. A functional block diagram of Module 4 is shown at Figure 38 and a detailed circuit diagram at Figure 1005. All relays are shown de-energised. With reference to Figure 38, Module 4 contains the following functional circuit blocks:

a. Low Voltage Crowbar.

b. VSWR Detector.

c. Conductance Detector.

d. Phase Detector.

e. Power Detector.

f. Antenna DC Resistance Detector.

g. Circulating Current Detector.

h. Fine Tuning Inductor and Capacitor Selection.

243. When a tuning sequence is initiated in the HF ATU by the HF R/T, a control signal on the 50R relay input line energises RLB and routes the RF input through a Power Detector and an RF counter. The resultant data is passed to Module 3 for analysis by the Microprocessor and determines whether the tuning sequence should be initiated or not.

244. With both RLA and RLB de-energised, the RF is routed through the Phase, Conductance and Antenna DC Resistance Detectors, whose outputs are routed to the Microprocessor. With RLA de-energised and RLB energised, the RF is routed to a Power Detector and an RF counter, again for analysis by the Microprocessor.

245. A dc bias is applied to the Phase and Conductance Detectors via the DET OFFSET control line, to allow the analogue dc to swing around a 2.5 V zero reference level. During the tuning sequences, the circulating currents are constantly monitored, and if the +19 V regulator rail drops below +13.5 V, the RF input is clamped by the Low Voltage Crowbar circuit.

246. RLA is energised by a control signal on the DET RELAY line when a successful tuning sequence has been completed. The RF is then routed through the selected tuning circuitry, bypassing the Phase and Conductance Detectors, and out to Module 5.

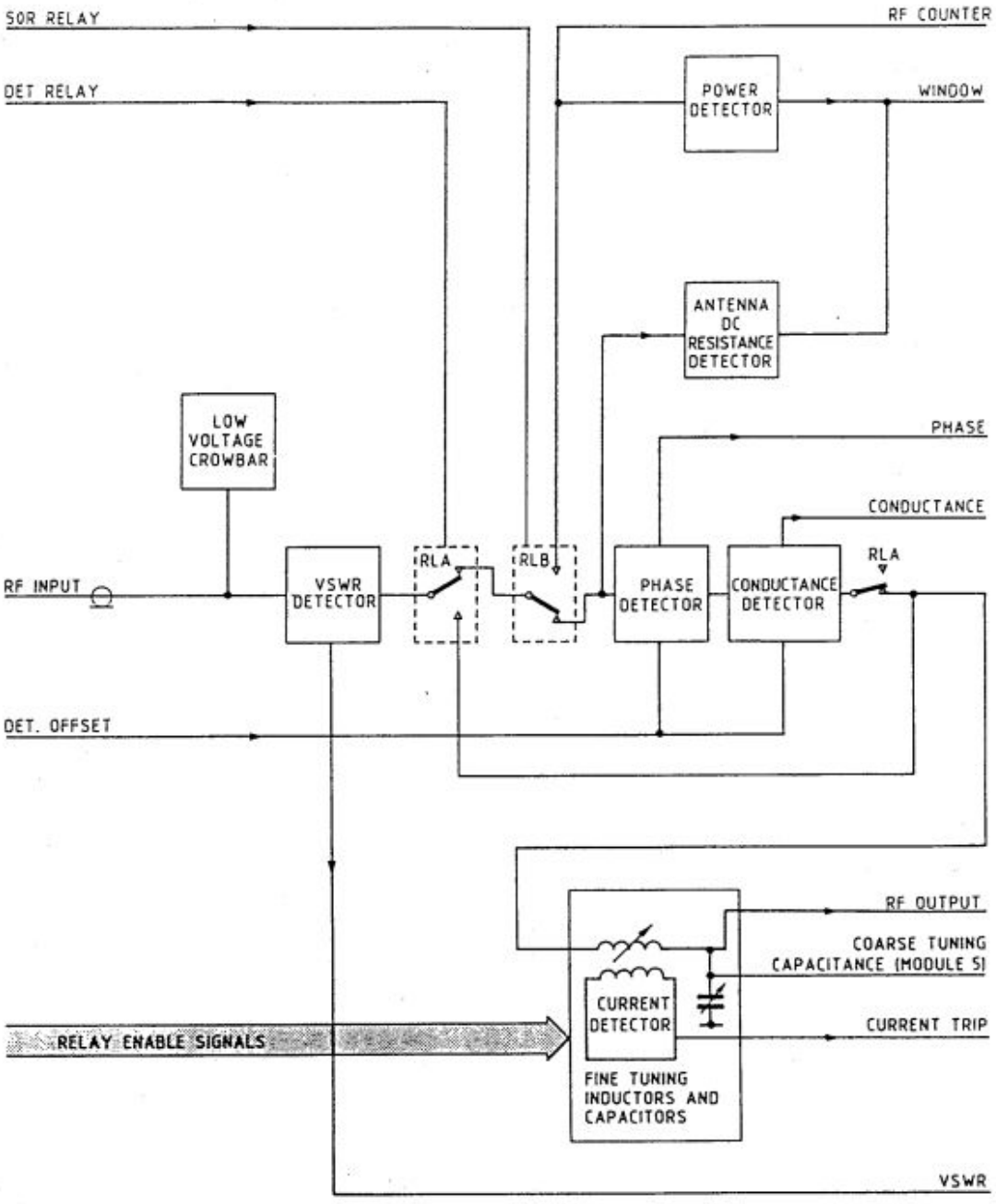

FIGURE 38 - MODULE 4 FUNCTIONAL BLOCK DIAGRAM

VSWR Detector (Figure 39, Figure 1005)

247. The VSWR Detector indicates the ratio between the forward and reflected RF power at the input of the HF ATU. The detector output is routed to a comparator circuit, whose output is high when the forward power is approximately eight times that of the reflected power, indicating an acceptable VSWR. To ensure that the comparator output is not effected by amplitude modulation of the RF carrier, a low-pass filter is inserted in circuit when the HF ATU is not tuning.

248. The circuit shown at Figure 39 consists of two identical power detectors, each supplied with an induced voltage from the secondary windings of transformer T1. To create a forward and reverse power detector, the two secondary windings are wound in opposite directions to each other.

249. Diode D1 and its associated components comprise the forward power detector, which rectifies the vector sum of the voltage developed across the capacitive potentiometer C1 and C2, and the voltage developed across R2 and R3 by the secondary winding of T1. The resultant dc voltage is applied to the voltage comparator IC1B-5, via potential divider R13 and R12, these resistors ensuring that IC1B-7 remains high while the voltage ratio at pins 5 and 6 of IC1B is less than a nominal 3:1. In practice this threshold can lie between 3:1 and 6:1. R6 and C11 provide a filter network on the output of D1. R91 and R4 form a potential divider chain which creates a small dc bias to increase the linearity of the detector, while L1 prevents the RF from being shorted to 0 V by R4.

250. Diode D2 and its associated components comprise the reverse power detector. The action of these components is identical to those of the forward power detector. The voltage induced across R7 and R8 is 180 degrees out of phase with the voltage developed across C17 and C18. These voltages are summed and the rectified output applied to IC1B-6. R9 and C13 provide a filter network on the output of D2. R11 and R10 form a potential divider chain which creates a small dc bias to increase the linearity of the detector, while L2 prevents the RF from being shorted to 0 V by R10.

251. IC1B-7 will remain low (0 V) until the dc voltage on pin 5 exceeds the dc voltage on pin 6. In terms of forward and reflected power, the crossover point from low to high (+10 V) on IC1B-7 occurs when the forward power is approximately eight times larger than the reflected power. R22 provides hysteresis and R25 is a pull-up resistor.

252. Because the detector is always in circuit, it is possible that modulation could adversely effect a marginal VSWR for short periods. To avoid this condition being reflected in the output (PL2-8), IC1B output is fed via an active filter circuit consisting of IC1A, R15, C14 and R50. This circuit acts as a 12 dB low-pass filter, R15, C14 and R50 smoothing any transients that may appear on the output of IC1B.

253. The low-pass filter is not required during the high speed switching sequences of automatic tuning, therefore TR7 is switched on by the +10 V (SWD) supply being applied to its base via R16. This effectively shorts out R15 and R50, causing IC1A to behave as a straightforward unity gain buffer. R26 is a pull-up resistor and R51 provides current limiting.

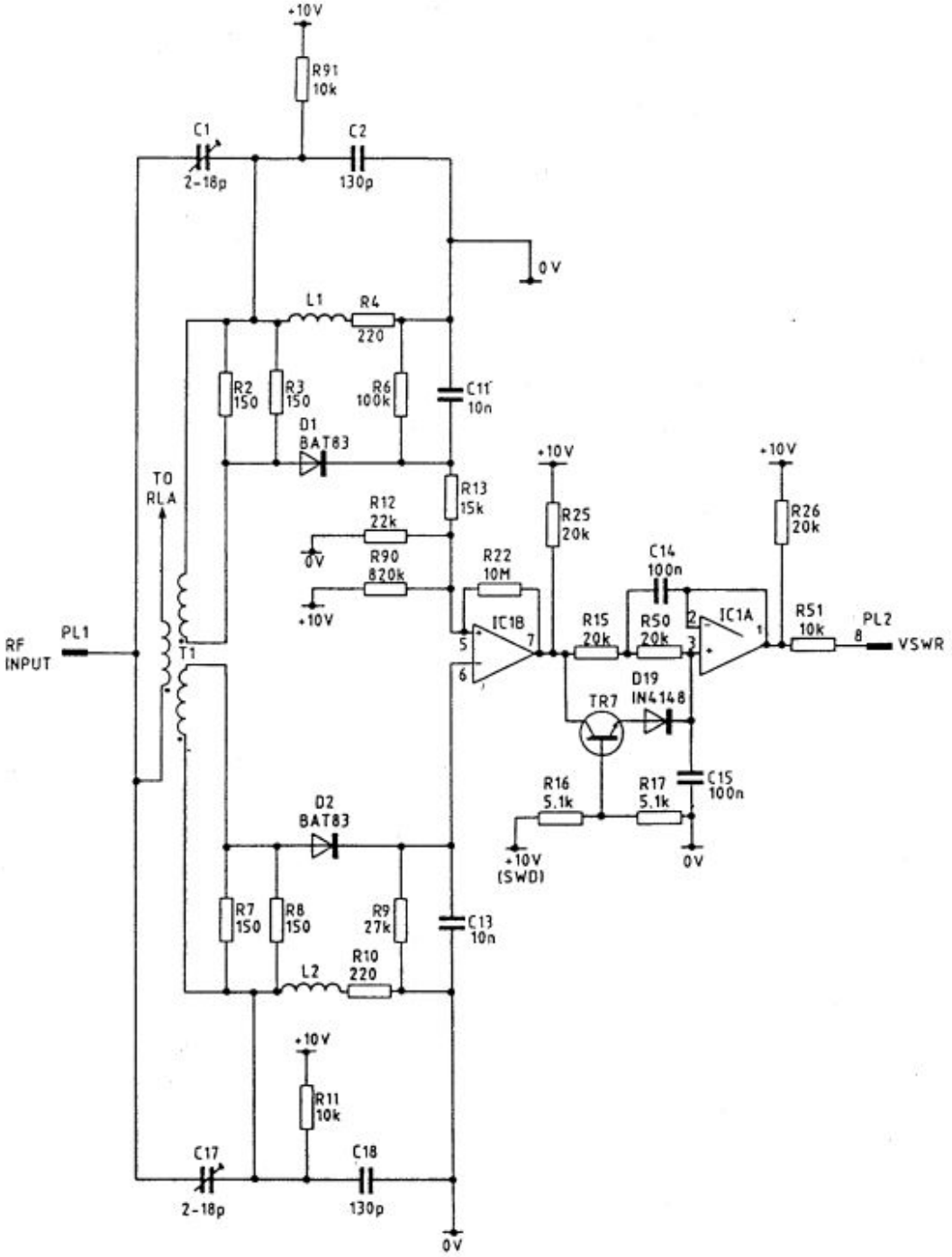

FIGURE 39 - VSWR CIRCUIT

Low Voltage Crowbar (Figure 40, Figure 1005)

254. If the +19 V regulator output falls below +13.5 V, the Low Voltage Crowbar circuit ensures that the RF input is removed from the tuned circuit selection relays before they open, by routeing it to 0 V via relay RLN.

255. Under normal +19 V supply conditions, TR4 is forward biased by +19 V applied to its emitter, and a base voltage of +16.5 V derived from R61, R62 and zener diode D29. The positive voltage derived from TR4 collector current (via R64 and R67) is applied to the base of TR6, taking its collector towards 0 V. The 0 V causes RLN to energise, opening its contacts and removing the 0 V line from the RF input. RLN is shown de-energised in Figure 40.

256. If the +19 V supply falls to +13.5 V, the voltage on the base of TR4 will be held at +13 V by the action of D29, causing the base/emitter junction to be reverse biased. TR4 switches off and removes the forward bias from TR6 which also switches off. The 0 V is removed from RLN relay coil, RLN de-energises and its contacts short the RF input to 0 V. D31 will conduct to prevent any large voltage induced by opposition to the collapsing magnetic field.

257. The circuit is nuclear-hardened by the electrical surge arrestor SG1, which clamps the RF in the event of a large current surge.

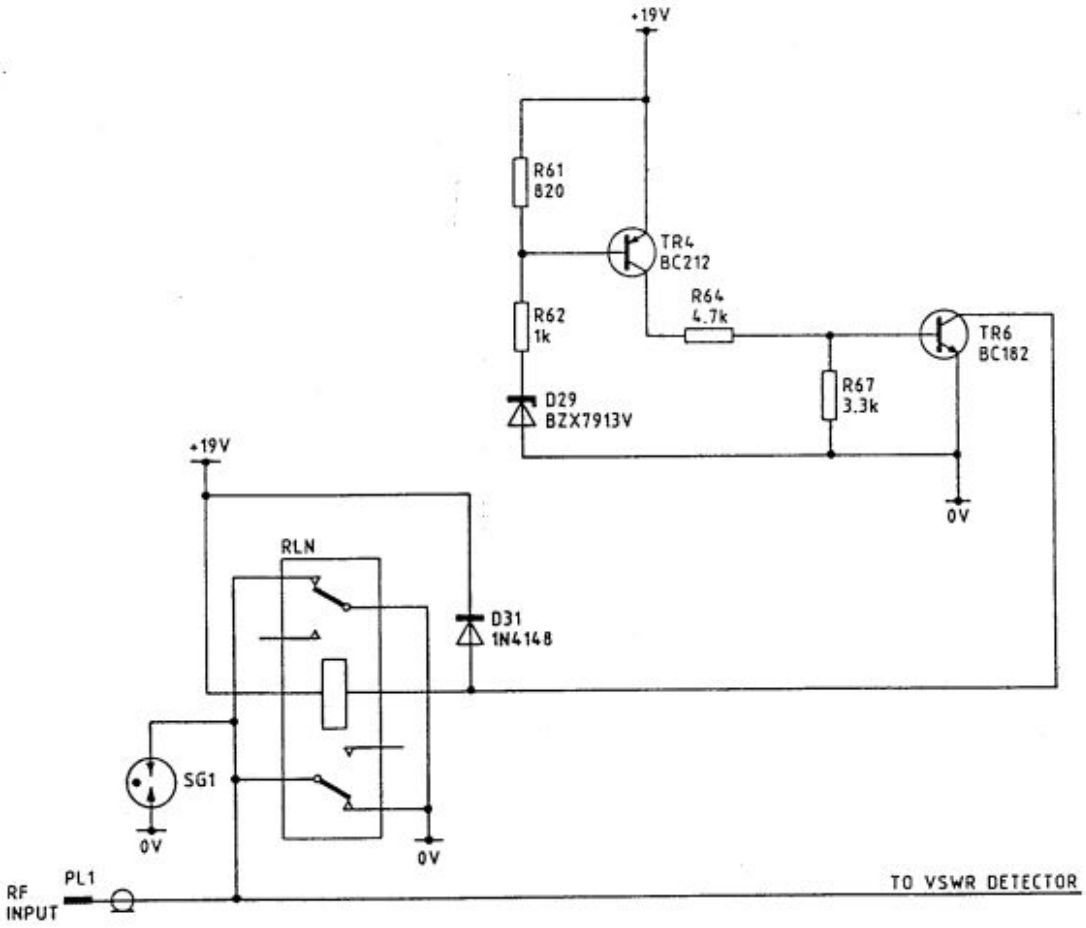

FIGURE 40 - LOW VOLTAGE CROWBAR CIRCUIT

Conductance Detector (Figure 41, Figure 1005)

258. The Conductance Detector is used to determine the magnitude of the resistive component (specified in terms of conductance), of the impedance presented by the HF ATU. The successful completion of the inductor switching tuning sequence, is indicated by a resistive component of 50 Ohms (20 milli-Siemens conductance). The output of the detector is an analogue dc proportional to the conductance of the HF ATU tuned circuits.

259. The detector circuits formed by D6 and D7, and associated components, have two inputs:

a. A function of the RF input voltage developed across C21 and C23.

b. A function of the in-phase line current developing a voltage across R29, which is in anti-phase to the voltage at a. above.

260. After detection by D7 and D6, the resultant dc voltages are developed across R36, R33, and R31, R32.These voltages are opposite in phase and equal in magnitude, when the ratio between the RF input voltage and the in-phase component of the RF line current is 50:1. Under these conditions, the in-phase resistive impedance component is 20 milli-Siemens, and the output of the buffer amplifier IC3A is 0 V. C32, C20, C34 and C22 provide de-coupling. In addition to the conductance, the impedance presented by the HF ATU contains some other reactive component, this is reduced at a later stage with the use of the Phase Detector circuit.

261. The dc output of IC3A becomes more positive as the conductance increases, and more negative as the conductance decreases.

262. A reference level voltage of +2.5 V is supplied from Module 3 to 4PL2-6. This voltage is applied to the Conductance Detector via R34, and to IC3A-3 via bias resistor R35, to allow the dc output from the conductance detector to swing around this reference level. L5, C31 and C10 provide a low-pass filter to the +2.5 V dc input.

263. To prevent IC3A-3 going below 0 V, D26 anode is held at +0.43 V by the potential divider R88 and R89. If IC3A-3 drops to 0 V, D26 conducts and clamps the line.

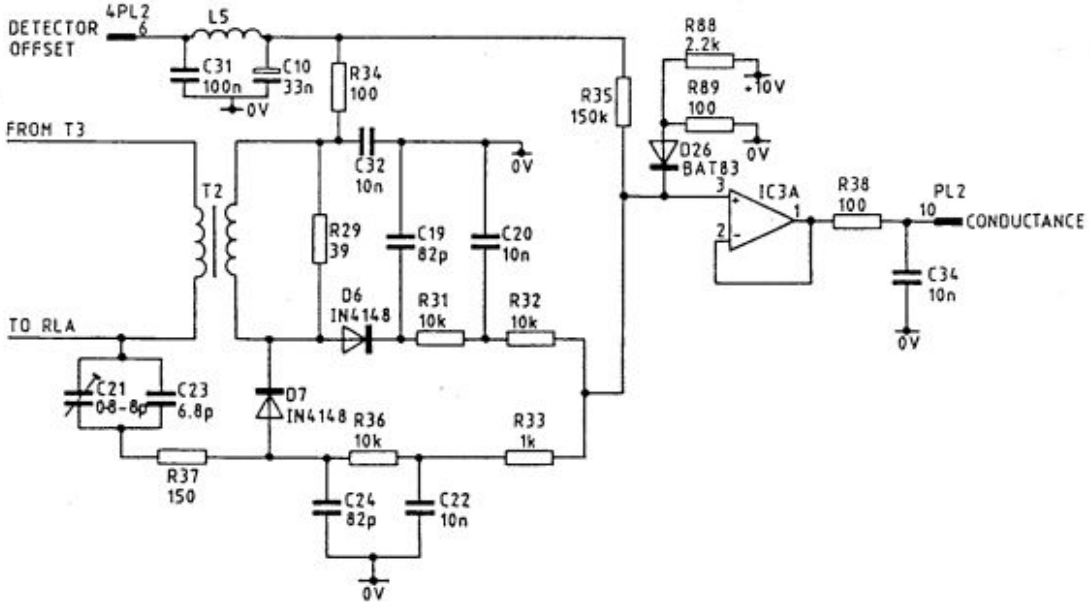

FIGURE 41 - CONDUCTANCE DETECTOR CIRCUIT

Phase Detector (Figure 42, Figure 1005)

264. The Phase Detector is an adaptation of the Foster-Seeley discriminator and determines the impedance of the HF ATU in terms of its inductive and capacitive reactance components.

265. An RF voltage, 90 degrees out of phase with the RF input, is produced across T2 primary, C28, R47 and T4, and is applied between the centre tap of T3 secondary and 0 V. A voltage proportional to the RF current is also developed across R39.

266. When the RF current and voltage are in phase, the rectified voltages produced by D8 and D9 are equal in magnitude but opposite in phase, producing 0 V at the slider contact of R42. Any reactance present in the HF ATU impedance will alter the relative RF voltage magnitudes applied to D8 and D9, producing a dc output at the slider contact of R42. The dc outputs produced will be positive for a capacitive reactance and negative for an inductive reactance. Decoupling is provided by C25, C26 and C27.

267. The output of the Phase Detector is applied to the buffer amplifier IC3B-5 and then out to 4PL2-9. A reference level voltage of +2.5 V is supplied from Module 3 to 4PL2-6. This voltage is applied to the Phase Detector via R43, and to IC3A-3 via R44, to allow the dc output from the Phase Detector to swing around this reference level.

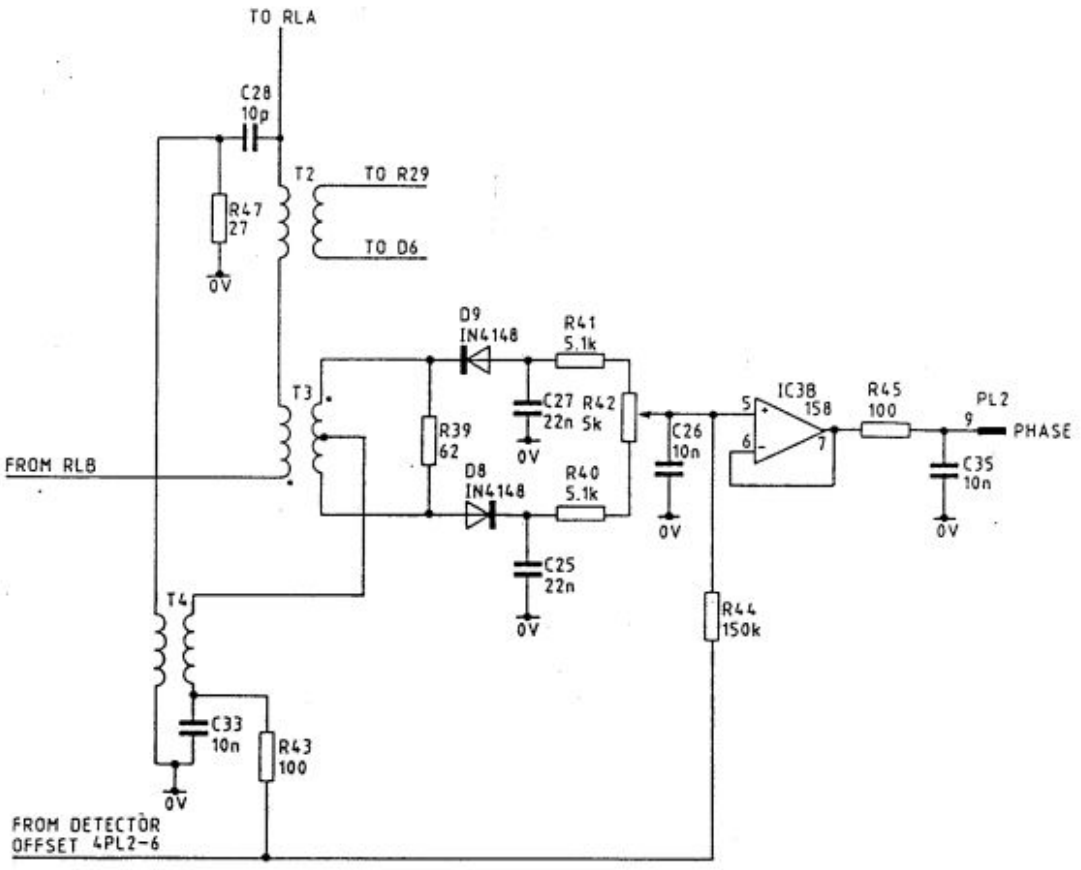

FIGURE 42 - PHASE DETECTOR CIRCUIT

Power Detector (Figure 43, Figure 1005)

268. The Power Detector measures the RF input power. If the RF input power is outside the limits of 1 W to 7 W, a logic 1 signal is sent to the microprocessor on Module 3 to abort the tuning sequence.

269. The RF input is applied across the detector load R63 and fed out, via isolating resistor R30 and 4PL2-25, to the counter circuits on Module 3. The RF input is also fed to the half wave rectifier D30, via potential divider R68, R69. After rectification, the RF power is reduced by the voltage divider network R70 and R71 and applied to comparator IC2A-5 and to IC2B-2. D24 restricts the detected RF voltage to +15 V.

270. A reference level of +3 V, derived from the +12 V supply, is applied via the voltage divider network R72, R20 and R21 to the comparator IC2A-6. A second reference level of +0.74 V is also derived from this network, and applied to IC2B-3 via R54.

271. If the RF input exceeds 7 W, the voltage on IC2A-5 will exceed +3 V, causing IC2A output to go to +10 V. IC2B output will be held at 0 V. If the RF input falls below 1 W, the reverse will happen with IC2A output held at 0 V and IC2B output going to +10 V. Whichever of these two conditions arises, either D4 or D5 will conduct, dropping 5 V across R80 (which forms a potential divider with R36 on Module 3) and putting a logic 1 (5 V) on 4PL2-7. The logic 1 is routed to the microprocessor on Module 3 and the tuning sequence is aborted.

272. Decoupling is provided by C57 and C16, and hysteresis on IC2A and IC2B is obtained from the feedback components R23 and R24. R27 and R28 are +10 V pull up resistors.

273. The outputs of IC2A and IC2B feed two of the three inputs of an OR function formed by D4, D5 and D23 in the antenna dc resistance detector circuit. If any of these inputs are taken high then PL2-7 WINDOW will become a '1'.

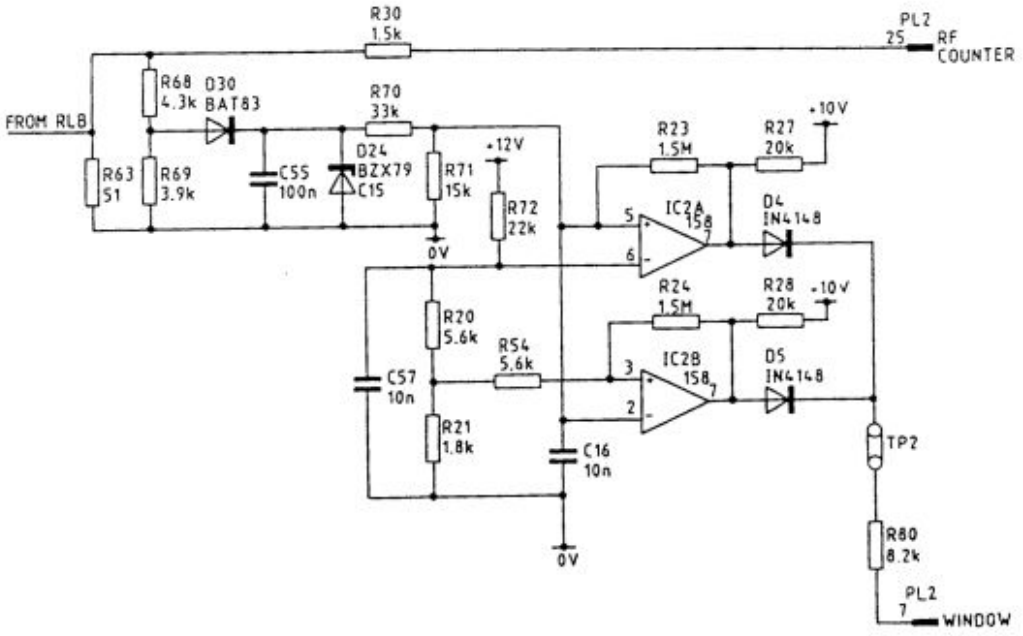

FIGURE 43 - POWER DETECTOR CIRCUIT DIAGRAM

Antenna DC Resistance Detector (Figure 44, Figure 1005)

274. If the dc resistance between the RF input and 0 V lines is less than 75 Ohms, the Antenna DC Resistance Detector outputs a '1', which is applied to D23. D23 forms an OR function with D4 and D5 of the power detector circuit, and the logic 1 on D23 causes a logic 1 to be applied to 4PL2-7, flagging a fault to the microprocessor on Module 3. The tuning sequence is then aborted.

275. As shown in Figure 44 , a reference voltage of +0.14 V is derived from the +10 V (SWD) line by potential divider R73, R77 and applied via R76 to the comparator IC4A-3. A dc voltage, dependent on the resistance between the junction of R74, R75 (RF line) and 0V, is applied to IC4A-2. If this resistance is less than 75 Ohms, IC4A output will be approximately +7 V. D23 will conduct and route the +7V through R80, which drops 2 V (in conjunction with R36 on Module 3) and puts +5 V (logic 1) on PL2-7.

276. R79 is a +10 V pull-up resistor, R78 provides hysteresis, and C50 and C51 are decoupling capacitors.

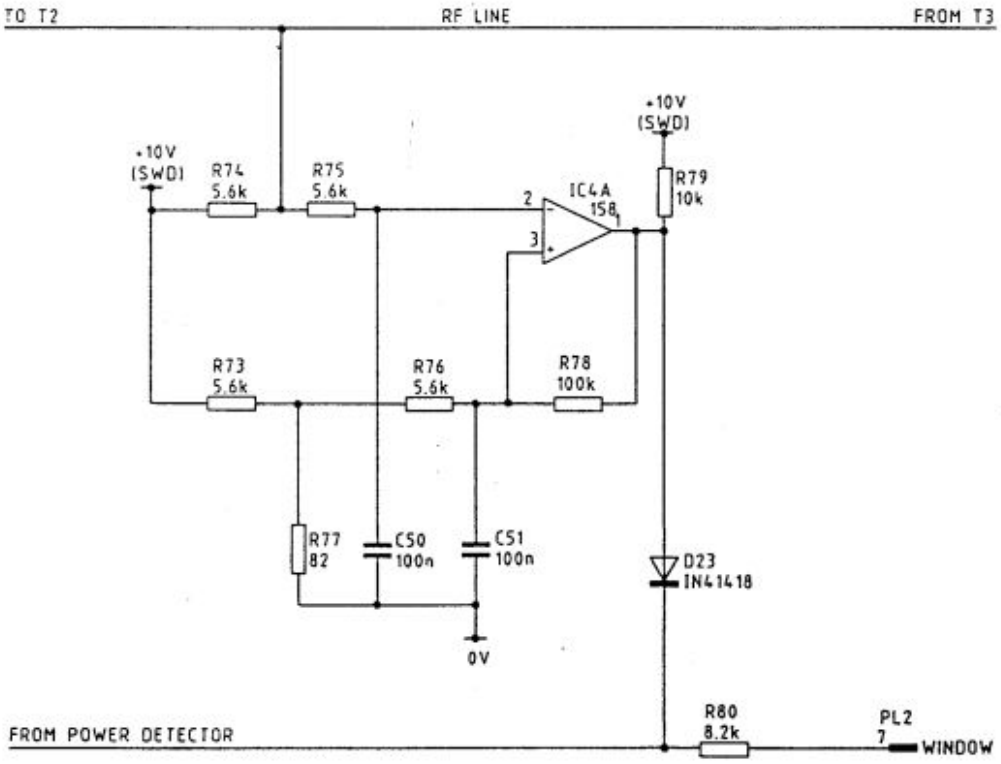

FIGURE 44 - ANTENNA DC RESISTANCE DETECTOR CIRCUIT DIAGRAM