RECEIVER/TRANSMITTER, HF (RT-F100)

Contents:

Further information available in EMEI TELS, T022

INTRODUCTION

1. The RT-F100 is a multi-channel, Receiver/Transmitter (R/T), providing upper sideband (USB), lower sideband (LSB), morse (CW) and DATA modes of operation in the 2-30MHz frequency range.

2. Refer to Figure 1. The HF R/T performs two main and six complementary functions.

a. Transmit. Provided by a frequency synthesiser based transmitter employing a balanced modulator to produce the modulated SSB signal, and two stages of mixing to raise the signal to the required final frequency. Antenna matching is provided by an Antenna Tuning Unit.

b. Receive. Provided by a double superhet receiver with synchronous demodulation. The receiver also employs frequency synthesis and antenna matching.

c. Power Supply Generation. Employs switching regulators to provide the required d.c. supplies.

d. Keypad Control and Display. Provides control data input and displays operator information.

e. Microprocessor Control. Provides software related control of all major functions.

f. Remote Control - provides remote pressel and intercommunication functions of the R/T at a distance of up to 3kM.

g. Data Interface - provides communication between the HF R/T and externally connected ancillary equipments over either a 2.4kBd or 9.6kBd DATA HIGHWAY.

h. Built In Test Equipment (BITE) - provides monitoring, by the microprocessor, of the major functions of the transmit and receive paths.

3. The R/T comprises 15 modules as follows :

Module 1	-	Chassis assembly
Module 2	-	PSU Module
Module 3	-	AF/SSB Module
Module 4	-	Remote Control Module
Module 5	-	Microprocessor Module
Module 6	-	Filter Module
Module 7	-	IF Strip Module
Module 8	}	
	}-	Keypad, Display Assembly
Module 14	}	
Module 9	-	Synthesiser Module
Module 10	-	Bandpass Filter Module

Module 11 - PA Module
Module 12 - ATU Module
Module 13 - Battery Filter Module
Module 15 - Fuse Board

PRINCIPLES OF OPERATION

COMMON CIRCUITRY WITHIN THE RT-F100

4 Within the R/T advantage is taken of solid-state switching elements to make some circuitry common to both the transmitter and the receiver. Three mixers and two oscillator elements provide all tuning and frequency-changing.

5. A simplified diagram of the combined signal path and switching is shown in Figure 2. All switching elements change over simultaneously to complete the transmission or reception paths as required.

FREQUENCY DERIVATION

[**Note:** In the USB Mode the carrier frequency is 2kHz below the 'Assigned' (front panel) frequency. In the LSB Mode the carrier is 2kHz above the 'Assigned' frequency.

Transmitter

[Note: In this worked example, an audio input frequency of 2kHz (0.002MHz) is used.]

6. The 'Audio In' is applied to the SSB MODULATOR where it is used to modulate the 1.4MHz REFERENCE frequency. The balanced modulator is hard wired to produce only the upper sideband component of the mixing process. At point 'A' the frequencies present can therefore be represented algebraically by (1.4MHz + 2kHz) i.e. 1.402MHz for the worked example.

7. The output from the SSB MODULATOR is fed via the SSB FILTER (which will be explained as part of the receiver frequency derivation) to the 1st TRANSMITTER MIXER where it is mixed with 36.6MHz (LSB selected) or 39.4MHz (USB or CW selected). The output from the mixer at point 'B' comprise the sum and difference frequencies and can be represented by:

a) With LSB selected :

(36.6MHz + 1.402MHz) i.e. 38.002MHz

AND

(36.6MHz - 1.402MHz) i.e. 35.198MHz

b) With USB or CW selected :

(39.4MHz + 1.402MHz) i.e. 40.802MHz

AND

(39.4MHz - 1.402MHz) i.e. 37.998MHz

8. The output from the 1st TRANSMITTER MIXER is fed to the 38MHz FILTER which has a bandwidth of 8kHz. This removes the unwanted frequencies produced by the mixing process. The output at point 'C' is therefore:

a) With LSB selected :

(36.6MHz + 1.402MHz) i.e. 38.002MHz

b) With USB or CW selected :

(39.4MHz - 1.402MHz) i.e. 37.998MHz

9. The filter output is fed to the 2nd TRANSMITTER MIXER together with the output from the TUNEABLE OSCILLATOR. The oscillator covers a range of 39.998MHz to 68.0029MHz and the actual frequency applied to the mixer is dependent upon the operating frequency selected by the user. At the bottom of the R/T frequency range (2MHz) the applied frequency will be 40.002MHz or 39.998MHz in the LSB and USB modes respectively. The output from the mixer comprises the sum and difference frequencies and, with 2MHz selected by the operator, the frequency at point 'D' can be shown as:

a) With LSB selected :

(40.002MHz + 38.002MHz) i.e. 78.004MHz

AND

(40.002MHz - 38.002MHz) i.e. 2.000MHz

b) With USB or CW selected :

(39.998MHz + 37.998MHz) i.e. 77.996MHz

AND

(39.998MHz - 37.998MHz) i.e. 2.000MHz

10. The unwanted 'sum' outputs from the mixer are rejected by the Low Pass Filter in the P.A. and the output at the antenna is therefore 2.000MHz

Receiver

[Note: In this worked example, the R/T is assumed to be set to 2MHz , CW. The received signal is the Upper Sideband of a 1.998MHz carrier, modulated by 2kHz audio (2.000MHz)]

11. The signal received at the antenna is fed to the 1st RECEIVER MIXER where it is mixed with the output of the TUNEABLE OSCILLATOR. At the bottom of the band this will be 40MHz. The output at point 'D' will be:

a) (39.998MHz + 2.000MHz) i.e. 41.998MHz.

AND

b) (39.998MHz - 2.000MHz) i.e. 37.998MHz.

12. The output of the mixer is fed to the 38MHz filter where the 'Sum' component is filtered out. The 2nd Receiver input at point 'C' is therefore, 37.998MHz.

13. At the 2nd Receiver Mixer the signal is mixed with 39.4MHz from the oscillator resulting in an output at point 'E' of:

a) (39.4MHz + 37.998MHz) i.e. 77.398MHz.

AND

b) (39.4MHz - 37.998MHz) i.e. 1.402MHz.

14. The output of the 2nd Receiver Mixer is fed to the SSB or CWN Filter. Both filters are tuned to the upper sideband of the IF (1.4MHz) and therefore either will reject the sum output from the Mixer. The SSB filter has a nominal bandwidth of 2.7kHz and the CWN filter has a bandwidth of 150Hz. The output at point 'F' is thus, 1.402MHz.

15. The filter output is fed to the Demodulator where the 1.4MHz is removed giving an audio output of 2kHz.

FUNCTIONAL DESCRIPTION

Transmit

16. Refer Figure 3, Sheet 1. Audio inputs for Voice, Data or CW transmission are fed to the AF/SSB Module as follows:-

a. Voice or data from the MIC (VOICE/DATA) input, or voice from the MIC (VOICE/FILL) input, is routed via passive filter networks on the Filter Board Module.

b. Voice from the MIC ANC input is routed via passive networks on the Remote Control Module.

c. Voice from the MIC REMOTE input is fed via filter networks on the Power Amplifier Module.

d. The CW TONE, a frequency of 2kHz used to modulate the carrier, is fed in directly from the Microprocessor.

e. A separate 2kHz, used to provide CW SIDETONE, is input on the WARNING TONES line from the Microprocessor Module.

17. The AUDIO PROCESSING AND SWITCHING circuit, controlled by the VOICE/DATA and NORM/HOP control lines from the microprocessor, provides voice operated gain adjustment and audio outputs for both sidetone and modulation.

18. Sidetone of the voice and data signals is fed to the AUDIO OUTPUT STAGES where it is amplified and fed out to the operators. The CW sidetone is fed to the AUDIO OUTPUT STAGES via the WARNING TONES line.

19. The output from the AUDIO PROCESSING AND SWITCHING circuit on the AUDIO line is fed to the FIRST IF GENERATOR AND RF MODULATOR for mixing with 1.4MHz frequency derived from the SYSTEM REFERENCE 5.6MHZ. This produces a USB component which, as the FIRST TX IF, is fed to the IF Strip Module.

20. During hopping communication the AUDIO is switched to the HF FHU via the UNPROCESSED AUDIO line by the AUDIO PROCESSING AND SWITCHING circuit. After processing in the FHU the audio is returned via the PROCESSED AUDIO line and then fed out to the FIRST IF GENERATOR AND RF MODULATOR.

21. Refer to Figure 3, Sheet 2. The modulated FIRST TX IF input to the IF Strip Module is routed via an IMPEDANCE MATCHING stage. In the hopping mode, during frequency transitions, the signal is muted by a muting switch, controlled by a TX MUTE signal from the Microprocessor Module. This prevents the transmitter sweeping through a band of frequencies during the transition.

22. The signal is passed through the SSB FILTER, amplified and input to the FIRST TX MIXER together with the output of the SECOND LOCAL OSCILLATOR. The frequency of the SECOND LO is determined by a microprocessor control signal according to whether Upper Sideband (USB) or Lower Sideband (LSB) is in use. The output of the FIRST TX MIXER, the SECOND TX IF, is filtered to remove the unwanted 'sum' components and fed to the SECOND TX MIXER.

23. In the SECOND TX MIXER the SECOND TX IF is mixed with an input from the MAIN LOCAL OSCILLATOR, controlled by the microprocessor, to produce a modulated RF DRIVE at the frequency of operation selected via the keypad. This RF DRIVE is buffered and fed out to the PA Module.

24. Refer to Figure 3, Sheet 3. The RF DRIVE from the IF Strip Module is filtered and fed to the FIRST RF AMP (RF Amplifier) stage which can be muted by the microprocessor during frequency hopping transitions.

25. The gain of the SECOND RF AMP stage is set by the BIAS LEVEL input from the Automatic Level Control (ALC) circuit. The power level selected at the front panel is relayed from the microprocessor via the POWER LEVEL SELECT line. An analogue voltage proportional to the the forward power is fed to the ALC circuit via the FWD POWER line from the ATU Module. The ALC circuit adjusts the bias to produce a final R/T output at the power level selected.

26. When the High Power Amplifier (HPA) is in use, SYSTEM ALC, fed in via the Auto Control connector on the rear panel, is switched into the ALC loop by the microprocessor to control the R/T output power level.

27. Conditions within the ATU are monitored via the FWD POWER and REFL POWER lines from the FWD/REFL POWER DETECTOR and OVERCURRENT from the CURRENT MONITOR. Should the comparison of forward and reflected power give a BAD VSWR signal, or should OVERCURRENT indicate excessive RF current conditions, the ALC will reduce the BIAS LEVEL and therefore the output power of the R/T. The same reaction will occur in the event of excessive heat within the PA Module being indicated by the HEATSINK TEMPERATURE SENSING element.

28. The output of the THIRD RF AMP is a nominal 1.25W. When output power levels lower than this value are selected the gain of the amplifier is reduced by the GAIN CONTROL stage under the control of the microprocessor signal, GAIN CUT. Power is also reduced in this manner during tuning.

29. The FOURTH RF AMP is switched in to obtain power levels of 5W or 20W. The level is determined by the bias applied which is selected by the 20W/5W SELECT from the microprocessor.

30. For power levels of less than 5W, the FOURTH RF AMP stage is by-passed and the FINAL RF DRIVE, in the range 20mW to 1.25W (as selected on the front panel), is output to the selected antenna via the Bandpass Filter and ATU Modules.

31. During automatic tuning of the ATU, the ANTENNA TUNE OFF/ON control signal from the microprocessor, switches an ATTENUATOR into the signal path to provide additional buffering between the PA and the ATU.

32. In the Bandpass Filter Module the signal passes through one of the seven BAND PASS FILTERS (F1-F7) selected, according to the frequency in use, by the microprocessor via the FILTER SELECT control line and the FILTER CONTROL circuit. The output from the bandpass filter is then fed out to the ATU Module via a 30MHz LOW PASS FILTER which reduces the level of any harmonics which might otherwise cause interference on the VHF band.

33. In the ATU Module, the FINAL RF DRIVE is routed to either the WHIP ANTENNA or the 50Ω SOCKET, by ANTENNA SELECT from the microprocessor, in accordance with the setting of the front panel 50Ω/Antenna switch. With Antenna selected, the RF is fed to an IMPEDANCE MATCHING network, whose inductive and capacitive elements are switched into or out of circuit, as required, by relays under the control of the microprocessor. This matches the output impedance of the R/T, at the operating frequency, to the impedance of the selected antenna.

34. The information necessary for the control of the IMPEDANCE MATCHING network is provided by three detectors within the ATU. The outputs from the detectors are REFL PWR MEAS, a voltage proportional to the reflected power, PHASE, a logic signal indicating whether the line voltage and current are in phase, PHASE MEASURED, an analogue of the phase difference, and CONDUCTANCE, a logic level indicating that the antenna has been matched to 50Ω impedance.

Receive

35. Refer Figure 4, Sheet 1. The received RF signal from the WHIP ANTENNA or from the 50Ω input socket is relay selected on the ATU Module by a signal from the microprocessor, initiated by the operator via a front panel toggle switch. The WHIP ANTENNA input passes through the RF MATCHING NETWORK of the ATU Module while signals fed in via the EXTERNAL ANTENNA input are fed directly to the Bandpass Filter Module.

36. The selected signal is fed to the Bandpass Filter Module where it passes through a 30MHz LOW PASS FILTER and then the appropriate band pass filter (F1 to F7) to the input of the IF Strip, via the PA Module. During the receive function the circuit elements of the PA Module are not required and are therefore by-passed.

37. In the IF Strip the received RF is fed into the FIRST RX MIXER where it is mixed with the output of the Main Local Oscillator (MAIN LO) from the Synthesiser Module. The frequency of the MAIN LO is controlled by the microprocessor so that the output of the mixer is the first IF of 38MHz.

38. The mixer output is fed through the FIRST RX IF FILTER, amplified by the FIRST IF AMP and mixed in the SECOND RX MIXER with one of two SECOND LO frequencies. The frequency of the SECOND LO is determined by the microprocessor according to whether USB or LSB is selected.

39. The output of the SECOND RX MIXER, the second IF at a frequency of 1.4MHz, is filtered by the VOICE DATA CW FILTER, or the CWN FILTER, selected by the SSB/CWN switch. A separate filter is used for CWN to reduce the bandwidth of the received signal and thus provide an improved signal to noise ratio. The second IF is then amplified in the SECOND IF AMP before having the audio content extracted in the DEMODULATOR. The 5.6MHz output from the SYSTEM REFERENCE OSCILLATOR, on the Synthesiser, is fed through a DIVIDER STAGE on the AF/SSB Module to obtain a 1.4MHz reference (REFERENCE FREQUENCY) which is fed to the DEMODULATOR. This 1.4MHz reference is mixed with the modulated second IF. The IF frequency content is cancelled and the audio modulation is fed to the AF/SSB Module.

40. A sample of the audio output from the DEMODULATOR is fed into an AGC GENERATOR stage that produces an AGC output which is fed back to the FIRST and SECOND IF AMP stages.

41. Refer to Figure 4, Sheet 2. The AUDIO from the IF Strip is passed to the AF/SSB Module where it is fed through an ALC (Automatic Level Control) stage which maintains a consistent mean level of output independent of its mean input level. The signal is then fed through the RX AUDIO ENABLE circuit to the AUDIO PROCESSING AND SWITCHING circuit. A sample of the received audio is fed to the SQUELCH CONTROL circuit where the level of squelch is controlled by the SQUELCH VOLTAGE from the R/T front panel control.

42. The outputs of the SQUELCH CONTROL circuit are fed to the RX AUDIO ENABLE circuit and the AUDIO OUTPUT STAGES. With no audio the output from the SQUELCH CONTROL would switch off the power amplifiers and de-energise the RX AUDIO ENABLE circuit preventing noise being passed to the AUDIO PROCESSING

AND SWITCHING circuits. With audio present the SQUELCH CONTROL would bias on the AUDIO OUTPUT STAGES and energise the RX AUDIO ENABLE circuit. When the front panel squelch control is set to off, the microprocessor overrides the SQUELCH CONTROL circuit, via the SQUELCH/NO SQUELCH line, switching on the AUDIO OUTPUT STAGES and energising the RX AUDIO ENABLE.

43. The AUDIO PROCESSING AND SWITCHING circuitry provides audio path routing together with associated amplification, filtering and muting functions appropriate to the various modes of operation of the R/T. It is controlled by two microprocessor control lines, VOICE/DATA and NORM/HOP.

44. During normal voice and data communication the AUDIO input is fed to the AUDIO OUTPUT STAGES for amplification.

45. During hopping communication the AUDIO is switched to the HF FHU via the UNPROCESSED AUDIO line. After processing in the FHU the audio is returned via the PROCESSED AUDIO line and then to the AUDIO OUTPUT STAGES for amplification.

46. The gain of the amplifier supplying the PHONES (VOICE/DATA) and PHONES (VOICE/FILL) ancillaries is adjusted by the front panel VOLUME CONTROL. The PHONES ANC and PHONES REMOTE outputs are provided by a fixed gain amplifier.

47. The audio output to PHONES (VOICE/FILL) and PHONES (VOICE/DATA) are fed out via the FILTERS on Module 6. Outputs to PHONES ANC are fed out via FILTERS on the Remote Control Module, and outputs to PHONES REMOTE are fed out via FILTERS on the PA Module.

48. WARNING TONES, generated by the microprocessor for BITE functions, are fed out of the R/T after amplification in the AUDIO OUTPUT STAGES.

Microprocessor Control

49. Refer Figure 1. The Microprocessor Module functions as the control centre of the HF R/T and, to some extent, the system into which the radio is connected.

50. Instructions for the operation of the R/T are held as a program in the Read Only Memory (ROM) and the working data for the program, including Fill data, are held in Random Access Memory (RAM). Data in RAM is maintained by a back-up battery during loss of power supply.

51. Control of the R/T is exercised by digital signals produced in response to inputs from the front panel controls and keypad, or from peripheral units. In addition, parameter levels within the R/T are constantly monitored and the module produces appropriate controls to direct the units functions.

BITE (Built In Test Equipment)

52. Refer Figure 1. BITE is provided for continuous monitoring, by the microprocessor, of the synthesiser lock condition, VSWR and dc supply voltage. The microprocessor generates audio warning tones and initiates a fault indication on the display if a fault condition is detected. Note that audio warnings will only occur whilst in the receive mode.

53. In addition, the microprocessor has a BITE test program in ROM which, when initiated by the operator, provides two separate levels of equipment test.

Keypad Control and Display

54. Refer Figure 1. The keypad comprises a 3 x 5 matrix of press-operated switches which are the main means by which the operator inputs instructions to the microprocessor. When an instruction is entered the R/T functions are set accordingly and the microprocessor causes relevant information to be shown on the Liquid Crystal Display (LCD).

Data Interface

55. Refer Figure 1. The Data Interface provides the HF R/T with two way communication with peripheral equipments over two data highways at 2.4kBd and 9.6kBd respectively. The FID, Extended Front Panel (EFP) use the 2.4kBd data highway and the Frequency Hopping Unit (FHU) uses the 9.6kBd highway.

Remote Control

56. Refer Figure 1. The Remote Control function allows an operator to utilise the receive and transmit facility of the R/T via a Field Telephone Cable. Operation of controls on a remote handset cause current changes on the line to the R/T. These are sensed by the remote control circuitry and translated into logic inputs to the microprocessor which sets the R/T circuits accordingly.

Power Supply Generation

57. Refer Figure 1. From the nominal +24V input switching regulators produce +10V, +6V, and +5V dc supplies.

DETAILED FUNCTIONAL ANALYSIS

58. The following description is based on the Equipment Functional Block Diagram. The description initially takes the form of a separate explanation for each mode of operation concentrating on the main signal routes and the modules on those routes. Inputs from, or outputs to, control and service modules are addressed during this process where their function affects the main route signal, but each control and service module is finally described in full as a separate functional module.

(Note: Control and service modules include the following items: Microprocessor Module, Keypad, Display Module, Synthesiser Module and PSU Module.)

59. All the switch functions shown within the modules (with the exception of S1 in the PSU Module) are controlled by the microprocessor. Control data from the microprocessor is clocked into control registers on the various modules. The data is then strobed by the microprocessor and appears at the control outputs of the registers.

60. The audio path switching on the AF/SSB Module is complex and the CONTROL SIGNALS legend therefore identifies, beside the associated control signal name, the position in which each switch contact is shown. Throughout the Functional Diagram all RX/TX switches are shown in the RX position. Table 1, Annex A, has been included to show the CONTROL REGISTER output logic associated with the VOGAD, Intercom and Sidetone functions. The various elements included are active with a Logic '1' applied. (i.e. 22A will be in the TX position with logic '1' applied)

Note : Unless indicated otherwise, Logic level '1' is equal to a voltage of +5 Volts and Logic level '0' is equal to zero Volts.

61. In order to simplify the task of following through the diagram and to assist with cross-referencing to detailed circuit diagrams, certain functions have been identified by using the circuit reference number of a component forming the major part of that function (e.g. VOGAD IC2). These should not however be regarded as a finite or comprehensive guide to the components involved in that function.

TRANSMIT

Voice

62. Refer Figure 5. Voice inputs from the local microphone are fed via VOICE/FILL or VOICE/DATA input sockets on the front panel of the R/T, through the Filter Board Module to the AF/SSB Module, Module 3. (3SK7/8 and 3SK7/1)

63. The ancillary microphone input (MIC ANC) enters at the rear panel ancillaries connector and is fed to the Remote Control Module, (4PL1/9) through the RFI FILTER assembly which, in addition to filtering, provides protection against inadvertent application of excessively high voltage levels to the line. The MIC ANC input is then fed to Module 3 (4PL6/2 and 3PL6/11) where it is amplified at 16B and fed to the COMMON MIC POINT.

64. The remote microphone input is fed in from the rear panel mounted remote terminals (REM - and REM +) to 11PL4/7 and 11PL4/10 on the PA Module and then, as MIC REMOTE, onto Module 3 (3PL5/6) to the COMMON MIC POINT.

65. The audio from the COMMON MIC POINT is fed to the VOGAD (Voice Operated Gain Adjusting Device) which is enabled via the VOGAD ON/OFF control line in the SSB mode on transmit. The VOGAD is a non-linear device which gives a constant level output to following stages for widely varying levels of input.

66. The audio is passed via the VOGAD OUTPUT ISOLATION stage, (Refer para 110), through 22B in the Voice position and 22A in the TX position to the COMMON AUDIO POINT (CAP) and then through amplifier 15D. To avoid noise introduction from reciever path circuits the ALC AMPLIFIER is disabled by the CONTROL REGISTER output TX/RX .

67. In the Normal (Non-Hop) Mode the audio is fed via 25A and 25C to the SSB GENERATOR.

68. In the Hop Mode the output from 15D, fed via 15A to the Frequency Hopping Unit (FHU) on the UNPROCESSED AUDIO OUT line, is compressed in the FHU and returned to Module 3 as PROCESSED AUDIO IN. It is then amplified in 15B and rejoins the path to the SSB GENERATOR via 25A in the Hop position.

69. A 5.6MHz input from the Synthesiser (Module 9) is also applied to the generator via a 'Divide by 4' stage providing an input of 1.4MHz. The resulting modulated output, an Upper Sideband signal on a 1.4MHz carrier, is amplified by TR25 and fed out as 1.4MHz TX to the IF STRIP (Module 7) via 12B, 3SK10 and 7PL7/8.

70. Refer figure 6. In Module 7 the 1.4MHz TX signal is fed through an impedance matching stage and is picked up by D7/8. It is then passed through the SSB FILTER via a path selected by the CW/SSB control input from Module 3 acting, via an inverter, on D8/10 and D11/14.

71. In the frequency hopping mode during the frequency transition period (10ms), the TX MUTE line from Module 3 is set to Logic '1', grounding the 1.4MHz TX signal via TR19 and thereby muting the transmitter. This prevents the transmitter 'sweeping' a band of frequencies whilst moving from one frequency to another.

72. The modulated 1.4MHz signal output from the SSB FILTER is fed via D12/15 and amplifier TR13 to the 1st TX MIXER where it is mixed with the 2nd LO input from the Synthesiser (36.6Mhz/LSB or 39.4/USB and CW). The mixer output is amplified, fed through D5/6 and then filtered in the 38MHz FILTER which removes the unwanted components of the mixing process.

73. From the filter the signal passes to the 2nd TX MIXER via D3/4 and D18/19 where it is mixed with the MAIN LO output (40MHz to 68MHz).

74. The 2nd TX MIXER output is amplified and passes via D21/22, 7PL6 and 11PL2 to the PA Module (Figure 7) where the LOW PASS FILTER removes the unwanted 'sum' outputs of the mixer.

75. The signal is amplified by the 1st RF, VARIABLE GAIN and 3rd RF AMPLIFIERS. The gain of the VARIABLE GAIN AMPLIFIER (VGA) is controlled via a summing circuit, SUMMING A, and is determined by the power level selected by the operator. In addition, the gain of the stage is automatically reduced in the event of a malfunction (Paras 104 to 109 refer).

76. The power level selected at the R/T front panel results in the PA CONTROL REGISTER activating one of the five control lines (power set lines A to E) applied to the BIAS LEVEL SWITCHING. The line activated determines the level of bias applied to the POWER CONTROL stage and the resulting dc output from the POWER CONTROL stage is fed via the ATTENUATOR, SUMMING CIRCUIT, ALC CR CIRCUIT and amplifier TR27, to the VGA where it is used to adjust the bias level, thereby setting the gain. The second input to the POWER CONTROL stage, V FORWARD, is a dc voltage proportional to the forward power level detected in the ATU Module. Any increase in the power output level will be fed back via the V FORWARD line to the POWER CONTROL stage whose falling output will cause the gain of the VGA to be reduced. This 'loop' forms the Internal Automatic Level Control (ALC) for the transmit function.

77. When the R/T is set to transmit there would not initially be any RF power present in the ATU Module and the ALC Loop would therefore attempt to set the VARIABLE GAIN AMPLIFIER for maximum output and a power surge would result. To prevent this the ALC CR circuit holds the bias applied to the VGA at a set level for a fixed period of time following the transition to the transmit condition on the TX/RX control line. This allows the RF power to build up before the ALC takes over control.

78. When a 100 Watt Power Amplifier (HPA) is used with the R/T (power level 7 selected), the PA CONTROL REGISTER activates the power level 'B' line setting the drive level to the HPA at a nominal 1.25W. The External ALC line is also activated and this energises switch 8A connecting the SYSTEM ALC to the SUMMING CIRCUIT. The SYSTEM ALC is a dc level inversely proportional to the power output from the HPA and is used to adjust the gain of the VGA in order to achieve and maintain an output level of 100W from the HPA. The Attenuator between the System and Internal ALC lines isolates the two controlling lines allowing the SYSTEM ALC to take control of the VGA gain setting.

79. The bias for the 3rd RF AMPLIFIER is stabilised to ensure that its' gain is maintained at a constant level. The minimum power output required from this stage is 20mW and the maximum is 1.25W (nominal). The ALC cannot vary the gain of the VGA over such a wide range and so, in the two lowest power settings (20mW and 80mW), the gain of the 3rd RF AMPLIFIER is reduced via the GAIN CUT control which switches in the FEEDBACK CONTROL reducing stage gain by 6dB's.

80. In the Hopping mode, during frequency transition, both the 1st and 3rd RF AMPLIFIERS are turned off via the TX MUTE line from the CONTROL REGISTERS.

81. In the TX position, the TX/RX input from the microprocessor energises:

a) TR23 which enables +10V (TX).

b) TR22 which applies +24V SWITCHED to RLA energising the relay and enabling +24V (TX).

82. With power levels of less than 5W selected, the output from the 3rd RF AMPLIFIER is fed via a POWER AMPLIFIER by-pass path, selected by relays RLC and RLB in the de-energised state, to relay RLA.

83. When a power level of 5W or 20W is selected RLC and RLB are energised under the control of 5/20W SELECT from the CONTROL REGISTER, and the output of the 3rd RF AMPLIFIER, nominally 1.25W, is fed to the POWER AMPLIFIER, TR10[illegible].

84. The gain of the POWER AMPLIFIER is set by the level of bias applied via transformer T4. This level is determined by the state of control A (5W SET) which is applied to the BIAS CONTROL circuit. With 20W selected the control is inactive and the bias, and therefore the gain, is set such that the required 20 Watts output is achieved. With 5W selected the control is activated, which sets the bias level to produce an output of 5 Watts from the amplifier. The output is fed via RLB, RLA, RLD/1, RLD/2, 11PL6 and 10PL4 to the Band Pass Filter Module, Module 10.

85. Refer figure 8. In Module 10, one of the seven Band Pass Filters (BPF), appropriate to the frequency of operation, is selected by the microprocessor via the BPF CONTROL REGISTERS and brought into circuit by energising a relay at each end of the filter. These filters provide a degree of co-siting capability and also attenuate second and higher order harmonics generated in the PA Module.

86. Latching relays are used for filter selection. These have both a 'set' and a 'reset' coil. Prior to the selection of a filter, the CONTROL REGISTER sets its Reset Control output 'High'. This 'resets' all the filter relays via the switching stage, TR1. RESET CONTROL then goes low and the appropriate Band Set line is then 'High'. This 'sets' the required relays placing the appropriate BAND PASS FILTER in the signal path. Note that, when operating in the 2FS Mode the band filter will be selected as appropriate for the Transmit or Receive frequency.

87. The signal from the BAND PASS FILTER is then fed through a 30MHz LOW PASS FILTER which further attenuates 2nd Order Harmonics reducing the possibility of interference on the VHF Band.

88. The transmit signal is next fed via 10PL3 and 12PL1 onto the ATU Module (Refer figure 9) which provides and maintains matching between the Bandpass Filter Module and the R/T Antenna at the selected frequency of operation. In addition the ATU Module also provides outputs for the protection circuits within the PA Module. (Paras 104 - 109 refer).

89. The TX signal at a frequency of between 2MHz and 30MHz is fed to Relay A via transformer T1 primary winding. The transformer secondary is connected to the FORWARD AND REVERSE POWER DETECTOR stage which rectifies the forward and reflected signals and sends a dc voltage, proportional to these RF power levels, to the PA Module (Module 11) as FWD POWER and REF POWER.

90. The relays used in the ATU module are the Latching type similar to those utilised in the BPF module. In order to 'Set' or 'Reset' any of the relays on the ATU module, the required relay must also be enabled. Relays are 'set' as follows. Data from the microprocessor clocked into the ATU control registers is placed on the RELAY ENABLE lines by the Strobe input from the microprocessor, thus enabling the appropriate relays. At the same time the microprocessor inputs a SET input via TR1/2 which latches the enabled relays to the 'set' position. Reset is carried out in the same manner.

91. The position of Relay A contacts is determined by the setting of the Antenna Selector Switch on the R/T front panel. With 50Ω selected the TX signal is fed directly out to the front panel via the 50Ω socket. In the whip antenna position the TX signal is fed via the primary of transformers T2, T4, the IMPEDANCE MATCHING circuit and the primary of T5 out to the Antenna socket on the R/T side panel.

Antenna Tuning

92. Tuning of the IMPEDANCE MATCHING circuit takes place when the R/T is keyed following the selection of a new frequency. On operation of the Pressel, the microprocessor switches all inductors into circuit and all capacitors out. It then constantly monitors the forward power level, VSWR, reflected power level, conductance and antenna voltage/current phase relationship while successively switching out inductors until approximate tuning is achieved. At this point capacitors, starting with the lowest values, are switched in until final tune is achieved. (i.e. VSWR = 3:1, conductance = 50Ω and the voltage and current in phase)

(Note that ATU tuning is not carried out when the Antenna Selector Switch is set to the 50Ω position).

93. The CONDUCTANCE DETECTOR in the ATU Module will give a logic '1' output via the DC Amp, IC1A, to the microprocessor when a 50Ω match has been achieved.

94. A dc voltage proportional to the reflected power level is fed from the FORWARD AND REVERSE POWER DETECTOR to the microprocessor as REF PWR MEASURED. The voltage will be zero when correct matching has been achieved.

95. The PHASE DETECTOR provides two outputs to the microprocessor via IC1C and IC1B :

a) A dc voltage proportional to the phase difference between the antenna voltage and current. (Phase Measured)

b) A digital output of logic '1' when V and I are in phase. (Phase)

96. DC voltage levels, proportional to the forward and reflected power, are fed out to the VSWR COMPARATOR on the PA Module as V. FWD and V. REFL.

97. When the VSWR is not in the acceptable region of 3:1, the comparator output will override the normal ALC loop action (Refer para 76) causing VGA to be cut back. The output of amplifier 10b will go high presenting a logic 1, on VSWR MONITOR, to the microprocessor which, in the event of successful tune not being achieved, will cause the display to indicate "BAD VSWR" to the operator. For power settings less than 5W, the display will not be activated by the microprocessor.

98. The action detailed at para 97 will also take place in the event of a high VSWR occurring outside of the tune cycle.

99. It can be seen that RF power is required in order to carry out antenna tuning. In an SSB transmitter where the carrier itself is suppressed the carrier must be modulated in order to provide RF power at the sideband frequency. Recall that the output from the SSB GENERATOR is the sum of the inputs and that the fundamental frequencies are

both suppressed. Without a modulating AF input the output would be zero. (i.e. No power output from the transmitter where there is no modulation present.)

100. To provide the necessary modulation during the tune cycle the microprocessor sets the R/T to the CW Mode. In this mode the carrier is modulated by a 2kHz audio tone from the microprocessor (Para 110 refers). In order to allow the PA Module to cope with the changing conditions incurred by the tuning process the microprocessor instructs the PA CONTROL REGISTER (Figure 7) to activate control signals A (5W SET), TUNE and GAIN CUT. The transmitter is set to the 5W power level via control line 'A' to the BIAS CONTROL circuit of the Power Amplifier.

101. The TUNE control energises RLD/1 and RLD/2, switching the TUNE ATTENUATOR 3dB into the RF path to buffer the PA against the changes which occur during tuning of the ATU. TUNE also causes the time constant of the ALC CR circuit to be reduced, thus allowing the ALC to respond faster to changes. GAIN CUT reduces the gain of the 3rd RF AMPLIFIER, thereby reducing the dynamic range of its output. The range of power levels monitored in the ATU during the tuning cycle are then also reduced, bringing the range of drive levels demanded by the ALC (Para 76 refers) to within the capabilities of the VGA.

102. When the 2FS Mode is selected, tuning at the Receive frequency is carried out by the microprocessor which uses a 'look-up table' to find the components appropriate to the frequency of operation. Tuning at the Transmit frequency is carried out in the normal manner but, once this has been carried out, the microprocessor stores the tuning settings required and, for each subsequent transmission, these settings are automatically restored without the need to carry out a full tune cycle.

103. In the Hopping Mode, the ATU is tuned at the 'Reference' Frequency.

Protection Circuits

104. The transmitter is protected against :

a) Overheating of the Power Amplifier stage.
b) Low supply voltage to the PA (on the 20 Watt power setting).
c) Excessive supply current being drawn from the 24V by the PA Module.
d) High VSWR due to an antenna mismatch.
e) Excess antenna current at the output from the ATU.

105. **Overheating of the Power Amplifier.** Current for the PA stage passes through the PA CURRENT SENSOR. A voltage proportional to the PA current is developed across a THERMISTOR which is in contact with the PA heatsink. This voltage is amplified by 11C and fed to the VGA as a control signal. Any increase in the PA temperature results in the resistance of the THERMISTOR falling, causing a fall in the feedback voltage and thus reducing the gain of the VGA. The BIAS CONTROL circuit is also in contact with the heatsink and has temperature compensation to reduce the bias as the temperature rises.

106. **Low supply voltage** . With 20W selected the LOW VOLTAGE SENSOR will be enabled. If the 24V supply falls below 20V the output of the sensor falls reducing the gain of the VGA.

107. **Excessive supply current.** In the event of the supply current exceeding 4.2A (approx), the output from the SUPPLY CURRENT SENSOR falls causing the gain of the VGA to be reduced.

108. **High VSWR.** Paras 96-98 refer.

109. **Excess antenna current.** Antenna current passing through T5 in the ATU Module (Figure 9) is monitored by the RF POWER CURRENT DETECTOR which feeds OVER CURRENT, a dc voltage proportional to the current, to the COMPARATOR (10A) in the PA module. In the event of excess current flowing in the antenna output circuit, the output of 10A will fall causing the output of the POWER CONTROL stage, and thus the gain of the VGA, to fall.

CW

110. Refer figure 5. In the CW mode, on transmit, a 2kHz square wave signal generated in the microprocessor is fed into the AF/SSB module at 3PL1/6 as 2kHz AUDIO TONE. The audio tone is filtered in the FILTER BUFFER to give a more acceptable audio waveform and fed via the VOGAD OUTPUT ISOLATION stage, which isolates the 2kHz from the input to amplifier 15C, and switches 22B and 22A to the COMMON AUDIO POINT. From this point the process is as already described for voice transmission.

111. During Morse transmission, pressel operation causes the 2kHz tone to be switched on and off within the microprocessor thereby interrupting the transmitter output. (Refer para 99). TX/RX switching is maintained in the TX position until approximately 1.7 seconds have elapsed without a key press. This prevents the PA stages switching on and off at the keying rate which would result in instability and a delay in reaching full power on each key press.

112. In the PA Module during keying in the CW mode, the CW HOLD line to the ALC CR circuit increases the response time of the ALC to prevent the ALC Loop from increasing the gain of VGA during signal gaps.

113. The VOGAD circuit remains switched off when CW mode is selected.

NON HOPPING RADIO ACCESS (NHRA)

114. Refer figure 5. Operation of the HAIL button on the keypad causes the Microprocessor Module RAM I/O TIMERS to produce the 11 second NHRA validation code, an FSK signal, consisting of 1.6kHz and 2.43kHz tones, in a similar manner to the 2kHz modulating tone. The FSK signal is input to Module 3 on the 2kHz Audio Tone line and follows the CW path through the module.

TRANSMIT (Data)

115. When used in the Data mode, audio data fed into the R/T via the VOICE/DATA socket on the front panel enters the AF/SSB module at 3SK7/11. When the pressel is keyed via the VOICE/DATA socket, PRESSEL 2 is activated. TR1/5 is switched by the RX/TX control thus applying 10 Volts to RL1. TR3, which is switched by the VOICE/DATA control, applies an earth to the other end of RL1 thereby energising the relay. The audio data is fed via Amplifier 16C. and switches 22B and 22A to the

COMMON AUDIO POINT. The process is then the same as already described for voice transmission.

116. Audio Data from the Extended Front Panel enters the R/T via the ANCILLARIES socket and is fed onto the AF/SSB module via 3PL6/11 as MIC ANC. The audio data is then fed via Amplifier 16B and switches 22B and 22A to the COMMON AUDIO POINT. Note that PRESSEL 2 is active when the R/T is keyed via The R/T VOICE/DATA socket or the Ancillary input socket. The VOGAD circuit remains switched off.

117. Where the Data mode is selected and an audio accessory (e.g. Handset GP) connected to the R/T VOICE/FILL input is keyed, PRESSEL 1 is activated. The R/T automatically goes to the USB (Voice) mode and the VOGAD circuit is enabled by the VOGAD ON/OFF control. The audio input at the VOICE/FILL socket is fed via the VOGAD circuit, VOGAD OUTPUT ISOLATION circuit and switches 22B and 22A to the COMMON AUDIO POINT. This facility permits the equipment operator to establish voice communication without having to change the mode selected at the R/T front panel.

SIDETONE

Voice

118. Refer Annex A, Figure 1. With the R/T function switch set to LOCAL, REM (Remote) or EXT (External) and with USB or LSB mode selected, operation of the pressel at either of the R/T front panel connectors or via the Ancillaries socket will cause the SQ/NO SQ control output to go high and switch on the ANCILLARY AND REMOTE AMPLIFIER and LOCAL POWER AMPLIFIER via the BIAS CONTROL line. Audio at the COMMON MIC POINT (CMP) will be fed out to the Local, Ancillaries and Remote connectors as follows:

a) **Local Audio.** From the 'CMP' the audio is amplified in Amplifier 16D, fed through switch 10A and the LOCAL POWER AMPLIFIER, to the VOICE/DATA connector on the R/T front panel as Phones 2 via 3SK7/1. The LOCAL POWER AMPLIFIER output is also fed via RL3 in the Normal position, to the VOICE/FILL connector on the R/T front panel as PHONES 1 via 3SK7/3 and 3SK7/9. (Two PHONES 1 lines are required for use in the Fill mode which is described in Para 158)

b) **Ancillary and Remote Audio.** From the 'CMP' the audio is fed via the VOGAD, VOGAD OUTPUT ISOLATION, switches22B and 22A, amplifier 15D and through switch 9A to the SUMMING B stage. The audio is amplified in the AUDIO AMPLIFIER FIXED GAIN and the ANCILLARY AND REMOTE POWER AMPLIFIER and fed out to the Ancillaries and Remote connectors as AUDIO OUT and REMOTE AUDIO respectively.

Data

119. Refer Annex A, Figure 2. With the R/T function switch set to LOCAL or EXT, and with Data mode selected, operation of the pressel at either the R/T front panel VOICE/DATA connector or the Ancillaries connector will activate PRESSEL 2. Audio will be fed through the ANCILLARY AND REMOTE POWER AMPLIFIER and LOCAL POWER AMPLIFIER (which are both switched on via the BIAS CONTROL line, as described in para 118) and out to the Local, Remote and Ancillary connectors as follows:

a) **Local Audio.** Audio (voice or data) entering the R/T via the VOICE/DATA connector is fed onto module 3 via 3SK7/11 and will pass through RL1 and amplifier 16C to switch 22B. Audio (voice or data) from the ancillary connector, is fed to module 3 as MIC ANC, amplified in 16B and passed to switch 22B. From 22B the audio is fed via 22A, amplifier 15D to switches 9A and 9B. The Local audio passes through SUMMING A into the VARIABLE GAIN AMPLIFIER. In the Data mode the gain is set to a fixed level by switch 10B which applies +10 volts to the amplifier bias components. Following further amplification the audio is fed out to the local sockets as described in para 118 (a).

b) **Ancillary and Remote Audio.** This is fed out to the ANCILLARIES and REM terminals as described in para 118 (b).

120. Refer Annex A, Figure 3. With the R/T function switch set to LOCAL or EXT, and with the Data mode selected, operation of the pressel via the R/T front panel VOICE/FILL connector will activate PRESSEL 1. Audio will be fed through the ANCILLARY AND REMOTE AMPLIFIER and LOCAL POWER AMPLIFIER (which are both switched on via the BIAS CONTROL line as described in para 118) and out to the Local, Remote and Ancillaries connectors as follows:

a) **Local, Ancillary and Remote Audios.** From the 'CMP' the Local, Ancillary and Remote Audio are fed out as described in para 118 (a) and (b). Recall that with PRESSEL 1 activated the R/T automatically switches to the USB mode until the pressel is released (Para 117 refers).

CW

121. Refer Annex A, Figure 4 With the R/T function switch set to LOCAL, EXT or REM, and with the mode set to CW, operation of the pressel 'keys' a 2kHz tone within the microprocessor. This tone is fed into the AF/SSB Module via 3PL1/12, sharing the WARNING TONE line. (Warning Tones are covered in paras 223-227 under the BITE Functional description). The sidetone frequency is generated separately from the CW modulating tone to allow the latter to be changed to suit a users particular requirement without the change affecting the sidetone audio, which, at 2kHz, has been found to be ideal for operational use. The 2kHz keyed audio is passed to SUMMING A and SUMMING B and out to the respective sockets and remote terminals via the audio power amplifiers which are both switched on via the BIAS CONTROL line as described in para 118.

REMOTE

Remote Call

122. Refer Figure 10. When the R/T function switch is set to REMOTE a logic 1 is applied to the REMOTE ON line in Module 4, switching on the STABILISED 18V GENERATOR. When the remote operator presses his Call button this generator supplies LINE CURRENT, which is fed out of the R/T via the REMOTE TERMINALS.

123. A current of between 14.5mA and 30mA is drawn through the LINE CURRENT SENSING LOGIC causing the REMOTE CALL line to the microprocessor to fall to logic 0. The microprocessor responds by placing a 2kHz tone on the WARNING TONE line which is then fed through Module 3 to the operators via the ANCILLARY AND REMOTE POWER AMPLIFIER and the LOCAL POWER AMPLIFIER.

124. With the function switch set to the LOCAL position the STABILISED 18V GENERATOR will be switched off. If the remote Call button is now pressed, current will be drawn through the LINE CURRENT SENSING (REMOTE OFF) circuit, causing 10V to be fed to the LINE CURRENT SENSING LOGIC which will set the REMOTE CALL Line to logic 0. The microprocessor sends a 2kHz tone on the WARNING TONE line as described in para 123 above. (Pressing the Call button on the R/T front panel also causes the 2kHz tone to be placed on the WARNING TONE line.)

Receive Mode

125. With the R/T in the receive mode, the TX/RX RELAY CONTROL line is held at logic 0 by the LINE CURRENT SENSING LOGIC. The REMOTE TX/RX RELAY will be de-energised, connecting the output from the R/T audio circuits to the REMOTE TERMINALS via the REMOTE AUDIC line and the isolating transformer.

Remote Pressel

126. When REMOTE is selected and the remote operator presses his transmit key, the current drawn through the LINE CURRENT SENSING LOGIC circuit will be between 8mA and 11mA. This current is too low to cause the the REMOTE CALL line to be activated but the REMOTE PRESSEL line will fall to logic 0, causing the microprocessor to set the R/T to the Tx condition.

127. At the same time TX/RX RELAY CONTROL will rise to logic 1 and energise the REMOTE TX/RX RELAY, connecting the remote operators microphone circuit to the COMMON MIC POINT via the MIC REMOTE line. Sidetone will be routed as shown in Annex A, Figure 5.

INTERCOM

128. With the R/T function switch set to I/C, the microprocessor instructs the CONTROL REGISTER on Module 3 (Figure 5) to place a logic 0 on the INTERCOM MUTE OFF/ON control line. This opens switch 11C, placing a resistor in the receive audio path and thereby attenuating the receive audio output. The SQ/NO SQ control line is set high, switching on the Ancillary/Remote and Local Power Amplifiers via the bias control line. The (B) ANC BYPASS line is also set high, closing switch 9D. In the intercom mode the RX/TX control line remains low even when the pressel is operated.

PRESSEL 1 and PRESSEL 2 Initiated Intercom

129. Refer Annex A, Figure 6. When either PRESSEL 1 or PRESSEL 2 is operated, the VOGAD ON/OFF and SIDETONE OFF/ON control lines are activated, enabling the VOGAD circuit and the path through switch 10A. The intercom audio is routed as follows:

a) **Local Intercom Audio O/P.** From the 'CMP' the audio is fed via amplifier 16D and switch 10A, set to Sidetone On, to the LOCAL POWER AMPLIFIER. The output of the amplifier is fed to the VOICE/DATA connector as PHONES 2, and via RL3 to the VOICE/FILL connector as PHONES 1.

b) **Ancillary and Remote Intercom Audio O/P.** From the 'CMP' the audio is fed via the VOGAD circuit, VOGAD OUTPUT ISOLATION, amplifier 15C and switch 9D to the SUMMING B stage. The audio is amplified in the AUDIO AMPLIFIER FIXED GAIN and the ANCILLARY and REMOTE POWER AMPLIFIER and fed out to the Ancillary and the Remote connectors as Audio Out and Remote Audio respectively.

Remote Initiated Intercom

130. Refer Annex A, Figure 7. With the R/T function switch set to I/C, the microprocessor activates the STABILISED 18V GENERATOR via REMOTE ON. Operation of the remote pressel will cause the LINE CURRENT SENSING LOGIC to output a logic 0 on the REMOTE PRESSEL line and a logic 1 on the TX/RX RELAY CONTROL line. The remote operators microphone will be connected to the CMP (Figure 5) via the MIC REMOTE line. REMOTE PRESSEL will cause the microprocessor to instruct the CONTROL REGISTER to output a high on the (A) ANC BYPASS line, activating switch 9C. The Intercom audio is routed as follows:

a) **Ancillary Intercom Audio.** The audio path is identical to that described at Para 129(b). Note however that the remote operators sidetone is a function of the remote handset.

b) **Local Intercom Audio.** The output of amplifier 15C is also fed, via switch 9C, to the SUMMING A stage and then through the VARIABLE GAIN AUDIO AMPLIFIER and the LOCAL POWER AMPLIFIER. From the amplifier the audio goes, as PHONES 2, via FILTER BOARD Module 6 to the VOICE/DATA connector, and via RL3 in the Normal position, as PHONES 1, through the FILTER BOARD to the VOICE/ FILL connector.

RECEIVE

RF Path

131. Refer Figures 8 & 9. The received signal, at a frequency of between 2MHz and 30MHz, enters the R/T at the ANTENNA TERMINAL or the 50Ω SOCKET and is fed to the PA MODULE via the ATU MODULE and the BAND PASS FILTER MODULE.

132. The signal, appearing at the PA Module (Figure 7) on 11PL6, is fed via RLD/2 and RLD/1 in the de-energised state, through RLA and out of the PA Module, as RX 2-30MHz, to the IF STRIP MODULE.

133. On the IF STRIP (Figure 6) the signal is fed via the INPUT PROTECTION AND LOW PASS FILTER, which guards against high energy pulses from the PA MODULE, and TX RX switch D18/19 to the input of the 1st RX MIXER where it is mixed with the MAIN LO output.

134. The 1st RX MIXER output is amplified and passed via D21/22, D3/4 and the 38MHz FILTER, which removes the unwanted 'sum' component of the mixing process, (Refer Para 12) through switch D5/6 to the 1st IF AMPLIFIER whose gain is controlled by the AGC GENERATOR AND CONTROL CIRCUITS (Paras 139-148 refer).

135. The 1st IF AMPLIFIER output is fed into the 2nd RX MIXER where it is mixed with the 2nd LO input, fed in from the SYNTHESISER via a low pass filter and SWITCHED BUFFER. In the the transmit mode the SWITCHED BUFFER will be turned off by a logic 0 on the TX/RX control line, thereby removing the LO input to the mixer and preventing the production of frequencies which might adversely affect the transmit signal.

136. The output of the 2nd RX Mixer is amplified and fed via switches D7/9 and D8/10 to either the SSB FILTER or the CW FILTER, depending on the mode of operation. With CWN selected, the control signal CW/SSB will be at logic 0 resulting in an output of logic 1 from the LOGIC INVERTER. Switches D8/10, D11/14 will be switched to route the received signal via the CW Filter. In all other modes the received signal will pass via the SSB Filter.

137. After the filters the received signal will be fed via switches D12/15 to the GAIN SET AMPLIFIER which is pre-set, on production and at Base Level, to bring the overall gain of the module within specification.

138. The output of the GAIN SET AMPLIFIER is fed to the 2nd RX IF AMPLIFIER whose gain is controlled by the AGC. The received signal is then fed, via switch D16/17, to the SYNCHRONOUS DEMODULATOR. The reference signal, 1.4 MHz REF, used for the demodulation process is derived from the 5.6 MHz XTAL OSC on Module 9. The audio output from the demodulator is amplified and fed out as RX AUDIO to the ALC AMPLIFIER and the FILTER/CLIPPER on Module 3.

Automatic Gain Control

139. A sample of the received audio is fed into the AGC GENERATOR. The output of the generator, a dc voltage analogue of the audio signal input level, is used to control the gain of the 1st and 2nd IF amplifiers. If the signal output of the receiver increases, the gain of the 1st and 2nd IF Amplifiers is reduced to compensate. AGC MEASURED, a voltage derived from the control output, is fed from the AGC generator, via 7PL7/16, AF/SSB Module 3 and 5PL2/31 to the Analogue to Digital Convertor for input to the microprocessor.

140. Refer Figure 11. The AGC GENERATOR contains two signal detectors. One has a short time constant of, typically, 20ms and rapidly establishes an AGC level to cope with large changes in signal level, such as the onset of a new period of audio traffic. The other detector has a longer time constant (typically 200ms) but gives a larger output for a given change in signal level. It therefore becomes the controlling element once established.

141. During breaks in reception the AGC will be held for approximately 1sec before collapsing to 0V in a time of 200ms. The 1sec hold time is extended when DATA and HOP are selected.

142. Refer Figure 12. These changes to the hold times are controlled by FAST/SLOW AGC and DATA/HOP, fed to the AGC GENERATOR from the Control Registers on the AF/SSB Module. During SSB or CW operation the hold time is set to 1sec by the FAST/SLOW AGC at logic 1 and the DATA/HOP at logic 0. For DATA the signal FAST/SLOW AGC is at logic 0 and DATA/HOP is at logic 1 to give a hold time of approximately 1.33secs. During HOP both signals are at logic 0 producing a hold time of 1.35secs.

143. Channel changes occur at 100ms intervals during frequency hopping and it can be expected that the received signal level will vary markedly from channel to channel. Refer to Figure 13. The decay time of the AGC GENERATOR output is long compared with the channel time, and in cases where a channel with a high signal level is followed immediately by one with a very low signal level, the AGC, operating normally, could not adjust the level of RF gain quickly enough to raise the low channel above the minimum sensitivity level of the following stages. The lower level signal would therefore be lost. For this reason the AGC, during hopping operation, is under microprocessor control.

144 Refer Figure 12. The microprocessor exercises this control by monitoring the level of the AGC control voltage via AGC MEASURED and adjusting the level of AGC PRESET accordingly. AGC PRESET is a voltage applied to the AGC GENERATOR from the DIGITAL TO ANALOGUE CONVERTOR on Module 5.

145. During each 10ms transition period between hopping channels, AGC CONTROL from the I/O Timer on Module 5 energises a switch connecting AGC PRESET to the AGC GENERATOR. This has the effect of resetting the AGC control voltage at the end of each channel reception period to a level determined by the level of AGC PRESET. During the 90ms of reception for each channel the AGC level is allowed to follow the received audio normally.

146. Refer Figure 14. Prior to any signal being received the AGC PRESET is adjusted to a level derived from the noise of the system and this preset is maintained during reception of the first four channels. AGC PRESET will then be set to give an AGC control voltage equal to the level produced by the weakest of the four channels. If four consecutive channels produce AGC levels above, or below, the preset, the microprocessor will alter AGC PRESET to produce a level equal to the AGC control voltage produced by the weakest of these four channels. Should any channel produce an AGC which is below the existing preset, this level will be taken as the new preset. (This is an action of the AGC circuitry; the level of the AGC PRESET line will not alter.) As before, this preset will remain current until four consecutive channels produce AGC levels higher, or lower, than the level demanded by AGC PRESET which will then be set to reflect the level of the weakest of the four channels.

147. The overall effect of this action is that at the beginning of reception of each channel the AGC has been returned to a level from which it can swing down to accommodate the weaker channels notwithstanding the relatively long falling time constant.

148. During the hopping transition period the gain of the 1st IF AMPLIFIER is reduced to zero via the TX MUTE line and RX INHIBIT (TR29) in order to block 'swept band noise'.

AF Path (Voice/CW)

149. The RX AUDIO from the SYNCHRONOUS DEMODULATOR is fed to the ALC AMPLIFIER which provides a constant level of audio output with varying levels of audio applied. The output from the ALC AMPLIFIER is fed to switch 11A which, under the control of the squelch circuits (See para 152), determines whether the audio will be passed to switch 22A directly, or through a high resistance.

150. From 22A the signal is fed to the CLIPPER/NOISE LIMITER via amplifier 15D, switch 25A in the NORM position, 25C in the RX position and 13A in the VOICE position. The CLIPPER/NOISE LIMITER removes noise spikes and high amplitude interference peaks. The level at which clipping occurs is set by the ALC CIRCUIT via the CLIPPER CONTROL line.

151. The signal is then fed through switch 13B and switch 11C to the SUMMING A and SUMMING B networks and then to the local, ancillary and remote outputs as described in para 129 (a) and (b).

Squelch (Voice)

152. The incoming signal RX AUDIO is filtered and clipped before input to the SQUELCH CONTROL DETECTOR which determines whether the signal is composed of noise or audio frequencies. The audio/noise level at which the squelch will operate is determined by the setting of the SQUELCH control on the R/T front panel. The output of the detector is a control to switch 11D which , if the signal has been judged to be audio, applies +10V to Switch 11A, shorting out the resistance in the audio path and permitting the RX Audio to pass directly to switch 22A; otherwise the resistance is included in the path and the received signal greatly attenuated. The +10V from switch 11A also, as BIAS CONTROL, enables the ANCILLARY AND REMOTE POWER AMPLIFIER and the LOCAL POWER AMPLIFIER.

153. The control voltage from the SQUELCH control is monitored by the microprocessor via SQUELCH MEASURED. If the control wiper is set to the 'OFF' position, 0V is fed to the microprocessor which instructs the control registers to set a high level on the SQ/NO SQ control signal. This control overrides the operation of the SQUELCH CONTROL DETECTOR and operates switch 11A to exclude the squelch resistance from the audio path and enable the audio power amplifiers.

Squelch (CW)

154. Because of the detection method used within the SQUELCH CONTROL DETECTOR the characteristics of a CW signal will result in it being classified as noise and, if not prevented, the squelch circuits will inhibit the audio path (See para 152). When a CW mode is selected therefore, the microprocessor causes the SQ/NO SQ control line to be set high, overriding the output of the squelch circuit and maintaining 'no squelch' operation.

AF Path (Data)

155. During Data operations the microprocessor outputs two signals, via the AF/SSB Module CONTROL REGISTER, to modify the received path as follows:-

a. A logic 1 output on the HOP/DATA line, applied to the ALC Amplifier, reduces the ALC time constant.

b. A logic 1 output on the VOICE/DATA line, applied to switches 13A and 13B, by-passing the Clipper/Noise Limiter.

156. The squelch circuits are disabled as described in para 154.

AF Path (Hopping)

157. During Hopping operations the received path is modified as follows under microprocessor control :-

a. A logic 1 output on the HOP/DATA line, applied to the ALC Amplifier, reduces the ALC time constant.

b. A logic 1 output on the NORM/HOP line, applied to switch 25A. The modified signal path is now from amplifiers 15D and 15A to the Unprocessed Audio Output at 3PL6/4 to the Hopper. The signal from the Hopper, Processed Audio at 3PL6/10, is fed via amplifier 15B and switch 25A to the Summing A and Summing B circuits via a common audio path.

158. The squelch circuits are again disabled as stated in para 154.

FILL INPUT

159. For the entry of FILL data into the R/T, the microprocessor sets control signal NORM/FILL from the control register to a high. This energises relays RL2 and RL3 so that the PHONES 1/DATA inputs, from the VOICE/DATA connector on the R/T front panel, are connected to the 2.4kB data link to the microprocessor.

MICROPROCESSOR CONTROL

Control Functions

160. Refer Figure 15. Control of the R/T is exercised via the Microprocessor Module. The processor executes operational program instructions held in ROM (Read Only Memory) using working data held in RAM (Random Access Memory). Data is transferred over an 8 bit data bus and addressing is via a 16 bit bus.

161. The purpose and relationship of individual signals to and from the module are dealt with at relevant points in the functional descriptions of the Tx and Rx paths, but Keypad instructions can be taken as an example. Information relating to key presses is input from the front panel via KEYPAD DATA on 5PL1/29. The microprocessor, under the control of the program in ROM, extracts from RAM the data necessary for the execution of the instruction and produces appropriate outputs on COMMON DATA

(5PL1/18) and AF DATA (5PL2/13). The DATA signals are applied to Control Registers on other modules. (These are the AF/SSB Module and the ATU, BPF and PA Modules for AF DATA and COMMON DATA respectively.)

162. The microprocessor produces an individual STROBE signal for each Control Register. COMMON DATA can thus carry data for any one of the ATU, BPF and PA Modules, with the Register for which the data is intended being 'opened' for data transfer by setting the appropriate strobe signal high.

Inter-module Digital signals

163. AF DATA and COMMON DATA, with their associated strobes, are passed through the RAM INPUT/OUTPUT TIMERS, as are the majority of digital inputs and outputs between Module 5 and other R/T modules.

Inter-Equipment Digital Signals

164. Inter-Equipment Digital Signals are passed through the RAM INPUT/OUTPUT TIMERS and the open collector SOURCE INTERFACE and LOAD INTERFACE as appropriate. (Outputs from the microprocessor are sent via the Source I/F and Input from the peripheral equipments via the Load I/F.)

Inter-module Analogue Signals

165. Some signals, e.g. AGC MEASURED from the AGC Generator (Module 7), are analogue representations of levels at various points within the unit. These are converted by the ANALOGUE TO DIGITAL CONVERTER (ADC) to digital form for input to the microprocessor.

166. The reverse process is carried out by the DIGITAL TO ANALOGUE CONVERTER (DAC) in the case of ANALOGUE SETTINGS, the control for the AGC Generator on Module 7.

Pressel

167. The three Pressel lines (PRESSEL 1, PRESSEL 2 and REMOTE PRESSEL) are fed to the INTERRUPT line of the microprocessor. A low on any of the PRESSEL lines will interrupt the microprocessor which will, via the RAM INPUT/OUTPUT TIMERS, set the TX/RX lines on 5PL1/25 and 5PL1/23 high, indicating the transmit condition to the other modules.

168. PRESSEL 1 is used when the R/T is set to LOCAL and keyed via the VOICE/FILL socket on the R/T front panel. It is fed via 6PL3/7, 3SK7/6, 3PL1/5 and 5PL2/28 to the microprocessor.

169. PRESSEL 2 is used when,

a. the R/T is set to LOCAL and keyed via the VOICE/DATA socket. It is fed via 6PL3/8, 3SK7/5, 3PL1/10 and 5PL3/8 to the microprocessor.

b. the R/T is set to EXT and the EFP is connected to the ANCILLARIES socket. It is fed via 4PL1/1, 4PL3/10, 3PL1/9, 3PL1/10 and 5PL3/8 to the microprocessor.

170. REMOTE PRESSEL, fed from the Remote Control Module 4, via 4PL3/3 and 5PL3/3, is used when the R/T is set to REMOTE or I/C and keyed via the remote terminals. (Refer Paras 122-130).

Serial Data Links

171. Serial data messages are exchanged between the HF R/T and other equipments on two balanced line data links operating at 2.4 kBd and 9.6 kBd respectively. On each link a Universal Asynchronous Receiver/Transmitter (UART) provides control of the message format and exchange protocols and also the interfacing between the serial message link and the parallel data bus to the microprocessor.

172 The 2.4 kBd link is used to communicate with ancillary equipments sited up to a maximum of 15 metres from the R/T (eg. the EFP). The input and output lines from and to Module 5 are fed via 5PL3/9 (DATA +VE 2.4kB) and 5PL3/7 (DATA -VE 2.4kB) to 3PL6/2 and 3PL6/12 on the AF/SSB Board, Module 3 (See Figure 5). In normal operation the path through Module 3 is via relay RL2 to 3PL6/1 (DATA +VE) and 3PL6/8 (DATA -VE) and then to Module 4 on 4PL6/4 and 4PL6/8 (See Figure10). On Module 4 the lines pass through RFI filtering circuits and exit on 4PL1/10 and 4PL1/14 to the ANCILLARIES CONNECTOR on the R/T rear panel.

173. The 9.6 kBd interface is used to communicate with equipments (eg. FHU) which require a higher rate of data exchange. The higher baud rate introduces bandwidth considerations which limit the length of cable that can be employed between equipments. Between the R/T and the FHU this is approximately 300mm. The 9.6 kBd interface lines from/to Module 5 are fed via 5PL3/11 (DATA +VE) and 5PL3/5 (DATA -VE), to 4PL3/4 and 4PL3/14 on Module 4, through RFI filtering and then, via 4PL1/7 and 4PL1/12, to the ANCILLARIES CONNECTOR on the R/T rear panel.

System Clock

174. The microprocessor timing is controlled by 5.6 MHZ µP CLOCK produced on the Synthesiser Board, Module 9 and fed out at 9aSK5 for input to Module 5 at 5SK5.

175. The 2.8 MHz output from the microprocessor is input to Frequency Divider circuits which produce a 1.4 MHz clock, for distribution to the 9.6 kBd and 2.4 kBd UARTs, and a 700kHz clock for output to other R/T functions as follows:

a. The AF CLOCK, output via 5PL2/24 and 3PL1/2 for use by the Control Registers on Module 3.

b. The SYNTH CLOCK, output via 5PL2/10 and input to Module 9 on 9aPL1/3 for use by the Control Register.

c. The COMMON CLOCK, output on 5PL1/14 is fed to Module 12 on 12PL4/1 for use by the ATU Control Registers. (From Module 12 the clock is distributed to Modules 10 and 11).

176. The 2.8 MHz clock pulses are also applied to the divider circuits in the RAM INPUT/OUTPUT TIMERS for the production of tones e.g. CW TONE and WARNING TONE for output to the AF/SSB Module.

Initial Switch On

177. When the R/T is initially switched on the +5V applied to 5PL1/2, from the PSU Module 2 (2PL7/4), is fed to the POWER UP RESET circuit. The output of the POWER UP RESET holds the RESET input to the microprocessor at 0V preventing normal processor action until the supply has stabilised. After approximately 200ms the POWER UP RESET will release the microprocessor RESET input permitting normal processor action to commence.

Low Battery Warning

178. The +24V input supply is fed to Module 5 on 5PL2/3. It is monitored by the LOW VOLTS (+19V) DETECTOR which uses the +5V regulated supply fed in from the PSU Module 2 (5PL1/2) as a reference. If the +24V supply falls below approximately +19V the detector output to the RAM I/O Timer goes high (+5V). The microprocessor then sends data, via the RAM I/O, on DISPLAY DATA (5PL1/6) to generate a LOW BATT indication on the Display, Module 8. At the same time a WARNING TONE of 300Hz pips is fed from the RAM I/O Timer, via 5PL2/25 and 3PL1/12, to the AF/SSB Board, Module 3, for output to the operators earphones.

Microprocessor Power Down

179. The +24V input supply is also fed to the LOW VOLTS (+13.5V) DETECTOR . If the input supply falls below approximately +13.5V the detector output to the RAM I/O TIMERS goes low. This warning enables the microprocessor to carry out the power-down routine before complete collapse of the supply.

Microprocessor Reset

180. The low output at the LOW VOLTS (+13.5V) DETECTOR is also fed to the POWER UP RESET circuit. The POWER UP RESET circuit applies a low to the RESET input of the microprocessor preventing normal processor action.

181. When the supply again rises above the threshold of the LOW VOLTS (+13.5V) DETECTOR its output goes high but the POWER UP RESET circuit does not release the processor until the incidence of a signal from the ENABLE circuit. This signal, derived from the 2.8MHz clock, occurs 1.5 seconds after the output of the LOW VOLTS (+13.5V) DETECTOR goes high giving the power supplies time to stabilise. The processor then resumes normal operation.

Memory Battery and Erase

182. The power supply to the RAM on the Microprocessor Module is derived from one of three sources, a 5.1V REGULATOR supplied by +24V UNSWITCHED on 5PL2/1, the +5V supply from Module 2, via 5PL1/2, or a 3V supply derived from a separate battery (MEMORY BATTERY) attached to the inside of the R/T top cover and connected to the module at 5PL4/1. The UNSWITCHED supply maintains the RAM and its contents, the FILL data, when the equipment is switched off. The 5V from Module 2 is the operational

supply and the 3V battery supply maintains the RAM during periods when neither of the other supplies are available.

183. The supplies are fed to the BATTERY ISOLATION circuit whose output, +V MEM, is applied to the RAM circuits. The Memory Battery will be isolated from the RAM circuit, by the BATTERY ISOLATION circuit, when +24V is applied to the R/T either by a manpack battery or vehicle supply. If the +24V is removed from the module the BATTERY ISOLATION circuit will connect the Memory Battery (+3V) to the RAM. The Memory Battery can not be switched off.

184. Erasure of the RAM memory contents occurs when the ERASE position is selected on the R/T front panel switches. The output of the BATTERY ISOLATION circuit is pulled to 0V via 5PL1/28 thus removing the power supply to the RAM circuits and destroying the memory contents. During this process it is possible that the +5V supply from the PSU Module 2 will be overloaded. To overcome this problem the 0V on the ERASE line is applied to the 5V INHIBIT circuit. This produces a +5V INHIBIT output which is fed, via 5PL1/20 and 2PL7/1, to the +5V REGULATOR CONTROL on PSU Module 2 switching off the +5V SERIES REGULATOR.

FRONT PANEL DISPLAY AND CONTROLS (Refer to Figure 16)

Keypad

185. The 15 key switches are connected as parallel inputs to the PARALLEL IN SERIAL OUT REGISTER (PISO). All inputs are held high (logic 1) until a key is pressed pulling the appropriate line down to 0V.

186. When the KEYPAD STROBE line, on 14PL1/4, is set high by the microprocessor, the PISO is opened for input from the 15 keypad lines. If a key is pressed during this time a logic 0 will be input to the appropriate stage of the register. Stages representing the other keys will remain at logic 1.

187. When the KEYPAD STROBE line is set to logic 0 the KEYPAD CLOCK, 14PL1/3, will clock the contents of the register out as a serial data word to the microprocessor, via the KEYPAD DATA line 14PL1/2. The microprocessor will interpret the data and send appropriate instructions to other modules on its' DATA outputs. An all 1's data word from the PISO would be interpreted as no change to the keypad and no action would be taken.

188. The intervals at which the KEYPAD is interrogated depends on the microprocessor workload but will be between 1 - 3msecs.

189. The KEYPAD ASSEMBLY is supplied with KEYPAD +10V, via 14PL1/6, and KEYPAD +5V, via 14PL1/5. Both supplies are fed from the Microprocessor Module 5.

190. Refer to para 194 for an explanation of KEYPAD BACKLIGHTING.

Display

191. Display data from the microprocessor is input to the SERIAL IN PARALLEL OUT REGISTERS on the DISPLAY DATA line, via 6PL1/5. The data is clocked into the

registers by the DISPLAY CLOCK appearing at 8PL1/4. The output from the registers, in parallel form, is fed out to the DRIVER/LATCHES. The parallel data is output to the LIQUID CRYSTAL DISPLAY when DISPLAY STROBE, from the microprocessor, goes high.

192. The DISPLAY ASSEMBLY is supplied with DISPLAY 5V PROTECTED, via 8PL1/6, and DISPLAY 5V, via 8PL1/7. Both supplies are fed from the Microprocessor Module 5.

193. Refer to para 194 for an explanation of DISPLAY BACKLIGHTING.

Keypad and Display Backlighting

194. Backlighting for the KEYPAD and DISPLAY is initiated by pressing the key marked LIGHT/PWR twice. The keypad data is sent to the microprocessor which outputs a 0V on KEYPAD ILLUMINATION,14PL1/7, and DISPLAY ILLUMINATION, 8PL1/5, switching on the illumination. The illumination will remain on for twelve seconds and holding the key down does not extend the ON time.

195. Power for the KEYPAD ILLUMINATION is supplied from KEYPAD 10V and the DISPLAY ILLUMINATION is supplied from DISPLAY 5V.

Mode Switch and 50Ω/Erase/Ant Switch

196. The MODE SWITCH is a two part, seven position switch controlling the functional mode of the R/T. There are six switchable positions OFF, LOCAL, EXT, TEST, REM and I/C. In the seventh position, ERASE, the switch is spring-biassed and ERASE is selected only while the switch is held against the spring.

197. The +24V VEHICLE or MANPACK BATTERY supply is fed, via relay RLA and 2PL7/9 on PSU Module 2, to the MODE SWITCH,1S2a, as 24V UNSWITCHED. With the MODE SWITCH in any position other than OFF the +24V will be switched to the PSU Module 2, as 24V SWITCHED, via 2PL7/3, for distribution around the R/T.

198. The R/T mode of operation is set by the MODE SWITCH 1S2b. 0V from the Microprocessor Module is fed to the switch via 5PL2/12. With the switch set to LOCAL, EXT, TEST, REM or I/C the 0V (logic 0) is returned to Module 5 on the appropriate input line of the RAM INPUT/OUTPUT TIMER and thus to the microprocessor for implementation of the mode indicated.

199. The 50Ω/ERASE/ANT SWITCH is a three position switch spring-biassed against selection of the ERASE position. With the switch set to 50Ω the 0V from 5PL2/12 is applied to the ANT/50Ω output to the Microprocessor Module. The microprocessor sends instructions to the ATU Mocule to switch RELAY A to the 50Ω position. With the 50Ω/ERASE/ANT SWITCH set to ANT the ANT/50Ω output returns to +5V (logic 1). The microprocessor will then instruct the ATU Module to switch RELAY A to the antenna position.

200. To erase information from the RAM on the Microprocessor Module, both the MODE and 50Ω/ERASE/ANT switches must be held in the ERASE position for a minimum of one second. In this position the 0V on 5PL2/12 is fed to 5PL1/28. Erasure

of the memory is described in para 184. When released, the MODE SWITCH will return to the I/C position and the 50Ω/ERASE/ANT SWITCH will return to the ANT position.

Squelch and Volume Controls

201. The functions of the SQUELCH and VOLUME CONTROLS have been described during the analysis of the AF/SSB Module 3. The controls are provided with 10V from the AF/SSB Module 3 via 3PL4/2 and 3PL4/6. A proportion of the 10V, corresponding to the position of the wipers, is fed out to the SQUELCH CONTROL DETECTOR, via 3PL4/3, and the VARIABLE GAIN AUDIO AMPLIFIER, via 3PL4/4.

FREQUENCY SYNTHESIS (Refer Figure 17)

202. **Synthesiser Outputs.** Module 9, the Synthesiser Module, produces the Main Local Oscillator and 2nd Local Oscillator frequencies and three 5.6MHz outputs. The Local Oscillator outputs, MAIN LO and 2nd LO, are sent to the IF STRIP Module. The other outputs, 5.6MHz AF/SSB REFERENCE, µP CLOCK and 5.6MHz BUFFERED are produced by the 5.6MHz crystal oscillator on board 9b and sent to Module 3, Module 5 and the rear panel 5.6MHZ STD output respectively.

203. **Main Local Oscillator.** The MAIN LO, is made up of two Voltage Controlled Oscillators (VCO) which together cover the required 40-68MHz range. The respective ranges of the VCOs are actually 39.9975 to 51.8424MHz and 51.8375 to 68.0024MHz and frequency is changed in steps of 100Hz.

204. **Control Data Transfer.** When a frequency change is initiated, via the front panel keypad or as part of frequency hopping operation, the microprocessor sends instructions to the CONTROL REGISTER on board 9b via SYNTH DATA. Data is transferred under the control of SYNTH STROBE and is clocked into the register by SYNTH CLOCK.

205. **VCO Select.** One of the control lines from the register operates a VCO SELECT circuit which switches in the appropriate VCO for the range in which the required frequency lies.

206. **VCO Control.** A second control line sets the division factor of a progammable frequency divider, PROG. DIV.(a), in the VCO control loop. The division factor set for PROG. DIV.(a) is such that, at the required LO output frequency, its output will be 100KHz. The output of the divider is fed to a phase comparator (PHASE COMP.) whose other input is a 100KHz signal derived by passing the output of 5.6MHz crystal controlled oscillator (5.6MHz XTAL OSC.) through a divide by 56 circuit (÷56). The output of the comparator is an analogue of the difference between the actual LO output and the required frequency and is applied as the control voltage to the VCO which adjusts accordingly. When the VCO output reaches the required frequency, both inputs to the comparator will be the same and no further change will take place.

207. **Control Loop Response Time.** During normal operation the LO is required to be brought into lock within 0.3 seconds. During frequency hopping operation the VCO control loop response time is reduced to 5ms by the MODE SELECT control line.

This accommodates the rapid (one per 100ms) frequency changes in this mode. Tuning can be accomplished in the shorter time because of the restricted frequency range over which changes will occur during hopping.

208. **2nd Local Oscillator.** The 2nd LO, on board 9a, works on a similar principle but is only required to produce one of two frequencies, 36.6MHz or 39.4MHz, for USB/ CW and LSB operation respectively. The control line, 2nd LO SELECT, sets the division factor of PROG. DIV. (b) to produce 20KHz at the correct LO output frequency. The control levels are logic 1 for USB/CW and logic 0 for LSB. Control for the VCO is derived by comparison of the divider output with a reference obtained from 100KHz REF fed in from board 9b.

209. **Failure to Lock.** When both inputs to the phase comparator are the same, 2nd LO PHASE LOCK ACHIEVED, to board 9b, is set to a logic 1. This is applied to an AND gate, the other input of which is a similar output from the Main LO comparator. If either, or both inputs to the gate are logic 0, indicating the LO out of lock, the output of the gate, SYN[redacted] FAULT, which is applied to the microprocessor, is set to 0. During normal operation if SYN[redacted] FAULT remains at 0 for longer than 0.3 seconds after the initiation of a frequency change, the microprocessor will activate a 300 Hz WARNING TONE signal to Module 3. The tone will be fed to the phones to alert the operator. The microprocessor will also initiate a 'SYN[redacted] FAIL' display.

210. **PSU Switching Frequency.** The switching frequency, or its harmonics, of the main power supply on Module 2 can cause interference with the operational frequency of the R/T. The microprocessor decides which of two possible switching frequencies will avoid interference at the selected operational frequency and, via the CONTROL REGISTER, sets the division factor of a programmed frequency divider, PROG. DIV.(c), to which the 5.6MHz reference is applied. The output of the divider, PSU CLOCK SYNC, is fed to Module 2 at a frequency of either 25.112KHz or 25.225KHz to become the reference for the power supply switching rate.

DC Supplies

211. Module 2 supplies +24V SWITCHED, +10V, +6V and +5V to board 9b. The +6V, +10V and +24V input are passed on to board 9a.

80v dc Generation

212. The Main Local Oscillator VCO CONTROL circuit operates from an 80V dc supply derived from 24V SWITCHED supplied by Module 2. The 80V DC GENERATOR is a switched mode circuit the switching control of which is provided by 100KHz REF. The generator incorporates self regulation and over current protection with further protection being provided by a 110V LIMIT circuit on its output.

MAIN POWER SUPPLY (Refer Figure 18)

213. The POWER SUPPLY module, Module 2, provides +24V, +10V, +6V and +5V dc supply rails for other modules within the R/T and, in the case of the +24V, for ancillary equipment. It also provides an 'R/T Power On' signal for other system equipments.

Supply Inputs

214. The nominal 24V dc supply to the PSU Module can be derived from a manpack battery attached the R/T or from a vehicle supply. The MANPACK BATTERY supply is input via the BATTERY FILTER, MODULE 13 and its positive line is fed through FS3 on the FUSEBOARD, Module 15, to SK2 on Module 2. The 26V VEHICLE CONDITIONED SUPPLY is input at the rear panel DC POWER plug 1PL. Pins A and D carry the +VE and -VE lines respectively. VEHICLE SUPPLY +VE is fused (FS1) and input to Module 2 on 2SK1. The negative lines of both supplies are commoned on Module 2 and fed back to chassis via FS2 on the FUSEBOARD. FS2 in the -VE line provides protection for the supply source where the equipment chassis is in contact with the -VE supply line (eg. Vehicle installation). If the +VE supply line is applied to the -VE terminal on the R/T, FS2 will blow preventing any damage to the supply and associated connectors.

+24V Supplies

215. The vehicle supply is self selecting by virtue of the operation of RLA whose coil is in series with it. With a vehicle supply connected the relay is energised and the output of the relay, 24V UNSWITCHED is therefore derived from VEHICLE SUPPLY +VE. With no vehicle supply present the relay is de-energised and 24V UNSWITCHED is derived from the battery supply.

216. The 24V UNSWITCHED supply is fed out to Module 5, Module 11 and to the FRONT PANEL MODE SWITCH. In any switch position other than 'OFF' the supply is returned as 24V SWITCHED. The switched supply is fed out to Modules, 4, 5, 9 and 10 and 15. From Module 15 after passing through FS4 it is returned to Module 2 as +24V SWITCHED (750mA) and then fed out on 2SK9/4 and 2SK10/2.

+10V Supply

217. Within the PSU Module 24V SWITCHED is applied to the +10V SERIES REGULATOR, a switching regulator whose operation is controlled by a feed back loop through the VOLTAGE PRESET and REGULATOR CONTROL circuits. The switching frequency is controlled by PSU CLOCK SYNC, from the Synthesiser Module, applied to the REGULATOR CONTROL via a PHASE LOCKED LOOP circuit. The PHASE LOCKED LOOP produces an output at a nominal 100KHz referenced to PSU CLOCK SYNC which is nominally 25KHz but will in actuality be either 25.112KHz or 25.225KHz (See para 210).

218. The output is passed through a CURRENT SENSOR circuit which inhibits the REGULATOR CONTROL circuit, and therefore the supply, should excess current be drawn. From the CURRENT SENSOR the supply is passed via lowpass filtering, to remove noise spikes, and a 12V limiter circuit to provide the +10V supply to Modules 3, 4, 5, 9 and 10 .

+5V and +6V Supplies

219. The +10V SERIES REGULATOR output also supplies the +5V SERIES REGULATOR and 6.2V SERIES REGULATOR. These are also switching regulators referenced to PSU CLOCK SYNC.

220. The 5V and 6.2V regulator outputs are also passed through lowpass filtering and are limited to 6.2V and 7.2V respectively.

221. A 5V INHIBIT from the Microprocessor Module switches off the +5V regulator to prevent overload during ERASE operations.

222. TX/RX from the Microprocessor Module goes to a 'High' when the R/T is switched to the transmit mode. This enables the output of +6.2V as 6V TX to Module 11 and Module 3 respectively.

Supply Indicators

223. LED indicators and test switches, S1 & S2, provide on board BITE indications of individual supply availability. When S1 is pressed the LED associated with each available supply, except the 6V TX, is illuminated via the SUPPLY TEST CIRCUIT. With S2 also pressed the 6V TX supply is brought on line and thus illuminates D9.

'SYSTEM ON'

224. The +10V supply rail is also fed out as SYSTEM ON to the REMOTE CONTROL Module and from there, via the AUTO CONTROL CONNECTOR, to other system equipments to indicate the 'Power On' status of the R/T.

BUILT IN TEST EQUIPMENT (BITE)

225. During normal R/T operation BITE circuits provide continuous monitoring of synthesiser lock condition, VSWR and dc supply voltages. In the event of a fault occurring an audio tone is generated and the fault condition indicated on the display. In addition, two separate levels of operator initiated BITE test programs can be run. Note that audio warnings will only occur whilst in receive mode.

Continuous BITE

226. Figure 19 shows the functional elements associated with the BITE circuits.

227. The MAIN LO LOCK ACHIEVED and 2nd LO LOCK ACHIEVED lines will be at logic 1 when the respective oscillators achieve lock. With both inputs to the AND gate at logic 1 the output to the microprocessor, SYNTH FAULT, will be high indicating no fault. If either oscillator fails to lock the SYNTH FAULT line will be at logic 0 and the microprocessor will initiate the following visual and audio warnings :-

a. NO LOCK' will be displayed on the Liquid Crystal Display (LCD).

b. A 300Hz continuous tone will be sent from the microprocessor, via the WARNING TONE line and audio circuits to the operator.

228. During transmitter operation the VSWR is continuously monitored as described in paras 96-98. If a VSWR fault occurs the microprocessor will initiate the following visual and audio warnings :-

a. 'BAD VSWR' will be displayed on the Liquid Crystal Display (LCD).

b. A 300Hz interrupted tone via the WARNING TONE line and audio circuits to the operator.

229. The microprocessor continuously monitors the +15V, +10V and MEM BATT +VE lines via the ANALOGUE TO DIGITAL CONVERTER. The +24V is also monitored as described in para 178. If a low voltage is detected the microprocessor will initiate the following visual and audio warnings :-

a. 'LOW BATT' will be displayed on the LCD.

b. A 300Hz interrupted tone via the WARNING TONE line and audio circuits to the operator.

Operator Initiated BITE

230. The operator initiates a BITE routine by setting the R/T Mode switch (1S2) to the TEST position which applies '0V' to the TEST input line of the Microprocessor. The front panel LCD will then display '0 OR 1'. To select the high level test (UNIT BITE), '0' is pressed on the keypad. For the low level test (MODULE BITE), '1' is pressed. If, during the operator initiated BITE routine a fault is detected, the sequence will be aborted and the failure indicated to the operator via the LCD.

231. The eight test routines employed during 'Level 1' operator initiated BITE are listed below. During receiver tests the R/T is automatically set to CW and tuned to a frequency of 10.5MHz. For transmitter testing the R/T is automatically set to CW power level 5 and uses the frequency selected by the operator prior to the initiation of the BITE routine. [Note: During 'Level 0' BITE only Receiver IF and ATU Output are used.]

Synthesiser

232. The synthesiser test checks that the MAIN LO achieves lock within the time specification.

233. The 2nd LO is set to 39.4MHz (USB) and the Main LO set to produce an output frequency of 2.0MHz. The Main LO is then changed to produce an output frequency of 29.9999MHz and the SYNTH FAULT line examined after 0.3 secs. If the SYNTH FAULT line is low the microprocessor will instruct the LCD to display 'SYN FAIL'; otherwise the Main LO is changed to produce an output frequency of 29.4999MHz and the SYNTH FAULT line examined 5ms later. 'SYN FAIL' will be displayed if a fault is apparent. If the tests are satisfactory the R/T is reset to 10.4998MHz.

Receiver IF

234. The receiver IF test checks basic performance by applying the output of a fixed frequency crystal oscillator (BITE OSCILLATOR) to the receive path at the first mixer stage. AGC is monitored to gauge the level of output from the IF stage.

235. For the RX IF test the BITE OSC INHIBIT is de-activated and the output of the BITE OSCILLATOR, at a frequency of 10.5MHz, is fed into the TX/RX IF AMPS AND MIXERS. The 10.5MHz is mixed with the MAIN LO and 2nd LO outputs, demodulated

by the RX DEMODULATOR and fed to the AGC GENERATOR. A voltage proportional to the signal level, derived from the AGC GENERATOR, is sent to the microprocessor board as AGC (MEASURED).

236. 'RX FAIL' will be displayed if the voltage measured is less than 1V. If the voltage is greater than 1V, a second measurement is made with the BITE OSCILLATOR switched off. The voltage measured for this test should be less than 0.68V otherwise 'RX FAIL' will be displayed.

AF Squelch

237. The AF squelch system is tested by pre-setting the squelch control threshold and providing received AF at two different audio frequencies. The performance is assessed by monitoring the SQUELCH BITE line which reflects the squelch status.

238. The SQUELCH DETECTOR is set to maximum squelch by the microprocessor applying +5V to the ANALOGUE SETTINGS line. The BITE OSCILLATOR is activated and the R/T set to a frequency of 10.4998MHz in the CW mode. This produces an AF of 200Hz at the SQUELCH DETECTOR. If the SQUELCH BITE line to the microprocessor is low, indicating that the squelch has not been lifted, 'AF FAILR' will be displayed. If the squelch BITE line is high, a second measurement is made with the R/T frequency set to 10.5103MHz to give a frequency of 10.3kHz at the SQUELCH DETECTOR. This time 'AF FAILR' will be displayed if the squelch BITE line is high indicating that the squelch had been lifted inappropriately.

Transmitter AF

239. This test checks the function of the SSB GENERATOR by applying its output to the RX DEMODULATOR and monitoring the AGC MEASURED line.

240. The 2kHz CW Tone is mixed with 1.4MHz within the SSB GENERATOR and the resulting output is fed, via the AF BITE ON/OFF switch in the energised position, as BITE FEEDBACK to the RX DEMODULATOR. The output of the RX DEMODULATOR is fed to the AGC GENERATOR whose output, AGC MEASURED, is fed to the microprocessor as AGC (MEASURED).

241. 'AF FAILT' will be displayed if the voltage measured is less than 1.5V. If the voltage exceeds 1.5V, a second measurement is made with the 2kHz CW Tone switched off. The voltage measured for this test should be less than 0.7V and 'AF FAILT' will be displayed where the voltage exceeds this level.

Transmit IF

242. This test checks the level of the transmitter RF drive present at the input to the POWER AMPLIFIERS, thereby testing the IF strip transmit circuits.

243. The 2kHz CW Tone is mixed with 1.4MHz within the SSB GENERATOR and output as 1.4MHz TX, via the AF BITE ON/OFF switch in the de-energised position, to the input of the TX/RX IF AMPS AND MIXERS. This signal is mixed with the local oscillator outputs and fed, via the POWER AMPLIFIERS, BAND PASS FILTERS and ATU IMPEDANCE MATCHING to the antenna. The output of the TX/RX IF

AMPLIFIERS AND MIXERS is detected on the PA Module. The output of the detector is fed, via the IF O/P BITE and BITE O/P switches, to the microprocessor as BITE PA.

244. 'IF FAIL' will be displayed if the voltage is less than 1V, indicating low RF drive. If the voltage exceeds 1V, a second measurement is made with the 2kHz CW Tone switched off. A voltage greater than 0.5V indicating the possible presence of noise will result in 'IF FAIL' being displayed.

PA

245. This test measures the output voltage of the POWER AMPLIFIERS.

246. The output from the Power Amplifier detected on PA Module is fed, via PA O/P BITE and BITE O/P, to the microprocessor as BITE PA.

247. 'PA FAIL' will be displayed if the voltage measured is less than 2.5V indicating low PA output. If the voltage exceeds 2.5V, a second measurement is made with the 2kHz CW Tone switched off. The voltage measured for this test should be less than 1V. 'PA FAIL' will be displayed where the voltage exceeds 1V.

BPF

248. The continuity of the Band Pass Filter in circuit during the test is assessed by reading the output of the FORWARD POWER DETECTOR. (The filter in circuit is determined by the frequency selected by the operator prior to test initiation.)

249. The output of the Band Pass Filter is detected by the FORWARD AND REVERSE POWER DETECTORS on ATU Module 12. The output of the detector, V FWD, is fed, via BPF O/P BITE and BITE O/P, to the microprocessor as BITE PA.

250. 'BPF FAIL' will be displayed if the voltage measured is less than 2V. If the voltage exceeds 2V, a second measurement is made with the POWER AMPLIFIERS muted. The voltage measured for this test should be less than 1V. 'BPF FAIL' will be displayed where the voltage does exceed 1V.

ATU Output

251. This test uses the VSWR COMPARATOR to check that the ATU is correctly tuned to the load. Refer Para 92.

252. 'ATU FAIL' will be displayed if the VSWR Monitor line is high.

SYSTEM CONTROLS FOR THE HF CSS

253. The main component equipments of the HF CSS are interactive, with the R/T F-100 acting as the control centre of the system.

254. Control signals, and in some cases the dc supply, are carried between equipments on a 19 way cable connected to the AUTO CONTROL socket on the rear panel of the R/T. Each equipment forwards the controls to the next in line.

255. The Frequency Hopper is an exception to this, being connected to the ANCILLARIES socket and having a different functional relationship with the R/T to that of the Co-Site Filter, High Power Amplifier, or Antenna Tuning Unit which are all in the external rf signal path to the antenna.

256. The output and input circuits for each signal are open collector source and load circuits respectively. A summary of open collector logic is given at Annex C.

257. The designation of the lines within the 19 way control cable presents some difficulty since the use of a particular line may change depending on the system configuration being operated. Figure 20 shows the possible configurations and also illustrates changes in signal name using the READY signal as an example. Pin connections are shown in Annex B, Table 1 and the use of the controls is explained in the following paragraphs.

258. SYSTEM ON becomes active (+10V) when the R/T is switched on. It enables the activation of the other equipments.

259. RESET is a pulse output (0V) from the R/T. It is issued as follows:

a. On switch on.

b. On each frequency change greater than 1KHz, for frequencies below 3MHz, and greater than 10KHz for frequencies above 3MHz.

c. When the front panel antenna switch is set to 50 ohms.

d. On each Tx/Rx transition during 2FS operation.

e. When the CSF PRESENT line goes high. (Required as CSF has its own on/off Switch)

During normal operation it causes the HPA, CSF and ATU to reset their tuning circuits and to initiate a tune sequence on the next pressel. In the 2FS mode it sets the ATU and CSF to by-pass during receive.

260. Tx/Rx is an output indicating the R/T transmit/receive status. It acts as a pressel line to the external equipments. Tx is indicated by 0V on the line.

261. RELAY CONTROL is an R/T output which sets the HPA to by-pass (i.e. When on receive). It follows the Tx/Rx line, except during tuning when it remains in the By-Pass Mode (i.e. +10V / Active) until the READY line indicates tuning completed.

262. 2FS becomes active (0V) when the R/T goes to transmit in the 2FS mode. (Refer to para 257.)

263. EXT UNIT PRESENT, PA PRESENT and CSF PRESENT (+10V active) indicate the presence and On/Off status of the external equipments. The PA PRESENT signal is also used in conjunction with ATU protection. (See para 269.)

264. PA CONTROL becomes active (0V) when power level 7 is selected. It permits the PA PRESENT signal to be produced subject to conditions within the HPA.

265. READY and FAULT are inputs to the R/T indicating the tuned/untuned and serviceability status of the external equipments. The active level is +10V. If both should occur together it will be presumed that a fault exists.

266. 28V and EARTH are supply outputs from the R/T to the CSF and, if the HPA is not present, to the ATU. If the HPA is present the ATU is supplied from there.

267. ALC (Automatic Level Control) is an analogue voltage fed back from an rf output monitor in the HPA to control the drive level from the R/T such that the output of the HPA is maintained at its nominal 100W level. The R/T output level is altered in inverse ratio to the voltage level.

268. ATU PROT (1) and ATU PROT (2) are protection signals to the HPA indicating unacceptable conditions within the ATU. The signals follow a sequence which causes a stepped reduction in power output from the system. In the event of adverse conditions occurring, ATU PROT (1) will become active first; this will cause the HPA output monitor to change its power output criterion to 50W and alter the R/T rf output level accordingly, via ALC. In the event that the fault clears (i.e. PROT (1) goes Low) the power will revert to 100W.

269. If the problem persists, ATU PROT (2) becomes active and ATU PROT (1) inactive. The HPA will enter the by-pass mode, PA PRESENT will become inactive (Low) and the R/T will revert to power level 4 (1.25W). In this state the operator can reset the power level up to 20W but if the problem in the ATU re-occurs ATU PROT (1) will again become active. This will reinstate PA PRESENT and the combination of 'low power state' and 'PA PRESENT' will cause the microprocessor to hold/reset the R/T power level to 1.25W.

270. Once PROT (2) has occurred the disappearance of the fault condition will not allow full power operation to be resumed until after a RESET and re-tune have been completed.

271. In the case of a low power configuration requiring direct connection of an ATU to the R/T, PA PRESENT is replaced by ATU PROT (2) which uses the same pin on the cable connector. The effect of ATU PROT (2) going high will then be the same as described for the final stage of the high power sequence i.e. the R/T sets its output level to 1.25W.