TELEPRINTER

TX 20

WORKSHOP TECHNICAL DOCUMENT

TECHNICAL DESCRIPTION

MAINTENANCE MANUAL

ILLUSTRATED PARTS CATALOGUE

SAGEM

TELEPRINTER TX 20

FOREWORD

The present Workshop Technical Document covering the TX 20 Teleprinter consists of three parts :

1 - Technical description

2 - Maintenance manual

3 - Illustrated parts catalogue

This document is a complement to the Field Maintenance Manual of the TX20 Teleprinter.

NOTA

This document cancels and replaces the Workshop Technical Document SA 10626

1

TECHNICAL DESCRIPTION

FOREWORD

The present TECHNICAL DESCRIPTION is only a support to understand the schematic diagrams.

In theory, the basic texts refer to the first version of the analysed board (Example : First block diagram of «PIA CLAVIER + MPU» board).

The «complementary data» refer to the second, third..... block diagram of the same board.

Therefore, differences of CIRCUIT REFERENCES can appear between the text and the various block diagrams.

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DRAWING 5 - "PIA IMP" board

DRAWING 6 - "PIA ERD + IT/ADA" board

DRAWING 7 - "PIA LECTEUR + AMPLI" board

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DRAWING 9 - "RAM + RPROM" board

DRAWING 10 - "PIA PERFO + AMPLI" board

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1 – UNIT CONTROL LOGIC

1.1 GENERAL

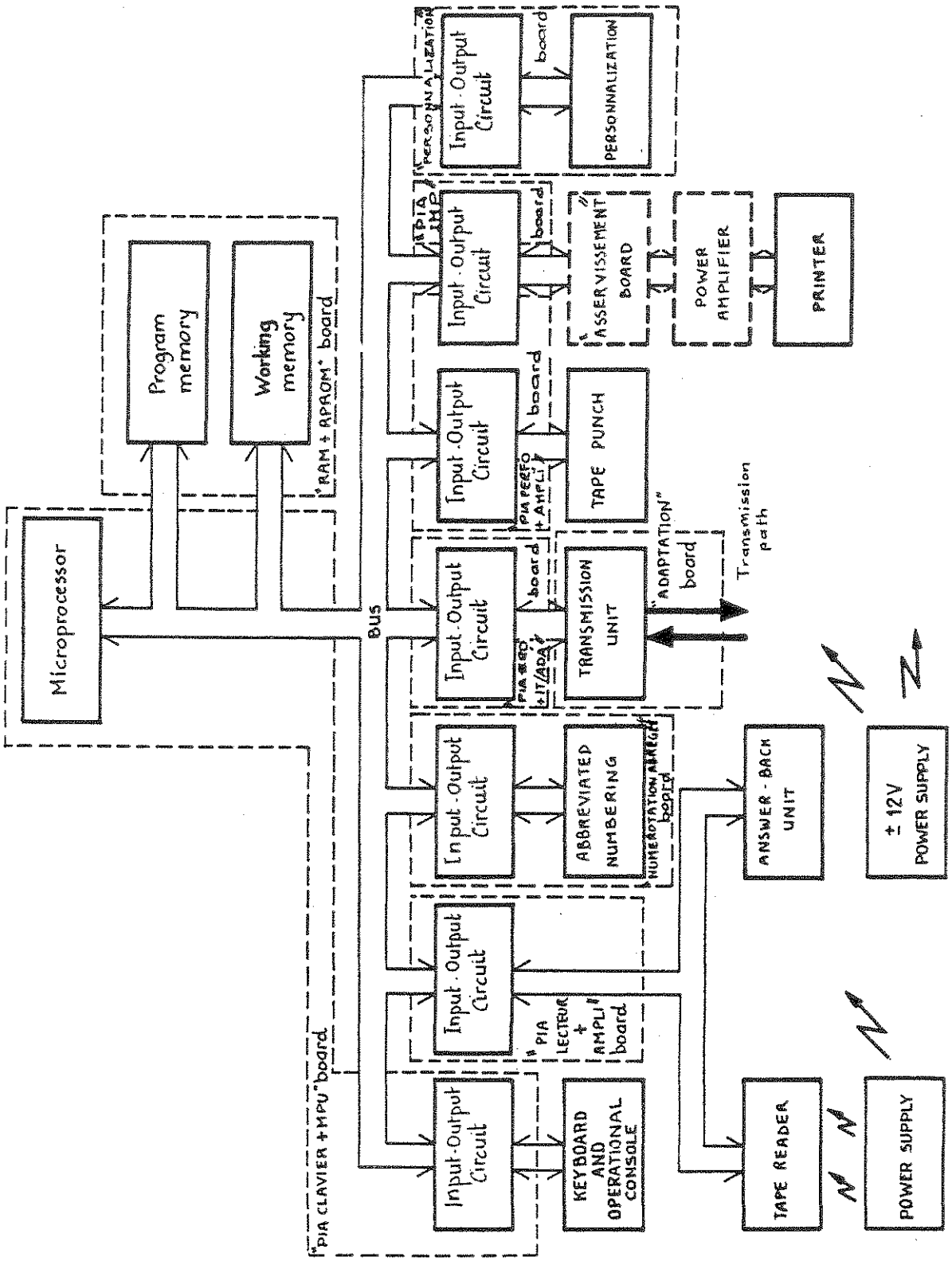
The control logic consists of :

- a microprocessor,
- a program memory,
- a working memory,
- module input-output circuits.

The control logic has the following basic purposes :

- testing and recognising MODULE statuses,
- according to these statuses, generating control sequences relative to the MODULES,
- respecting the hierarchies that exist between MODULES,
- ensuring data transfers from input MODULES to the relative output MODULES,
- temporarily storing incoming data when the output MODULE being addressed is not ready to receive it,
- ensuring data sequencing according to the incoming data and their origins,
- identifying characters or sequences of characters in the incoming data,
- according to these sequences and the origin of the data, generating MODULE remote control orders,
- counting characters belonging to code sub-assemblies and generating orders according to the count made,
- code-converting of incoming data prior to transfer towards certain MODULES.

LOCATION OF FUNCTIONS IN MODULES



Module	Location of associated electronics
OPERATIONNAL CONSOLE	"PIA CLAVIER + MPU" board "PERSONNALISATION" board "RAM + RPROM" board
KEYBOARD	"PIA CLAVIER + MPU" board
ANSWER-BACK UNIT	"PIA LECTEUR + AMPLI" board "PERSONNALISATION" board "RAM + RPROM" board
TAPE READER	"PIA LECTEUR + AMPLI" board "RAM + RPROM" board
TAPE PUNCH	"PIA PERFO + AMPLI" board "PERSONNALISATION" board "RAM + RPROM" board
TAPE STORE	"PIA PERFO + AMPLI" board
PRINTER, consisting of :	
. PRINTING DEVICE	"PIA IMP" board
. SENSOR	"ASSERVISSEMENT" board
. DRIVE MOTOR	POWER AMPLIFIER "ALIMENTATION" board "ASSERVISSEMENT" board
. PAPER ADVANCE	"PIA ERD + IT/ADA" board
. LINE FEED MOTOR	"PIA PERFO + AMPLI" board "PERSONNALISATION" board
. RIBBON ASSEMBLY (LEFT)	"PIA IMP" board
. RIBBON ASSEMBLY (RIGHT)	"PIA IMP" board "PIA PERFO + AMPLI" board "PIA ERD + IT/ADA" board
"NUMEROTATION ABREGEE"	"PIA CLAVIER + MPU" board
TRANSMISSION UNIT	"PIA ERD + IT/ADA" board "ADAPTATION" board
Power supply	POWER AMPLIFIER "ALIMENTATION" board + 12 V POWER SUPPLY TRANSFORMER MAINS FILTER "PARAFOUDRE" MAINS CABLE "RAM + RPROM" board

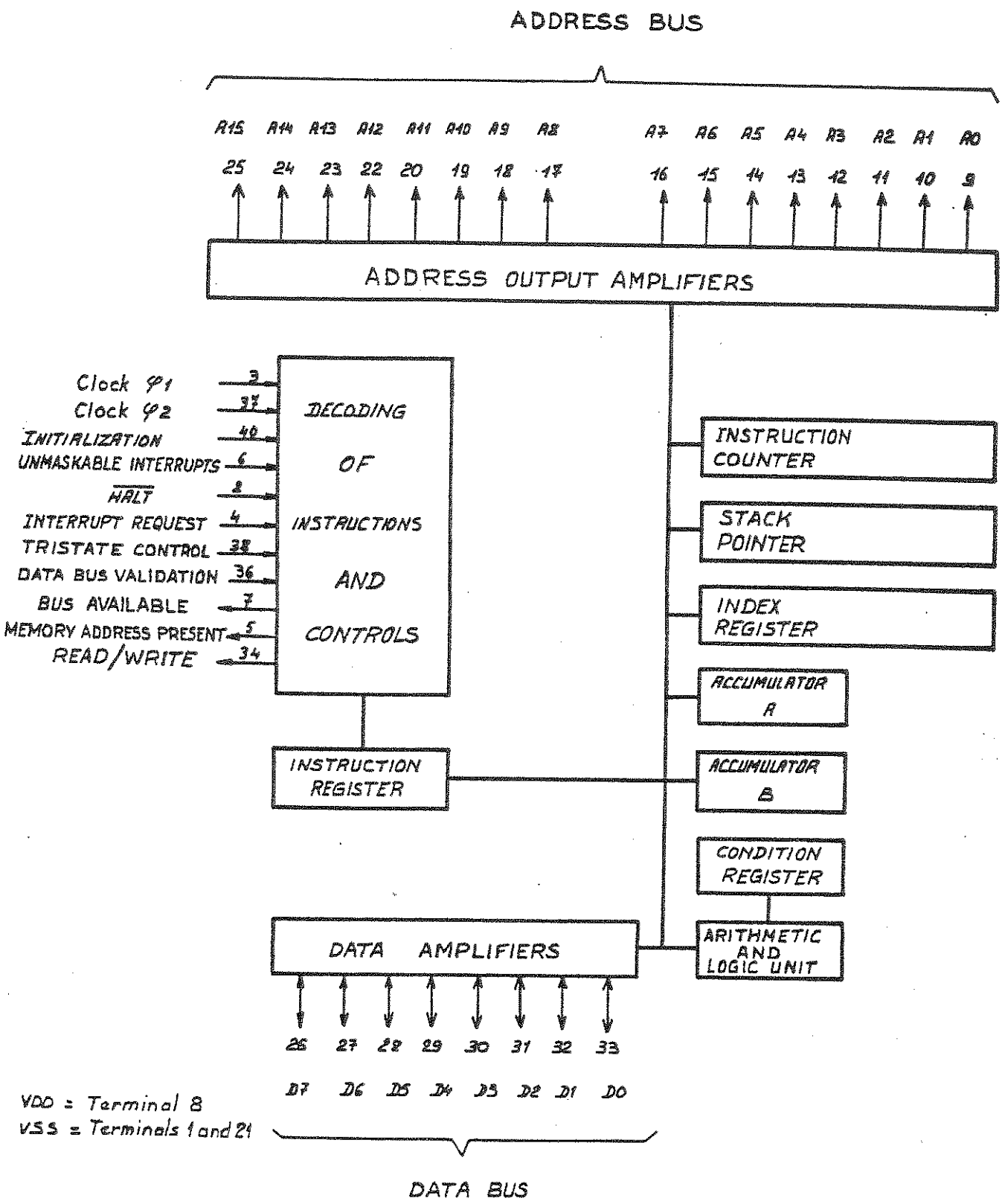


Figure 1 General structure of microprocessor

1.2 CHARACTERISTICS OF MICROPROCESSOR

1.2.1 General structure (see figures 1 and 2)

The microprocessor is an 8-bit word wired control microprocessor addressing a 64 k word capacity memory and having peripherals comprising :

- one instruction counter (16 bits),
- one stack pointer (16 bits),
- one index register (16 bits),
- two 8-bit accumulators A and B,
- one 6-bit condition register.

1.2.2 Addressing

The microprocessor has 7 addressing modes :

- accumulator addressing : one of the two accumulators A or B is specified in the instruction (one 8-bit byte),
- immediate addressing : the operand is contained in the instruction (two or three 8-bit bytes),
- direct addressing : these two-byte instructions are used for addressing the first 256 bytes of the memory,
- extended addressing : these three-byte instructions are used for addressing the entire memory,
- indexed addressing : these two-byte instructions are used for addressing the 256-byte location identified by the index register,
- implicit addressing : these one byte instructions relate to the stack or the internal registers,
- relative addressing : these two-byte instructions are used for addressing between 126 and + 129 bytes with respect to the instruction counter (conditional branching).

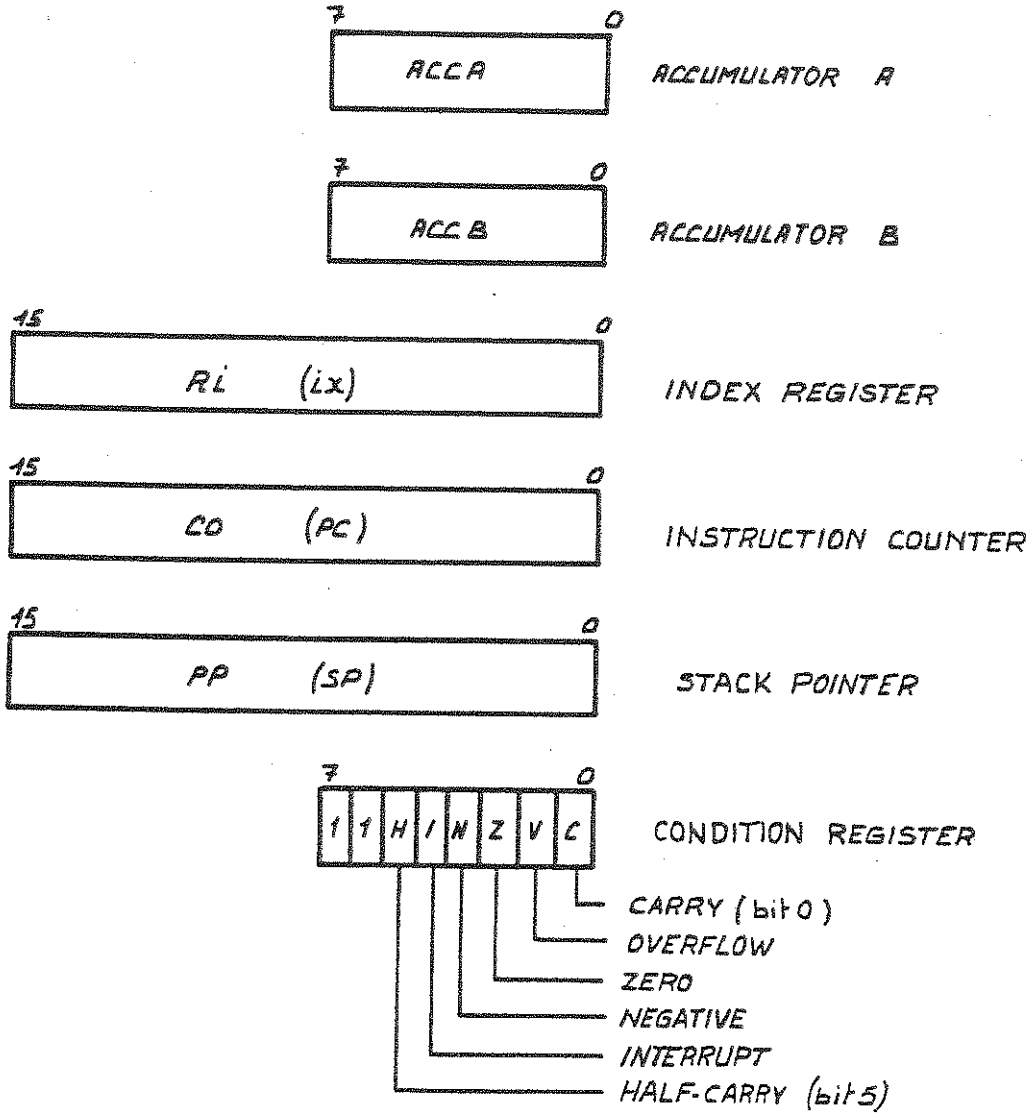


Figura 2 General structure of microprocessor

1.2.3. Instruction set

The instruction set comprises 72 instructions :

- memory or accumulator reference instructions : 30
- instructions concerning the index register and stack handling : 11
- conditional branching and jump instructions : 23
- instructions relative to the condition register : 8

In particular, the instruction set includes :

- program sequencing instructions : conditional jumps, sub-routine call instructions with automatic protection of the instruction counter in the stack and a sub-routine return instruction with automatic restoration of the instruction counter,
- context change instructions : call supervisor, change and store instruction counter and return instructions with automatic context restoration,
- instructions relating to the stack.

1.2.4 Interrupts

There are three types of interrupts available :

- maskable interrupt,
- unmaskable interrupt,
- software interrupt.

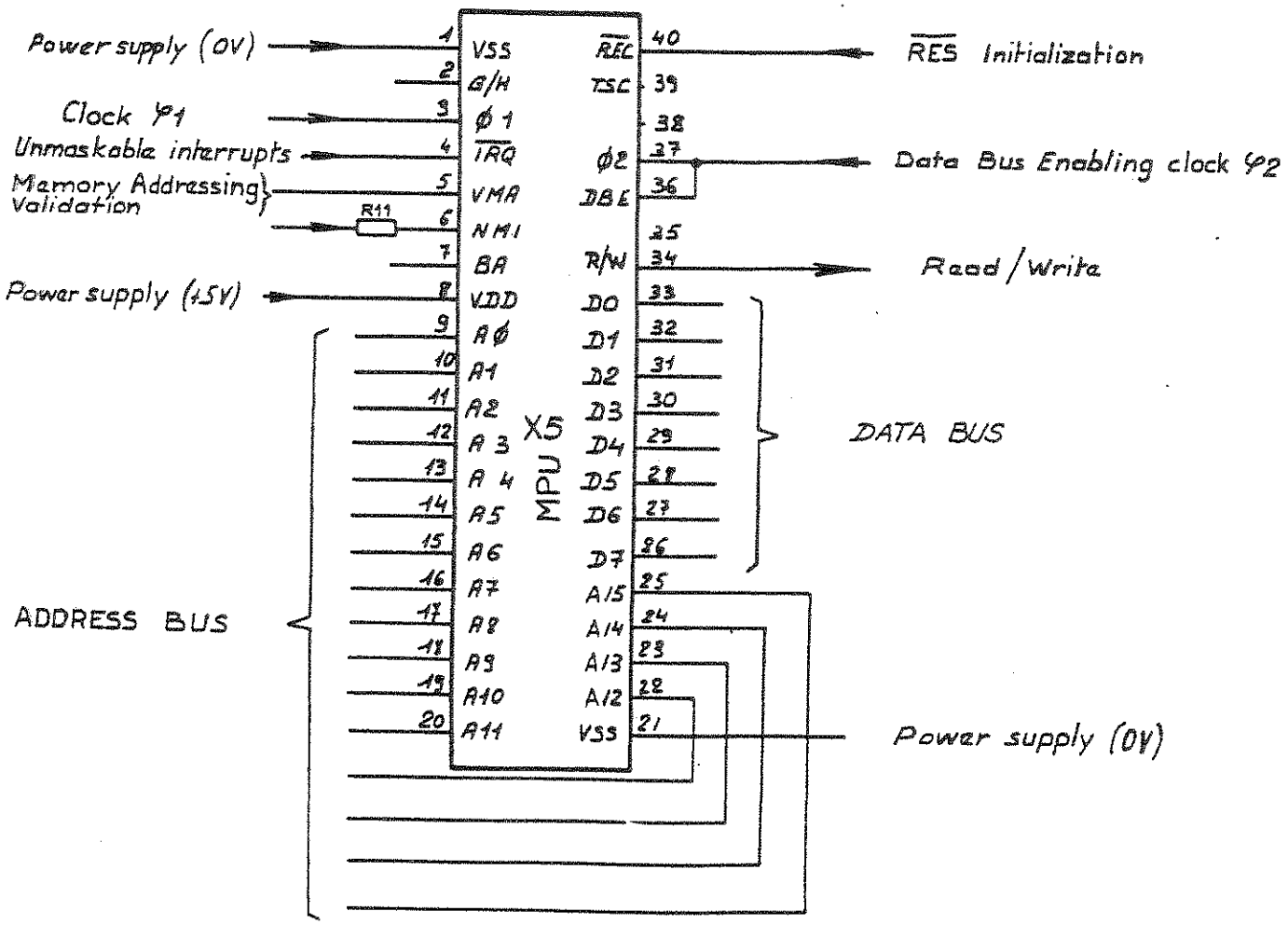
The interrupts are managed automatically with protection of the context in the stack and connection to the addresses contained in a fixed memory location.

1.3 OPERATION OF MICROPROCESSOR

("PIA CLAVIER + MPU" board)

The microprocessor (X5) requires a + 5 V power supply for VDD (0 V for VSS, two terminals) and a two phase clock consisting of signals $\varphi 1$ and $\varphi 2$ wich are in phase-opposition (see paragraph : time base).

The "$\overline{RES}$" initialization signal appearing at ($\overline{REC}$) and coming from the "ALIMENTATION" board can be used for disabling the microprocessor (X5) during switching on or in the event of a brief break in the mains. The Memory Addressing Validation signal "VMA" is used for generating the Enabling signal "E" (see paragraph : time base). All the unmasked interruptions coming from the various input/output circuits of the unit appear at terminal ($\overline{IRQ}$). The address bus consists of a group of 16 wires in parallel (A0 to A15). The data bus, consisting of 8 wires (D0 to D7) is validated by the $\varphi 2$ clock also wired on the Data Bus Enabling (DBE) input. The microprocessor generates the Read/Write signal "R/W" allowing dialogue between the microprocessor and the unit input-output circuits via buses.

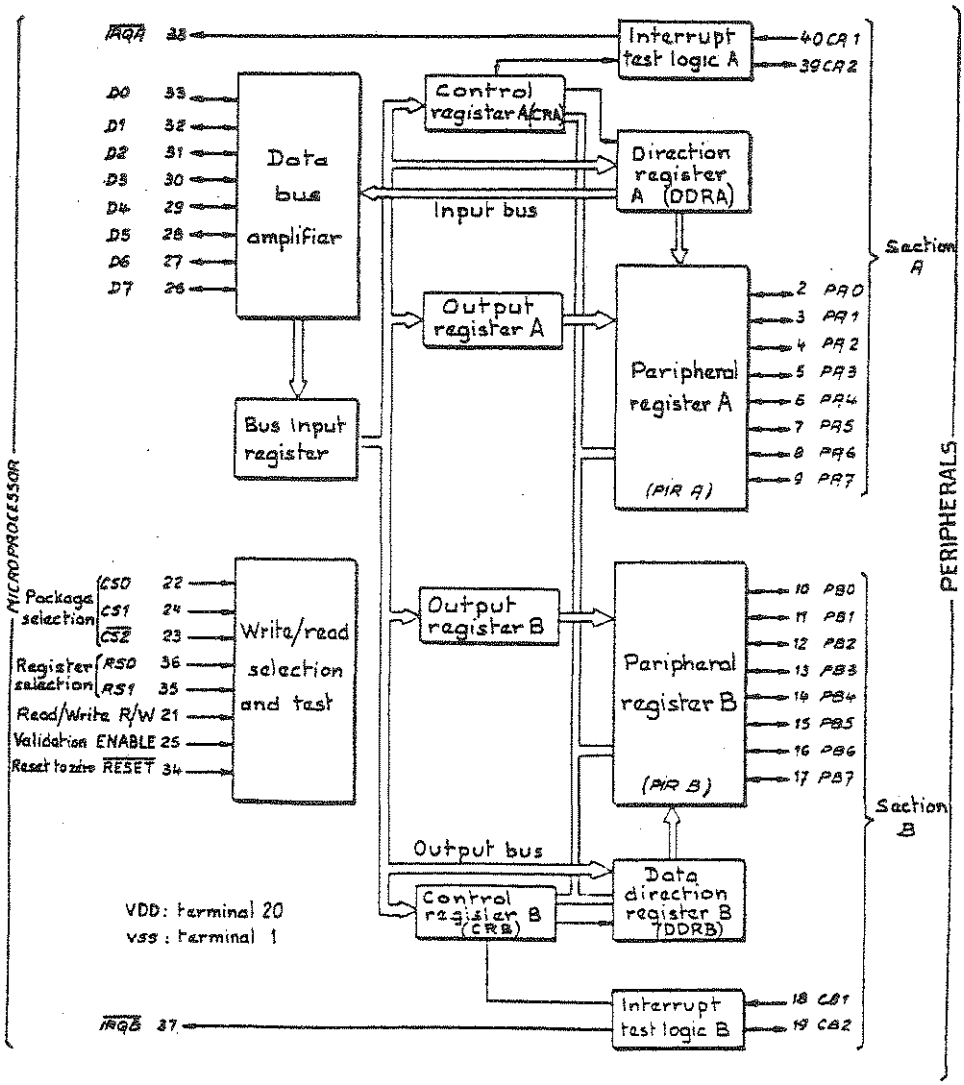


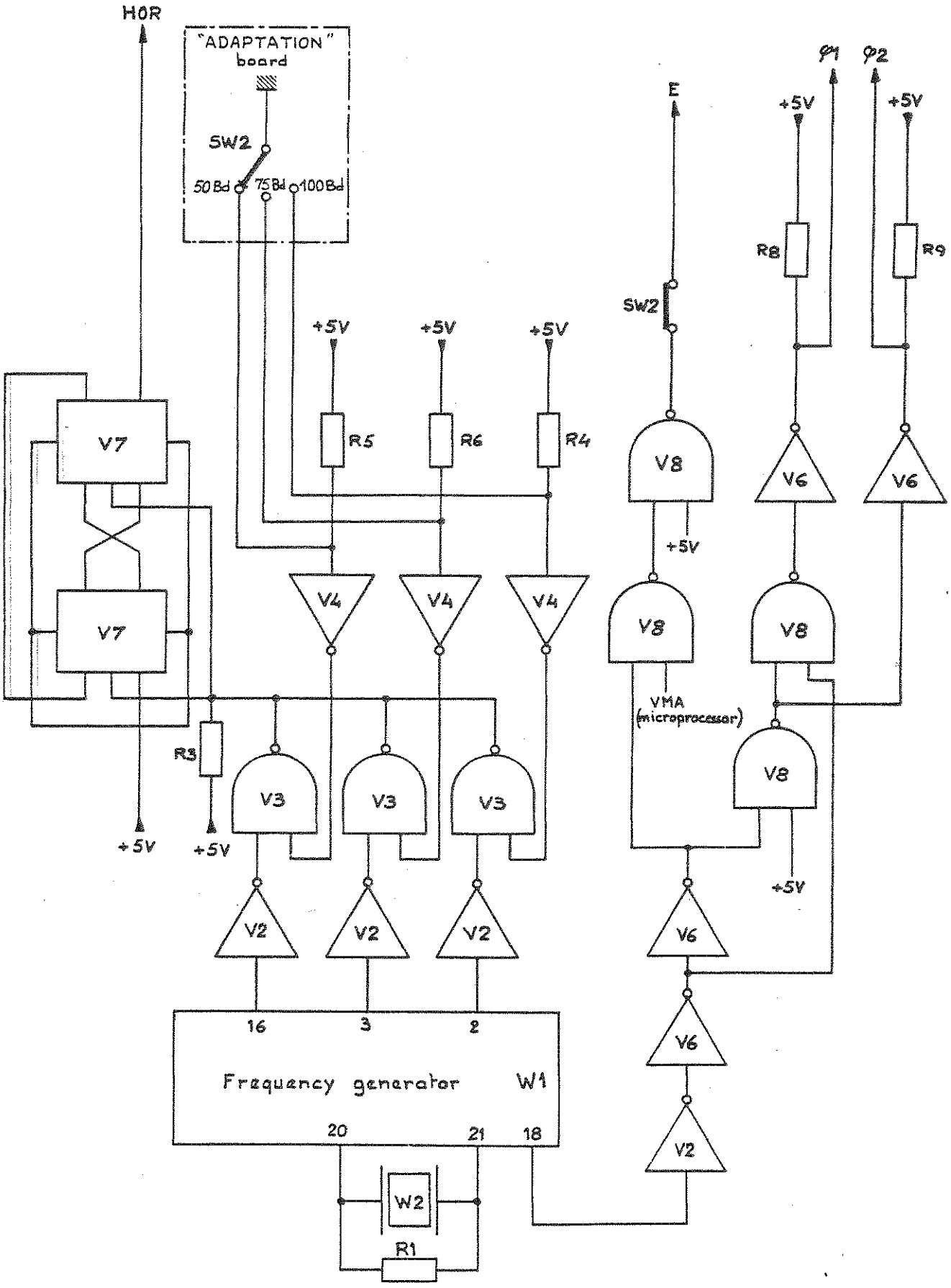
1.4 CHARACTERISTICS OF INPUT-OUTPUT CIRCUIT

General structure

The PIA input-output circuit consists of :

- a bidirectional bus for transfers to and from the microprocessor,
- two 8-wire bidirectional buses for transfers to and from the peripherals,
- two peripheral registers (PIRA and PIRB),
- two programmable control registers (CRA and CRB),
- two operating direction definition registers for each of the wires on the two peripheral transfer buses (Data Direction Registers DDRA and DDRB),
- four interrupt input lines which can be checked individually (CA1, CA2, CB1, CB2). Two of them (CA2, CB2) can also be used as peripheral control output lines.




HOR
"ADAPTATION" board
SW2
50 Bd
75 Bd
100 Bd
+5V
+5V
+5V
R5
R6
R4
V7
V7
V4
V4
V4
R3
V3
V3
V3
+5V
+5V
V2
V2
V2
16
3
2
Frequency generator
W1
20
21
18
W2
R1
E
SW2
V8
+5V
V8
V8
VMA (microprocessor)
V8
+5V
V6
V6
V6
V6
V2
φ1
φ2
+5V
+5V
R8
R9
V6
V6

Time base

1.5 TIME BASE

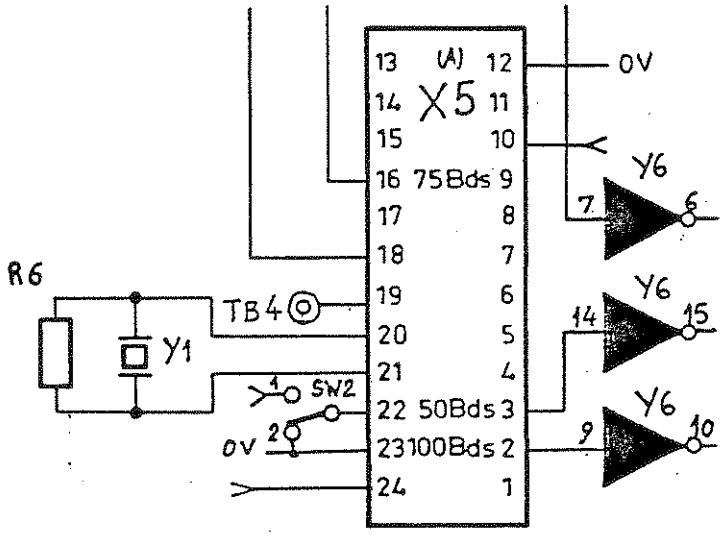
("PIA CLAVIER + MPU" board)

The time base of the unit consists of a frequency generator (W1) ("PIA-CLAVIER + MPU" board) controlled by a crystal (W2).

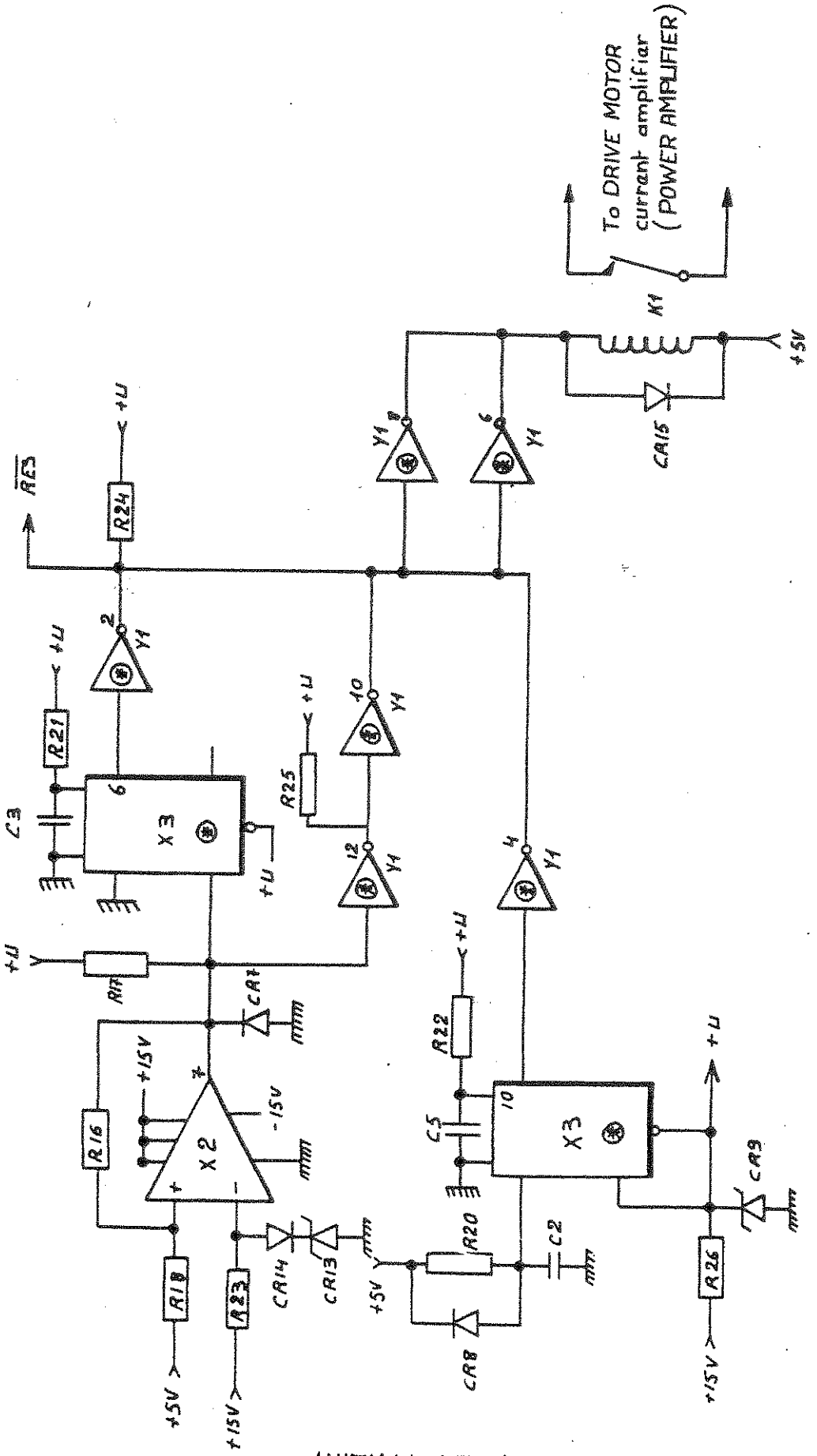
Three outputs of the frequency generator are used for obtaining the clock signals corresponding to telegraph speed of 100 bauds, 75 bauds and 50 bauds. The selection of the telegraph speed used is obtained by switch (SW2), located on the "ADAPTATION" board, the logic gates assembly (V2, V3 and V4) and the resistors (R4, R5 and R6). The signal resulting from the selection is then divided by three by a group of flip-flops (V7) which furnish the clock signal (HOR) necessary for operating the general-purpose asynchronous transmitter-receiver circuit UART (Y2) ("PIA ERD + IT/ADA" board).

The two clock signals (φ1 and φ2) required for the operation of the microprocessor (X5), are also generated by the frequency generator (W1). Signals φ1 and φ2 are brought into phase opposition by a group of logic gates and inverters (V6 and V8). The Validation of Memory Addressing signal "VMA" from the microprocessor (X5) inhibits the Enabling signal "E". Switch (SW2) opens the "E" signal circuit in order to test the input-output circuit (Y2) of the KEYBOARD when using the test set EMP-2

1.5.1 Complementary data



The switch (SW2) allows a margin $\geqslant$ 45 %



(*) +U power supply

INITIALIZATION CIRCUIT

1.6 INITIALIZATION CIRCUIT

(«ALIMENTATION» board, plates 3-1, 3-2)

The initialization circuit is used for two purposes :

- firstly, applying a pulse, active at level zero, for resetting an initial state at "$\overline{RES}$" (restart) for the microprocessor and the input-output circuits in the following cases :

  . switching on of the unit,

  . brief break in power supply voltage,

  . drop in power supply voltage beyond tolerance provided for,

- then, inhibiting the DRIVE MOTOR amplifier during the initialization signal.

1.6.1 Operation during switching on

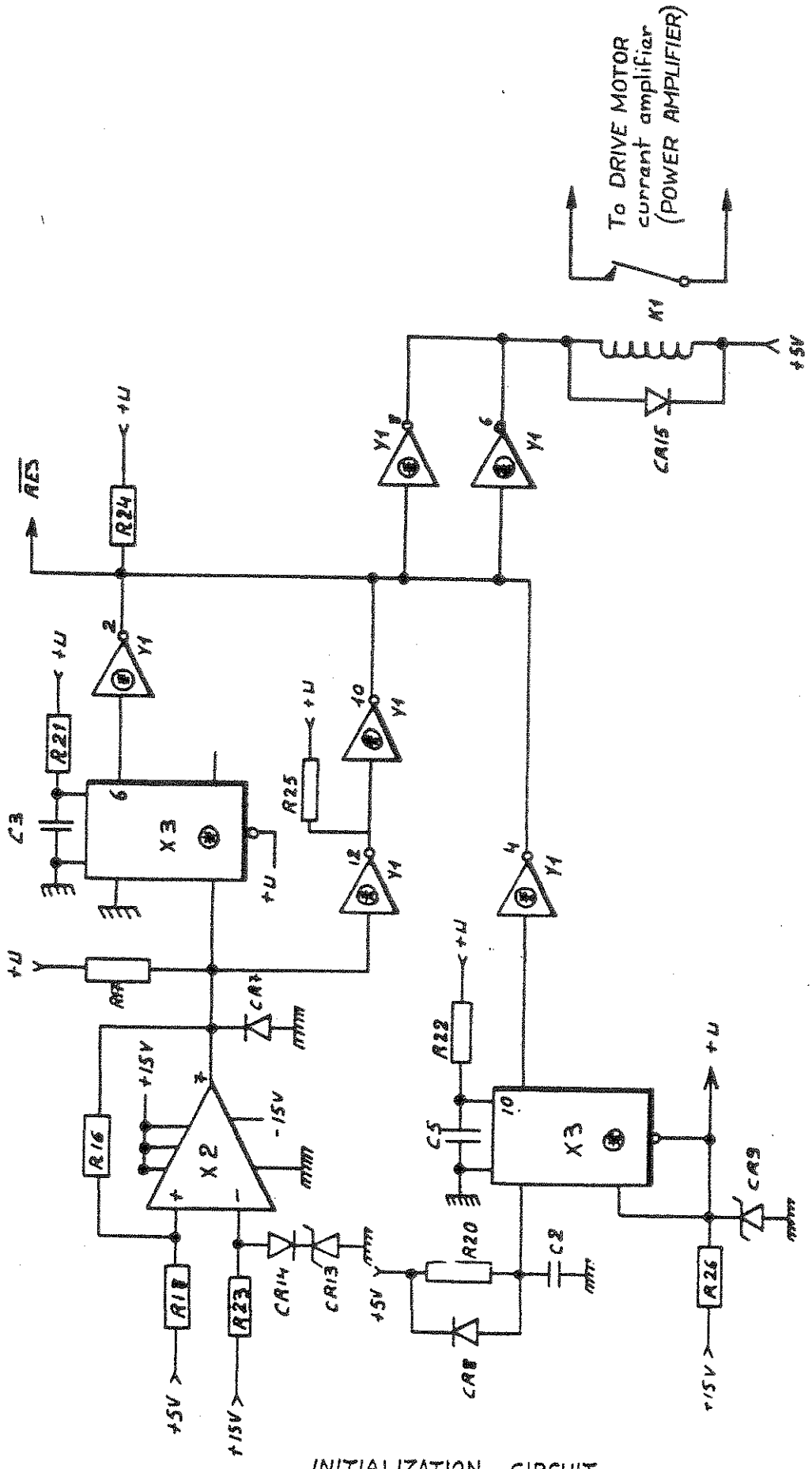
During switching on, the + 5 V power supply is applied and charges capacitor C2 through resistor R20. The leading edge of the capacitor charge signal triggers monostable (X3-10) which generates a positive pulse (see NOTE). The inverter (Y1-4) complements this pulse to supply a pulse, active at level zero, to initialize "$\overline{RES}$".

The voltage "+U" energizing resistor (R24) charging the open-collector inverters (Y1-2) (Y1-10) and (Y1-4), is obtained from the + 15 V via resistor (R26) and is regulated by diode (CR9).

Diode (CR8) is used for quickly discharging (C2) in the event of a break in the power supply voltage.

Parallel-connected inverters (Y1-6) and (Y1-8) control relay (K1) from "$\overline{RES}$". (K1) is normally closed and blocks the DRIVE MOTOR amplifier during the initialization pulse then opens when energized, to enable carriage movement.

NOTE : Monostable (X3-10) signifies : monostable corresponding to output (10) of package (X3). Pulse duration : 30μS typical.



⊛ +U power supply

INITIALIZATION CIRCUIT

1.6.2. Operation during a short break in the power supply voltage

Because the + 15 V power supply voltage remains established longer than the + 5 V, the operational amplifier (X2) receives the + 5 V through resistor (R18) of the positive input and compares it to a reference, obtained by diodes (CR13-CR14) and resistor (R23) from the + 15 V.

When a break in the mains power supply causes the + 5 V voltage to drop below the input reference threshold (4.6 V), the amplifier (X2) provides a high to low level signal which triggers monostable multivibrator (X3-6).

Multivibrator (X3-6) generates a positive pulse (longer than 60 ms), complemented by inverter (Y1-2), to give the initialization pulse "$\overline{\text{RES}}$", active at level zero.

During the transmission of "$\overline{\text{RES}}$", the inverters (Y1-8) and (Y1-6) return relay (K1) to the de-energized state thus blocking the DRIVE MOTOR amplifier. Resistor (R17) energizes the output transistor of the amplifier (X2) while the diode (CR7) clamps the negative peaks of the output signal.

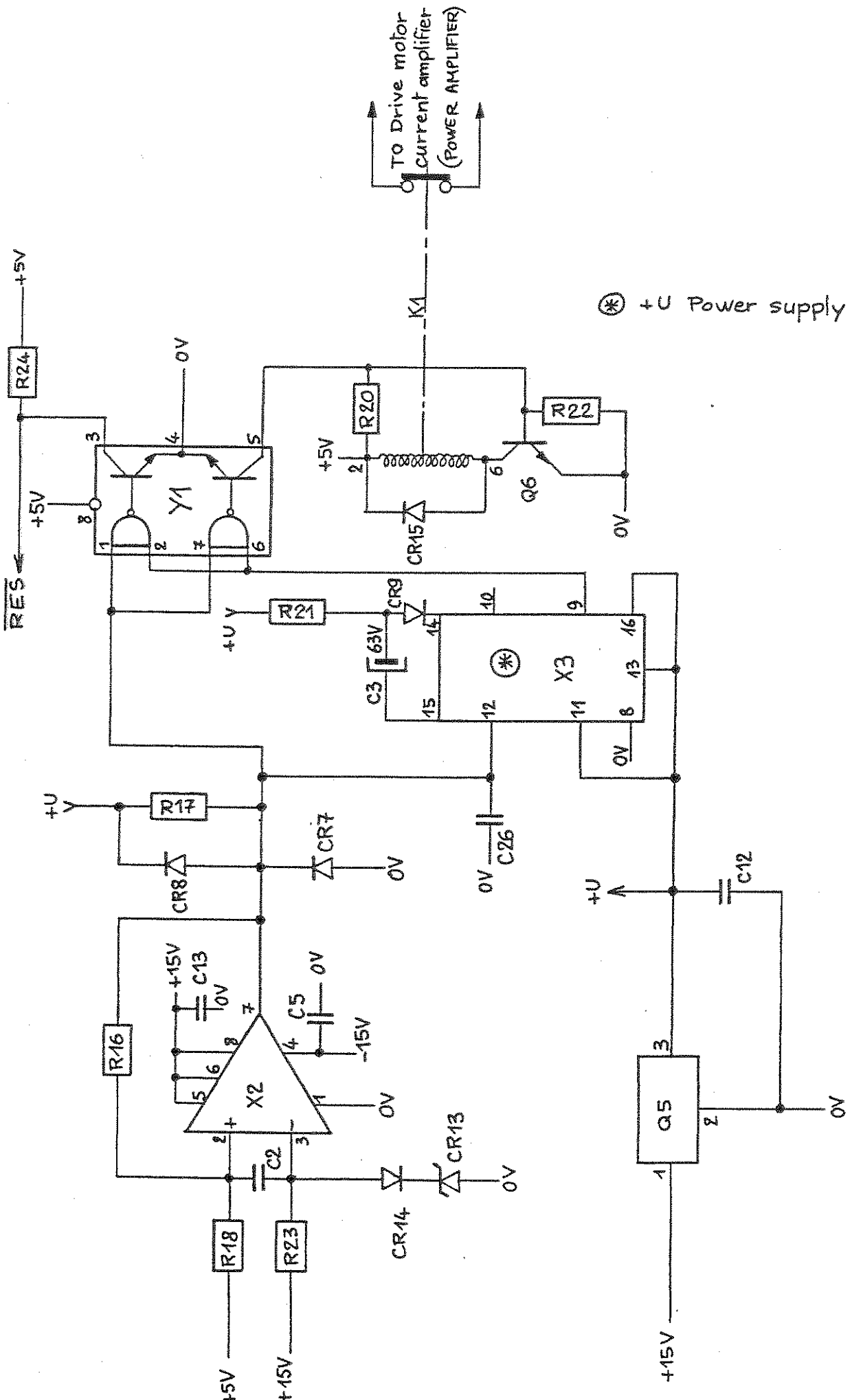
1.6.3. Operation during a drop in power supply voltage

When the power supply voltage drops beyond the rated tolerance, the + 5 V voltage comprises ripple superposed on the DC voltage.

The ripple, shaped by amplifier (X2), triggers multivibrator (X3-6) which generates the "$\overline{\text{RES}}$" signal through the inverter (Y1-2).

The operating details are identical to those described in the preceding paragraph.

If the power supply voltage drop continues beyond the duration of the multivibrator pulse, the "$\overline{\text{RES}}$" signal is supplied by the inverters (Y1-12) loaded by resistor (R25), and (Y1-10).



INITIALIZATION CIRCUIT

1.6.4 Complementary data

INITIALIZATION CIRCUIT
(«ALIMENTATION» board, plate 3-3)

The initialization circuit is used for two purposes :

- Firstly, applying a pulse, active at level zero «$\overline{\text{RES}}$» (Restart), which initializes all the input-output circuits and the microprocessor, in the following cases :

  . switching on of the unit,

  . brief break or drop in power supply voltage beyond tolerance provided for.

- then, inhibiting the DRIVE MOTOR amplifier during the initialization signal.

1.6.4.1 Operation during switching on

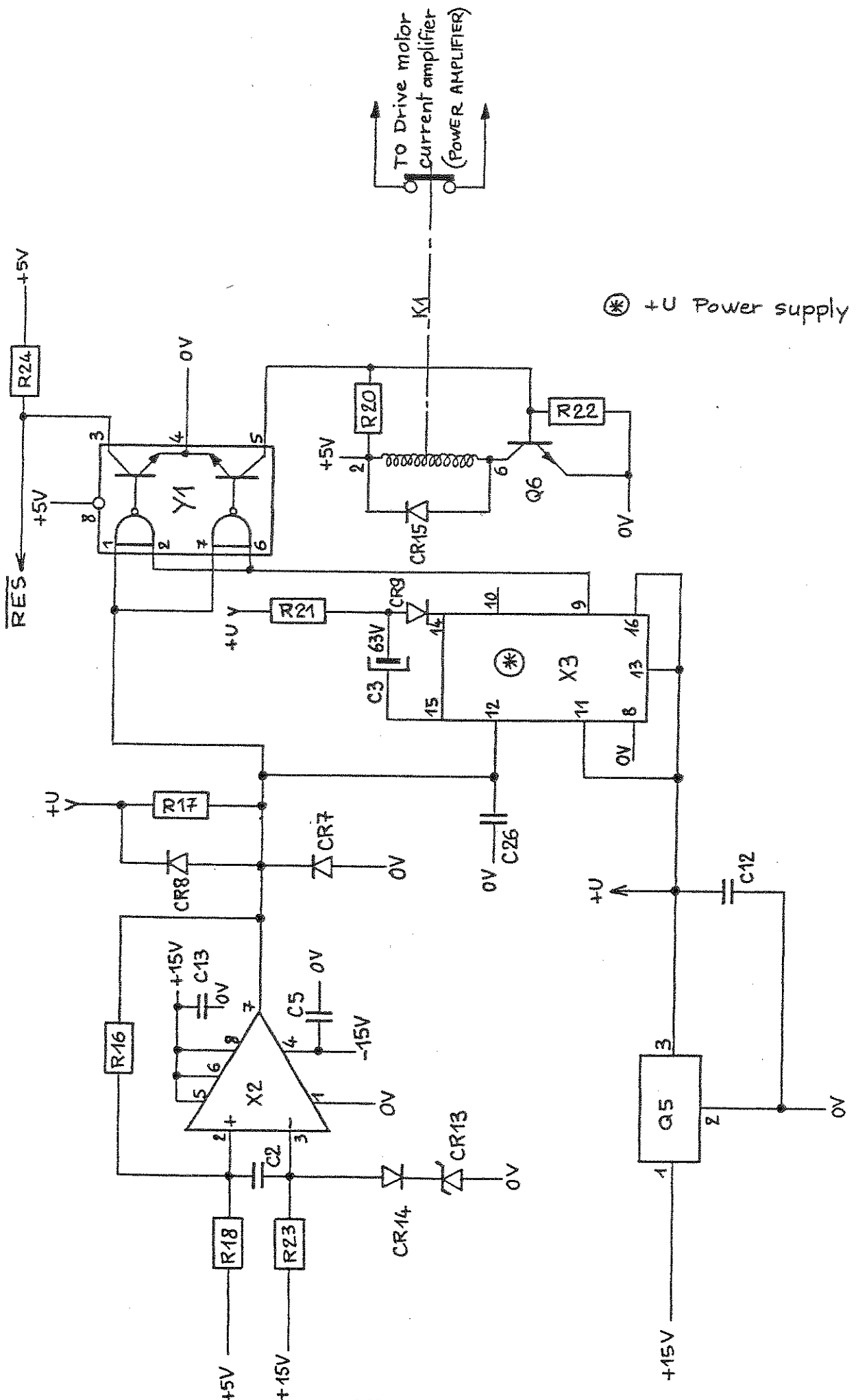
During switching on, the + 15 V power supply is applied before the + 5 V, permitting to supply the monostable (X3) and to provide the reference voltage on (X2) before the + 5 V.

The voltage «+ U» energizing resistors (R17) and (R21) is obtained from the + 15 V through the voltage regulator (Q5).

The comparator (X2-7) generates a high level logic, the positive transition puts (X3-9) to a low level during the time constancy of the monostable determined by the resistor (R21) and the capacitor (C3) (about 150 ms). The inputs (Y1-1) being to «1» and (Y1-2) to «0» the output transistor of (Y1) becomes conducting and generates a pulse, active at level zero «$\overline{\text{RES}}$». After 150 ms (X3-9) changes to a high level thus causing switching to state «1» of «$\overline{\text{RES}}$».

During the transmission of «$\overline{\text{RES}}$», the transistor (Q6) becomes blocked and the relay (K1) which is normally closed blocks the DRIVE MOTOR amplifier. After 150 ms the contact opens and enables carriage movement.

The diodes (CR8 - CR7) clamps the peaks of the output signal.



INITIALIZATION CIRCUIT

1.6.4.2 Operation during a short break or a drop in power supply

Because the + 15 V power supply voltage remains established longer than the + 5 V, the comparator (X2) receives the + 5 V through resistor (R18) of the positive input and compares it to a reference, obtained by diodes (CR13 - CR14) and resistor (R23) from the + 15 V.

When a break in the mains power supply causes the + 5 V voltage to drop below the input reference threshold (4.6 V), the comparator (X2-7) provides a high to low level signal, the inputs (Y1-1) and (Y1-7) switch and the signal «$\overline{\text{RES}}$» changes to a low level. When the power supply becomes normal the comparator (X2-7) generates a low to high edge which triggers monostable (X3). After 150 ms, the signal «$\overline{\text{RES}}$» changes to «1», the transistor (Q6) is saturated and carriage movement is permitted.

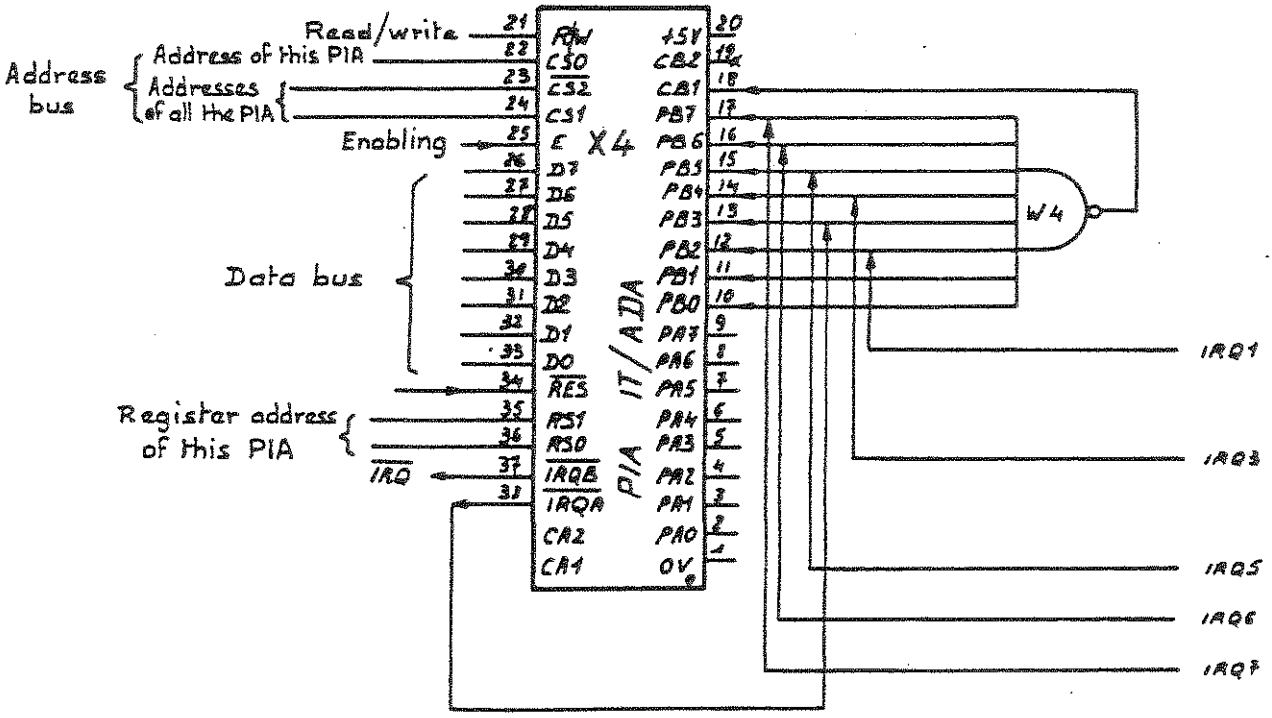
1.7 PROGRAM INTERRUPT INPUT-OUTPUT CIRCUIT

("PIA ERD + IT/ADA" board)

The interrupts (IRQ1 to IRQ7) from the various unit input-output circuits simultaneously excite :

- inputs (PB0 to PB7) of the input-output circuit ("PIA IT/ADA", X4),
- an 8-input "NAND" logic gate (W4).

The output signal of the logic gate is applied to input (CB1) of (X4). Output ($\overline{IRQB}$) of (X4) supplies the "$\overline{IRQ}$" signal applied to the microprocessor on the "PIA CLAVIER + MPU" board.



1.8 PROGRAM AND WORKING MEMORIES

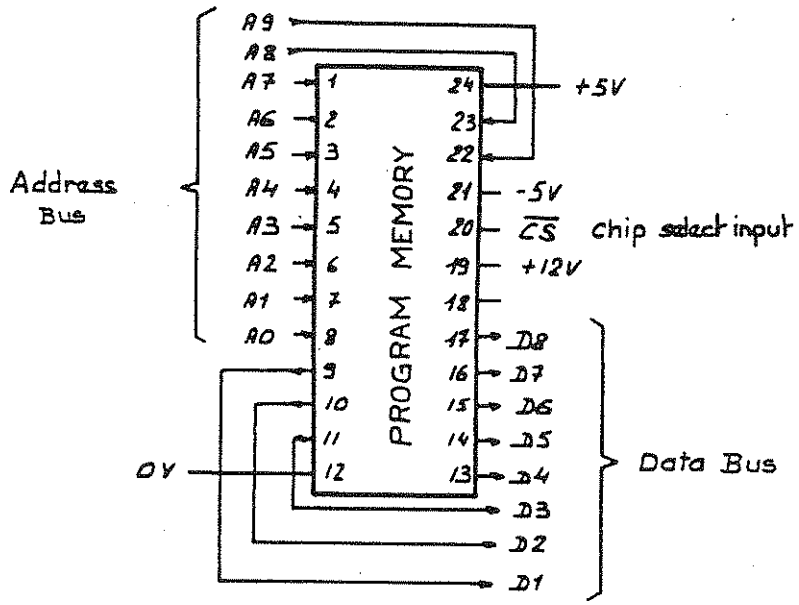
(«RAM - RPROM» board, plate 9-1)

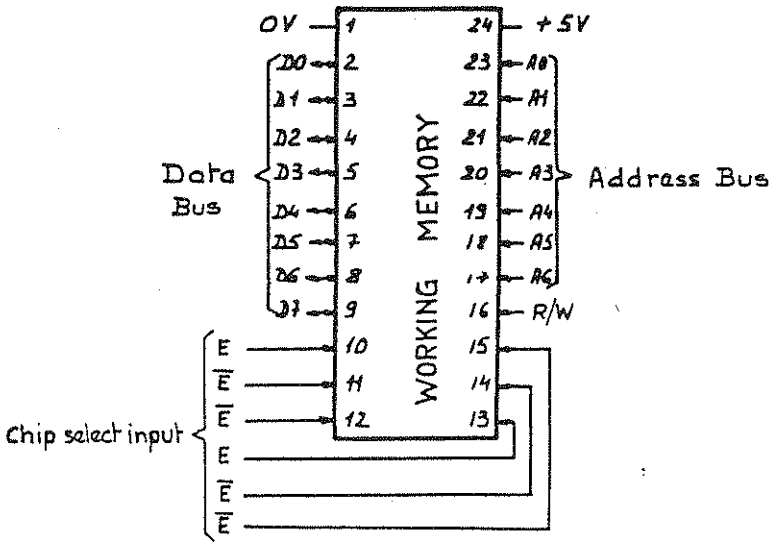
1.8.1 General

The unit uses two types of memories :

- the program memory (RPROM or REPROM)
- the working memory (RAM).

The instructions, contained in the program memory, define the reactions of the unit according to the context and the controls received. The working memories permanently store the status of the unit and record certain data which cannot be processed immediately.





1.8.2 Program-memory (figures 1 and 2)

The outputs (D0 to D7) are connected to the data bus. The addressing signals "A0" to "A9" are adapted to levels 0 and + 5 V by the circuits (Z1 to Z3). The selection of a package is ensured by the input ($\overline{CS}$). A decoder circuit (Z4) makes selections from signals "A10", "A11" and "A12". The program memory consists of 7 packages (Y2, Y3, Y5, Y7 to Y10) mounted in I.C. sockets.

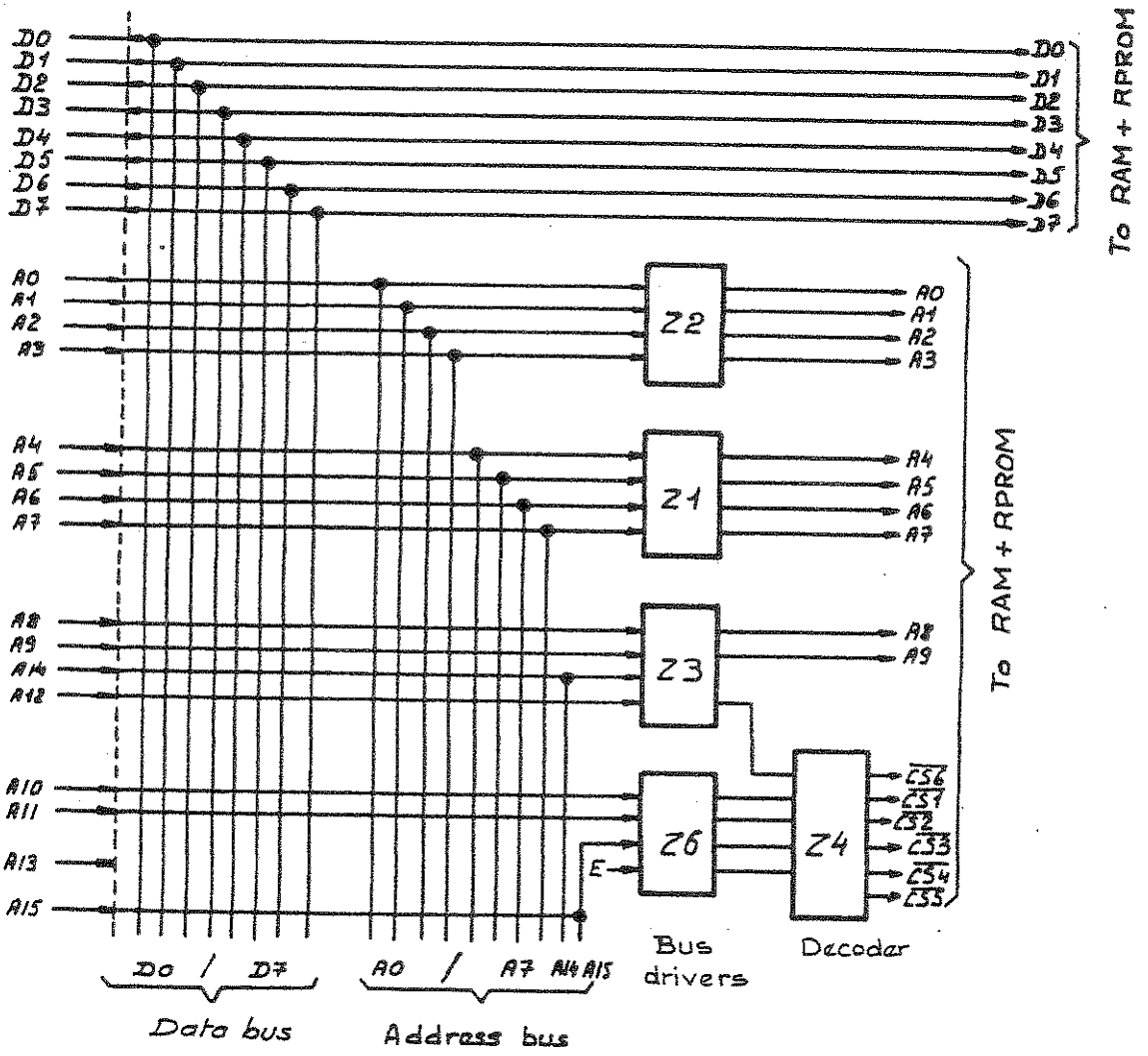


figure 1 Program memory

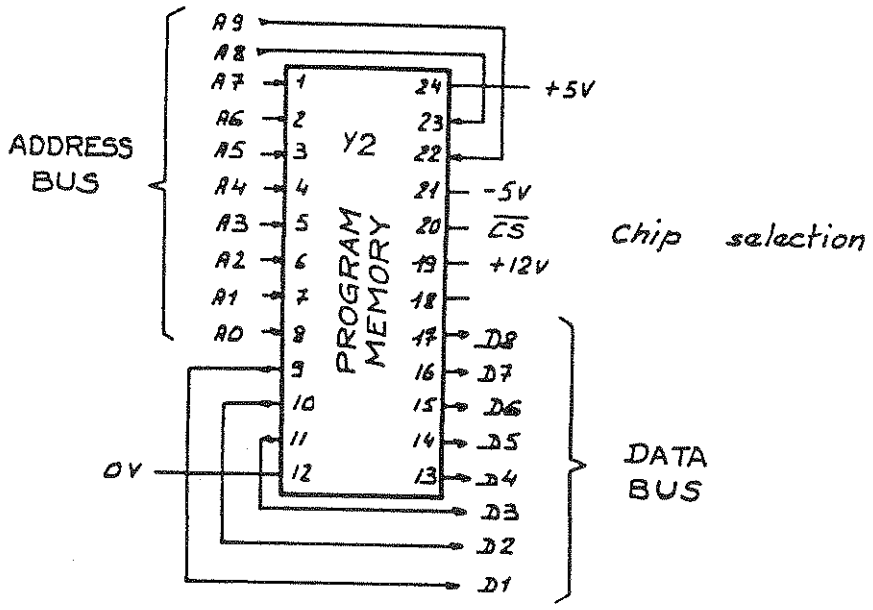


Figure 2. Program memory (R PROM)
7 identical packages Y2, Y3, Y5, Y7/Y10

1.8.3 Working memory (figures 1 and 3)

The inputs or outputs (D0) to (D7) are connected to the data bus. The addressing signals "A0" to "A6" are adapted to levels 0 and + 5 V by the circuits (Z1) and (Z2). The selection of a package is made through inputs (E) and ($\overline{E}$), with "A7", "A8", "A14", "A15" and "E" signals. The working memory consists of two packages (Y12 and Z11).

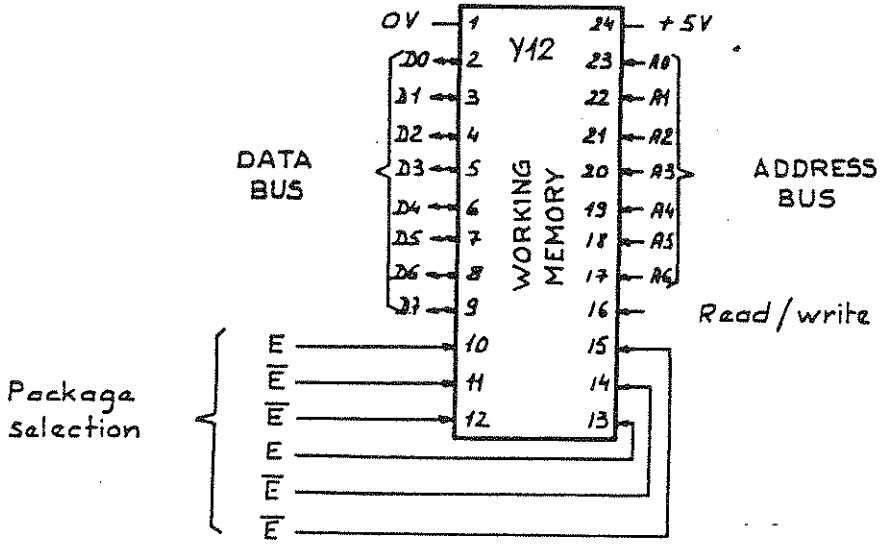


Figure 3 Working memory (RAM)
two identical packages Y12 and Z11

1.8.4 Complementary data

(«RAM + RPROM» board, plate 9-3)

Program memory (Figure 1)

The program memory consists of 4 packages (Z01, Z02, Z03, Z04) mounted in I.C. sockets.

The selection of a package is provided by inputs «E*» and «ADM1*» to «ADM5*». These inputs are driven by a decoder - demultiplexer circuit from signals «$\overline{AD11}$», «$\overline{AD12}$», «$\overline{AD13}$» and «$\overline{SELCM}$». The signal «$\overline{SELCM}$» is generated from signals «AD14», «AD15» and «R/W*».

Logicial 8 K : strap S in position $\lessdot$ 8 K.

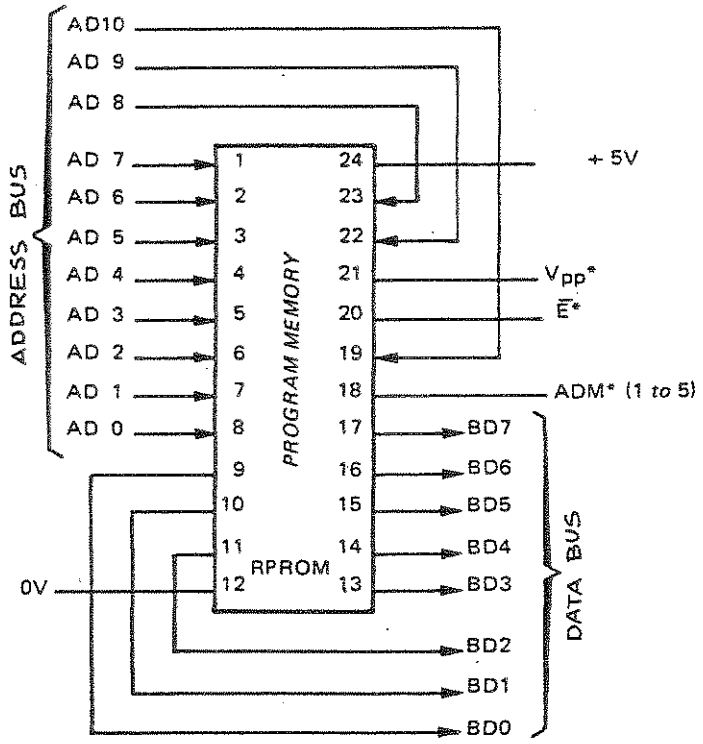


FIGURE 2 - PROGRAM MEMORY (RPROM)
(4 identical packages Z01, Z02, Z03, Z04)

Addressing signals «AD0» to «AD10» proceeding from «A0» to «A10» and outputs «BD0» to «BD7» are respectively adapted to the address bus and to the data bus of the microprocessor through adaptors circuits (Z06, Z07, Z08, Z13, Z16).

Working memory (Figure 2)

The working memory consists of 2 packages (Z14 and Z15).

The inputs or outputs «D0» to «D7» are connected to data bus.

Signals «AD0» to «AD9» and «D0» to «D7» are respectively adapted to the data bus and to the address bus through adaptors circuits (Z06, Z07, Z13, Z16).

The selection of a package is made through inputs «$\overline{CE}$» and «R/W*», with «A14», «A15», «E» and «R/W*» signals.

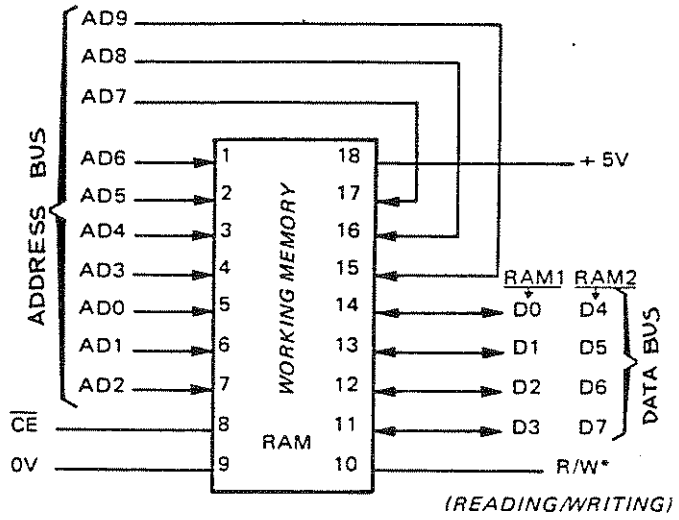
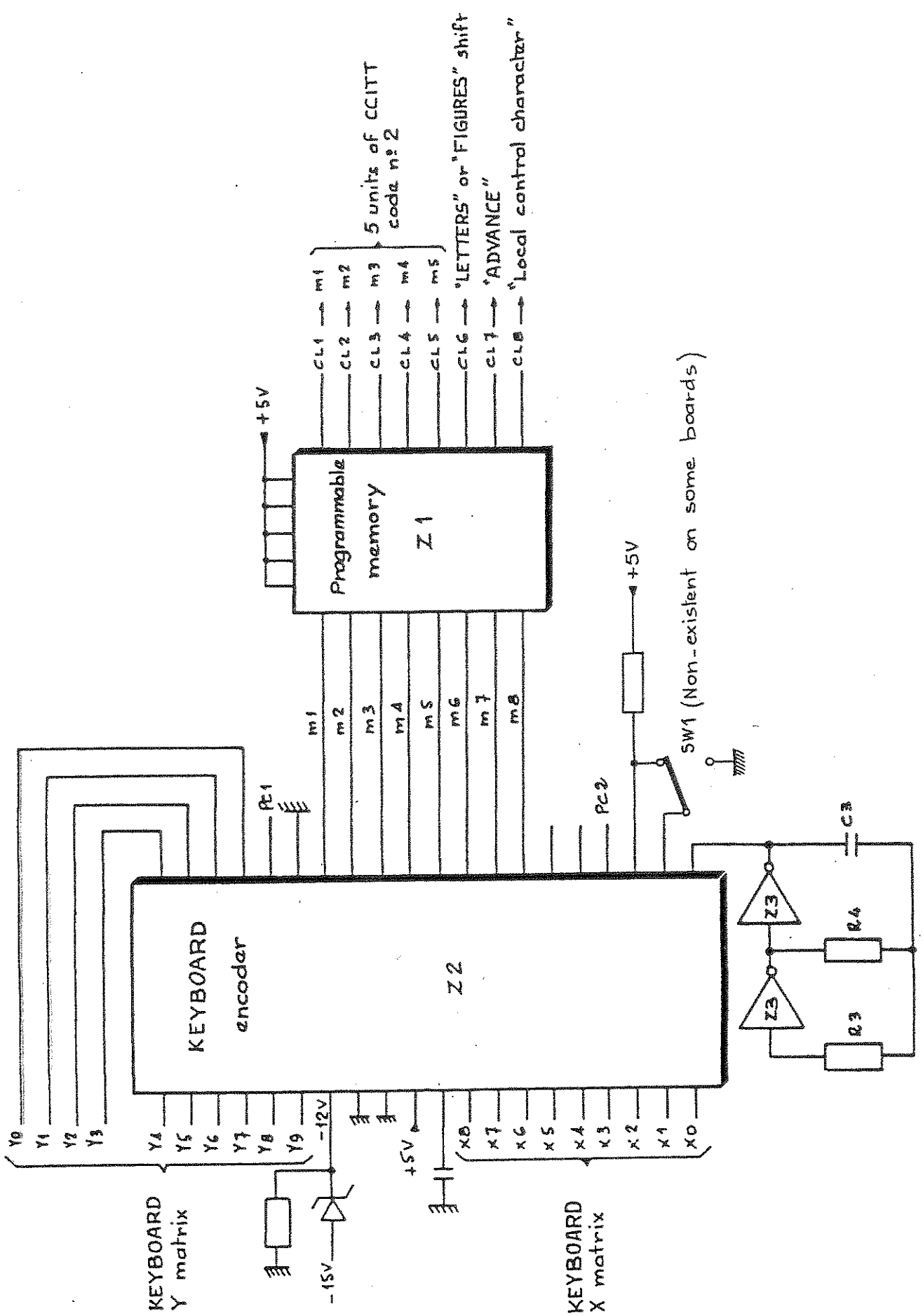


FIGURE 2 - WORKING MEMORY (RAM)
(2 identical packages Z14 and Z15)



"CLAVIER" board

2 – KEYBOARD
(«CLAVIER» board)

2.1 GENERAL

The keyboard is of the extended type. The 9 inputs (X0 to X8) of the KEYBOARD matrix, associated with 10 outputs (Y0 to Y9) of the same matrix, allow 90 combinations to be generated.

The electronic part of the KEYBOARD mainly consists of two "MOS" circuits :

- one KEYBOARD encoder (Z2),
- one "ROM" programmable memory (Z1).

When a key is depressed, the encoder of the KEYBOARD (Z2) supplies :

- character presence signals "PC1" and "PC2",
- the addressing of the memory corresponding to the selected character code (m1 to m8).

The KEYBOARD encoder compares the output signals from two counters : (X0 to X8) from the first one, (Y0 to Y9) from the second one. The depressing of a key generates continuity between an X and a Y. The similarity between the signals (Y0 to Y9) and (X0 to X8) causes the transmission of "PC1". Signal "PC2" remains present as long as the KEYBOARD key is held down.

An external clock provided by two inverters (Z3), two resistors (R3 and R4) and a capacitor (C3), supplies a signal to the KEYBOARD encoder with a frequency of approximately 10 kHz.

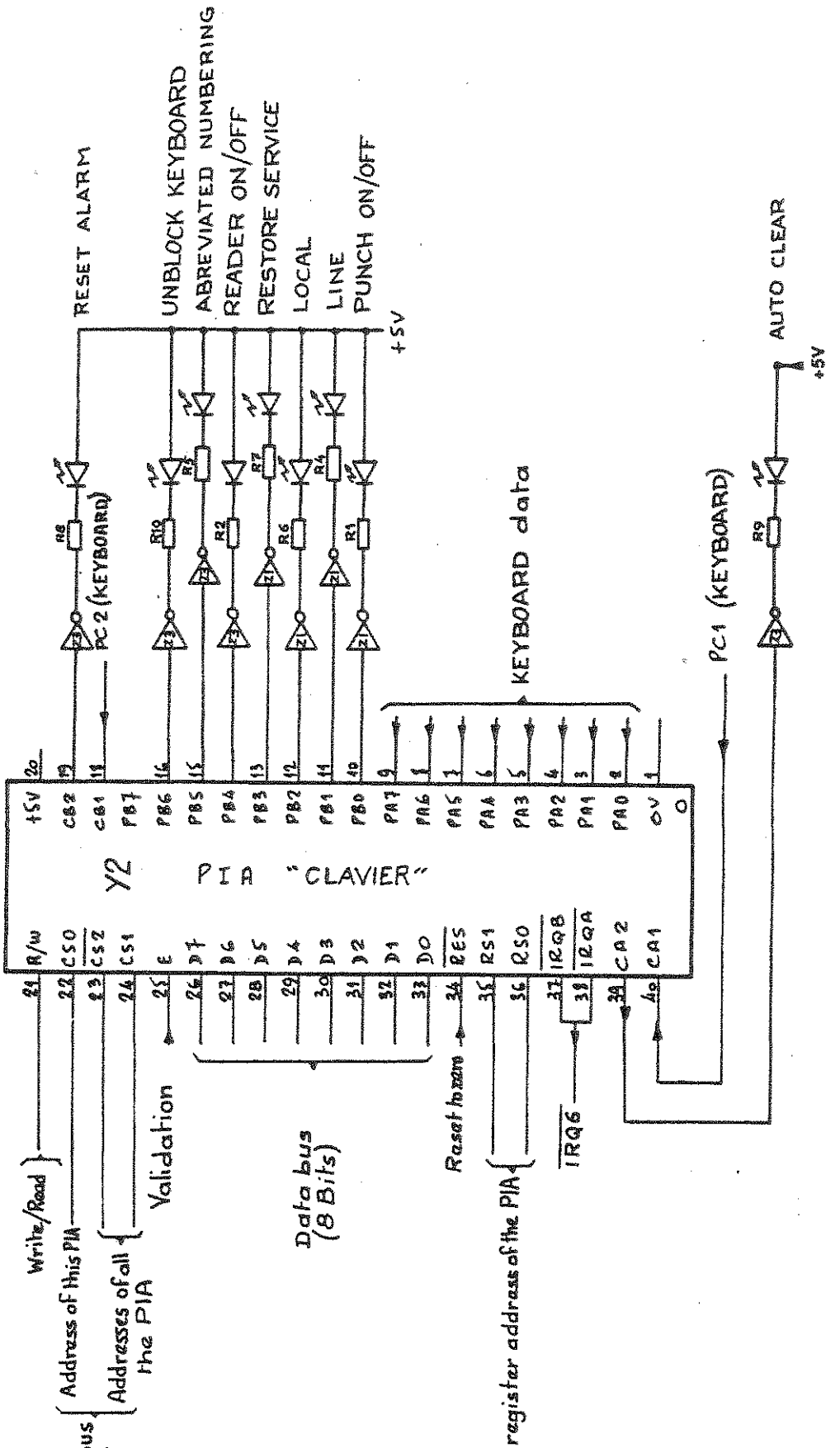
The programmable memory (Z1) code-converts the following signals for the "PIA CLAVIER + MPU" board :

- the 5-units of CCITT code No. 2 ("CL1" to "CL5"),
- the "LETTERS" or "FIGURES" shift ("CL6"),
- "character causing advance" ("CL7"),
- "local control character" ("CL8").

The generation of the "LETTERS" or "FIGURES" character is automatic.

When a key is depressed, signal "PC1" induces the triggering of a count in MPU (X5) of "PIA CLAVIER + MPU" board. After 1 second, if the signal "PC2" corresponding to the releasing of the key has not cancelled the count, the character is transmitted repeatedly.

The switch (SW1) allows selection of fast typing on two or several keys. According to its position, (SW1) applies a logic level «0» or «1» to terminal (2) of the KEYBOARD encoder (Z2).



KEYBOARD input_output circuit

2.2 KEYBOARD INPUT-OUTPUT CIRCUIT

("PIA CLAVIER + MPU" board)

The input-output circuit (Y2) is addressed by signals (CS0, CS1 and $\overline{CS2}$). One of the registers of the input-output circuit (Y2) is selected by signals (RS0, RS1).

The character presence signal "PC1" supplied by the KEYBOARD triggers the interrupt request of part A ($\overline{IRQA}$) towards the PIA IT/ADA input-output circuit (X4) of the "PIA ERD + IT/ADA" board. The signals "CL1" to "CL8" supplied by the KEYBOARD appear at inputs (PA0 to PA7) of the KEYBOARD input-output circuit (Y2). The outputs (PB0 to PB6) control the amplifiers (Z1 and Z3) of the OPERATIONAL CONSOLE light-emitting diodes corresponding to the selection functions.

The character presence signal "PC2" supplied by the KEYBOARD triggers the input-output circuit (Y2). "CB1" controls the interrupt request of part B ($\overline{IRQB}$) to the input-output circuit PIA IT/ADA (X4) of the "PIA ERD + IT/ADA" board.

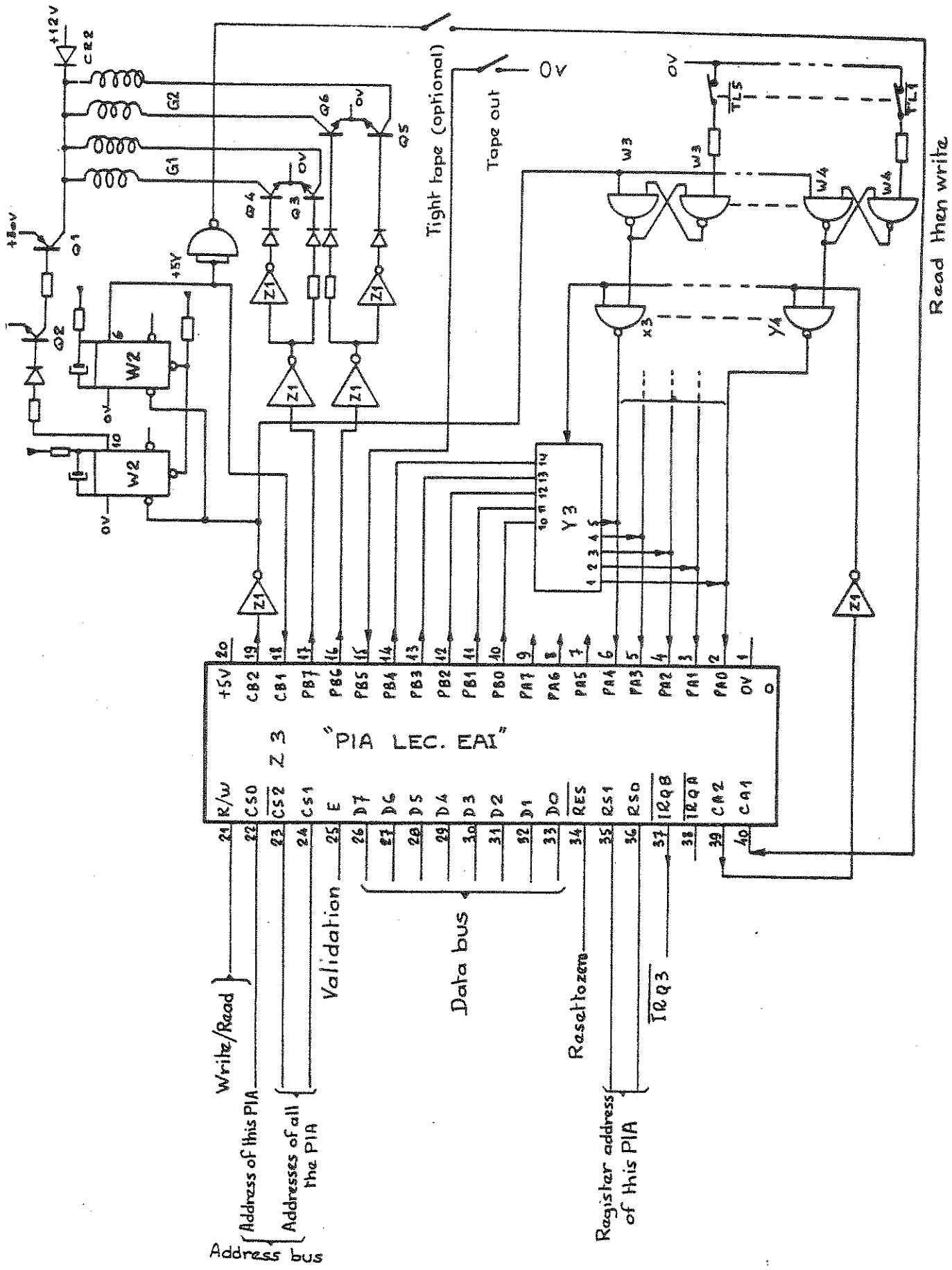
Resetting is obtained by the application of the "restart" signal on ($\overline{RES}$).

2.3 OPERATIONAL CONSOLE

(OPERATIONAL CONSOLE, "CLAVIER", "PIA CLAVIER + MPU" boards)

In the same way as the KEYBOARD keys, the control keys of the OPERATIONAL CONSOLE select the KEYBOARD encoder. The 7 inputs (X1 to X7) associated with the 2 outputs (Y8 and Y9) generate local controls.

The OPERATIONAL CONSOLE controls are displayed by light-emitting diodes. Resistors (R1 to R10) are connected in series with the light-emitting diodes in order to limit the current.



TAPE READER and ANSWER-BACK UNIT

input-output circuit

3 – PUNCHED TAPE READING (TAPE READER, «PIA LECTEUR + AMPLI» board)

3.1 TAPE READER

3.1.1 Characteristics of TAPE READER

- Maximum reading speed : 15 c/s
- Reading mode : character by character
- Character visibility during reading
- Nominal thickness of tape (DIN 6720) : 0.1 mm
- Maximum thickness of tape with sticker : 0.3 mm.

3.1.2. Characteristics of tape feed system

- Motor power supply voltage : 30 V
- Sustaining voltage : 12 V.

3.2 TAPE READER AND ANSWER-BACK UNIT INPUT-OUTPUT CIRCUIT ("PIA LECTEUR + AMPLI" board)

3.2.1 General

The "PIA LEC.EAI" input-output circuit (Z3) supplies certain common signals to the TAPE READER and the ANSWER-BACK UNIT and receives signals from them.

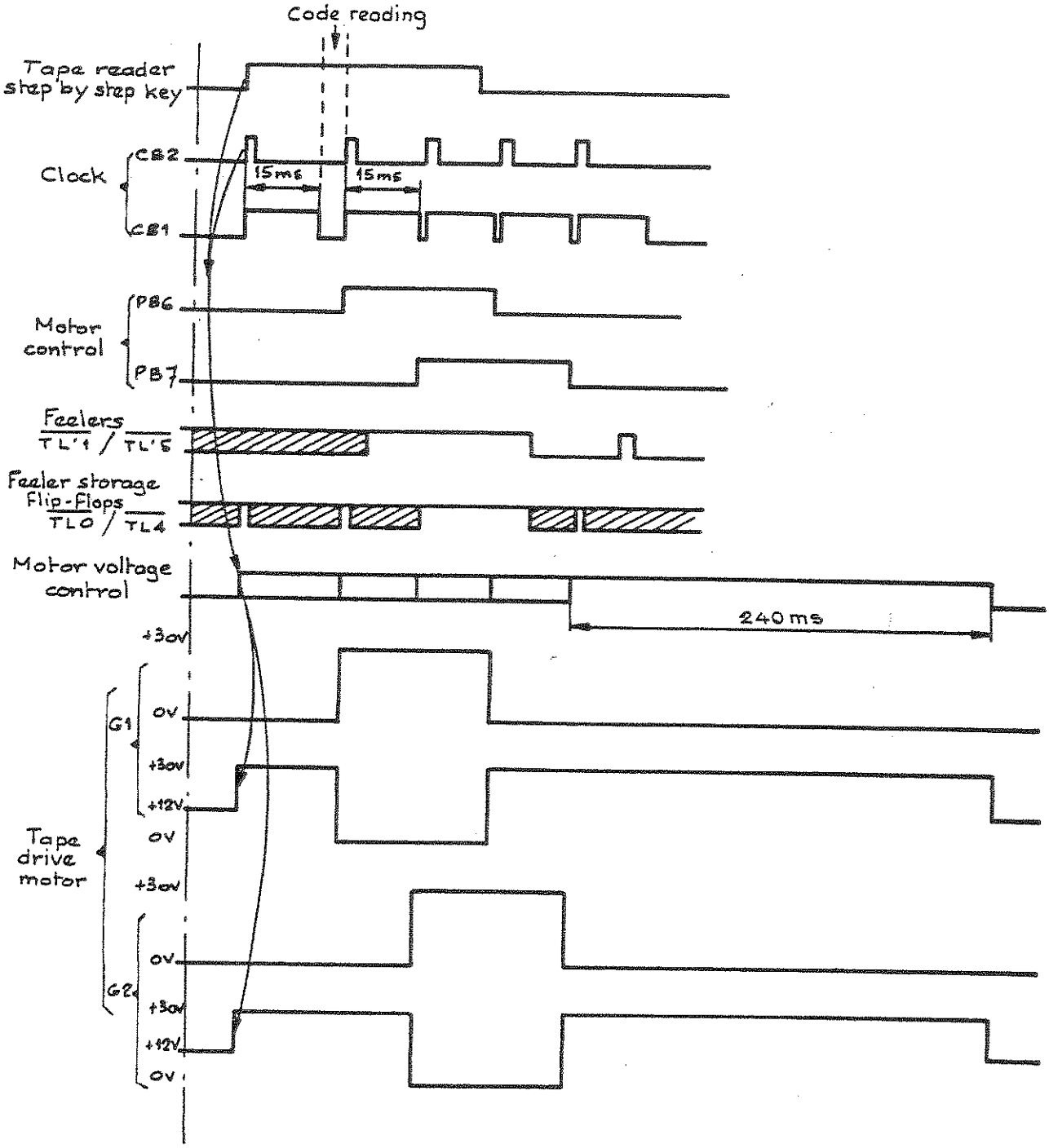
1) The tape reader consists of :

   - a reader tape feed function ensured by a four-phase stepper motor making 48 steps per revolution. The motor controls the movement of the sprocket wheel via a 1:3 ratio demultiplication to provide 4 motor steps per tape transport step,
   - a function acknowledging character punched on the tape ; reading is made by feelers.

2) The answer-back code is stored in a programmable memory (Y3).

3.2.2 Operation

The phases of the tape drive motor are supplied through transistor (Q1) at a voltage of + 30 V during the operation of the TAPE READER. When the TAPE READER is stationary, the diode (CR2) switches the voltage to + 12 V in order to maintain torque on the motor.



TAPE READER Signal timing diagram

The signal "CB2" from the "PIA LEC. EAI" input-output circuit (Z3) triggers :

- a monostable (W2-6)(pulse duration 15 ms typ.) designed to inform the microprocessor that it can, if necessary order another motor step,

- another monostable (W2-10)(pulse duration 240 ms typ.) controlling the motor power supply 12 V/30 V voltage switching circuit.

When the TAPE READER is stationary, the feelers detect a hole in the tape (corresponding to a codification "1" of CCITT code No. 2) and cause a status "0" to appear at the input of the flip-flops (X3, W3, W4) which store the status of the feelers "$\overline{TL0}$" to "$\overline{TL4}$".

The character read is acknowledged by the control logic just before the first transition of the motor phases.

The storage flip-flops are reset to zero by the next "CB2" pulse.

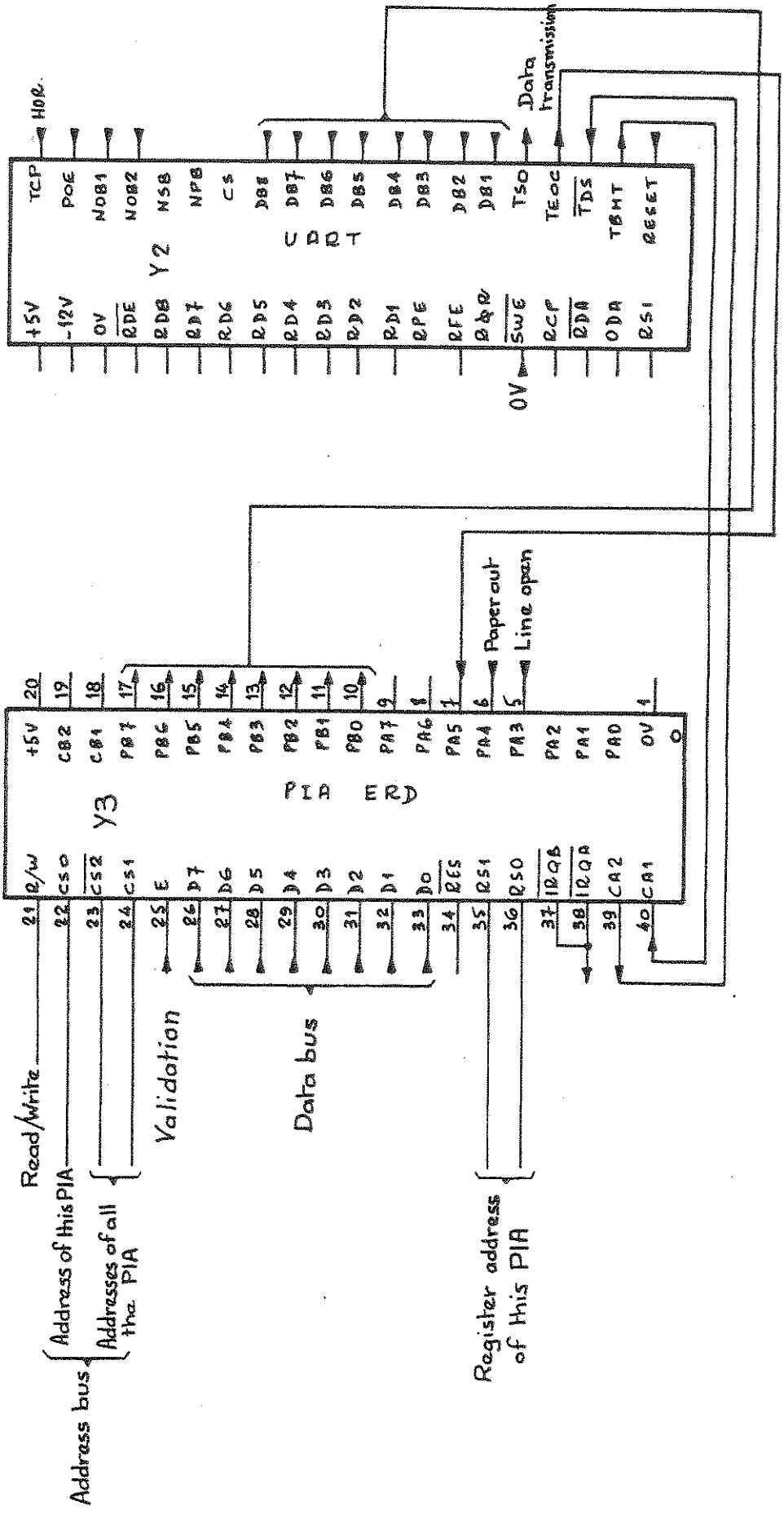
Signal "CA2" validates :

- either the TAPE READER ("CA2" = 0),

- or the answer-back code memory ("CA2" = 1).

A "tape out" wire is connected at (PB5) of the input-output circuit (Z3). A logic state indicated by a feeler denotes that a tape is present in the TAPE READER. The two wires leading to the "tight tape" contact(option), are connected to the "PIA LECTEUR + AMPLI" board. The contact applies the signal from monostable (W2-6) to the input (CA1), thus interrupting the tape transport by the program.

The 5-units from the answer-back code memory are "OR WIRED" with the 5-units of the TAPE READER. The memory circuit (Y3) is addressed by the input-output circuit (Z3) and supplies it with the 20 characters of the answer-back code.



Transmission input-output circuit

4 – TRANSMISSION - RECEPTION
(«PIA ERD + IT/ADA» and «ADAPTATION» boards)

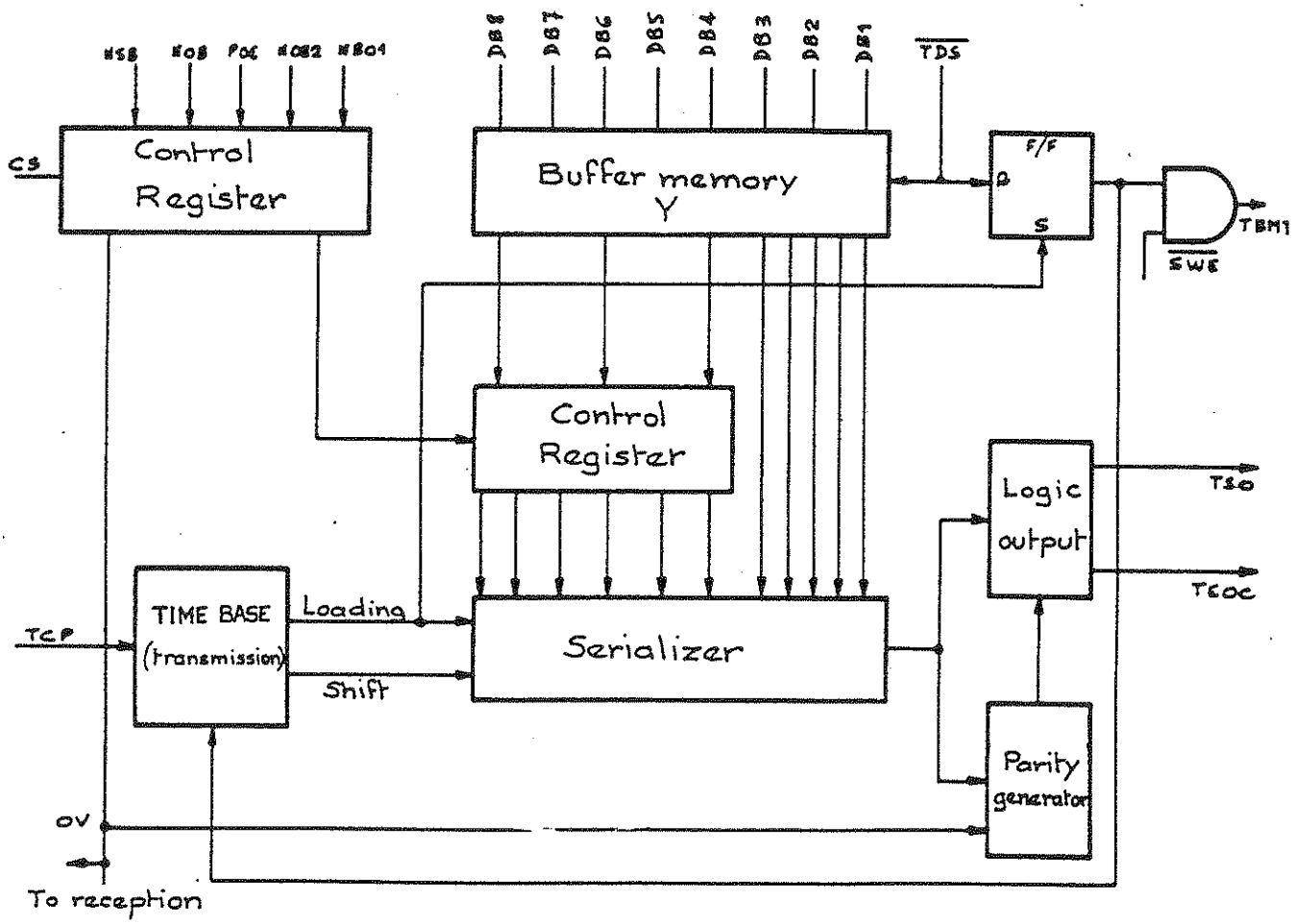
4.1 GENERAL

The "transmission and reception" circuit consists of : a "PIA ERD" input-output circuit (Y3), an "UART" Universal Asynchronous Receiver-Transmitter circuit (Y2), both located on the "PIA ERD + IT/ADA" board, and the components required to adapt the unit to the transmission path.

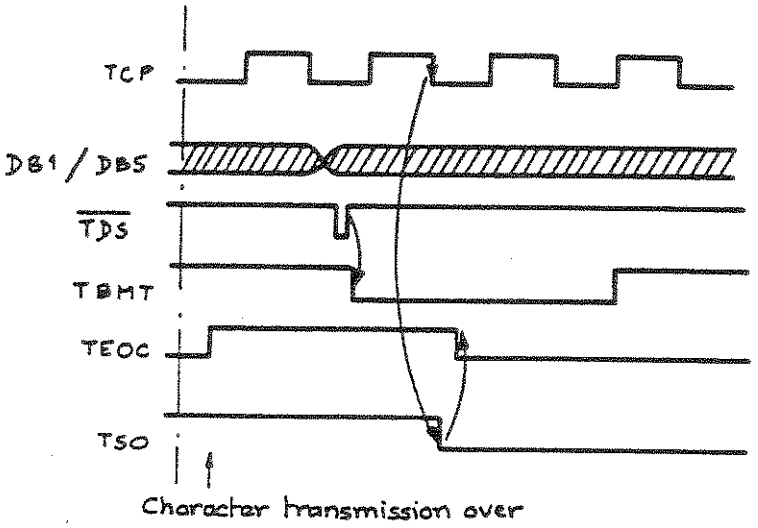
4.2 TRANSMISSION INPUT-OUTPUT CIRCUIT

("PIA ERD + IT/ADA" board)

Part of the "UART" circuit (Y2) generates the transmission function. The input ($\overline{SWE}$), connected to the logic 0 V, selects the output (TBMT) at level TTL. The inputs (POE, NOB1 and NOB2) of the control register select the code used and the parity. The clock signal "HOR" , from the "PIA CLAVIER + MPU" board, controls the transmission time base in (Y2), through input (TCP). The (Reset) input uses a logic level "1" to clear all the registers and counters of (Y2).



The 8-units "PB0" to "PB7" of the character to be transmitted, from input-output circuit "PIA ERD" (Y3), appear at inputs (DB1 to DB8) of the UART circuit (Y2). A level 0 pulse at input ($\overline{TDS}$), enables data input into the buffer memory. The "start" signal is generated on the first trailing edge of the "TCP" clock signal after "$\overline{TDS}$" has been returned to "1". A leading edge of the "TEOC" signal indicates that the transmission of the character and the "stop" signal is over ; this "1" level is held until the trailing edge of the next "start" signal occurs. The "TBMT" signal indicates that the preceding character of the buffer memory has been transferred into the serializer and that another character can be taken into account. The character is transmitted by the output (TSO) of (Y2).

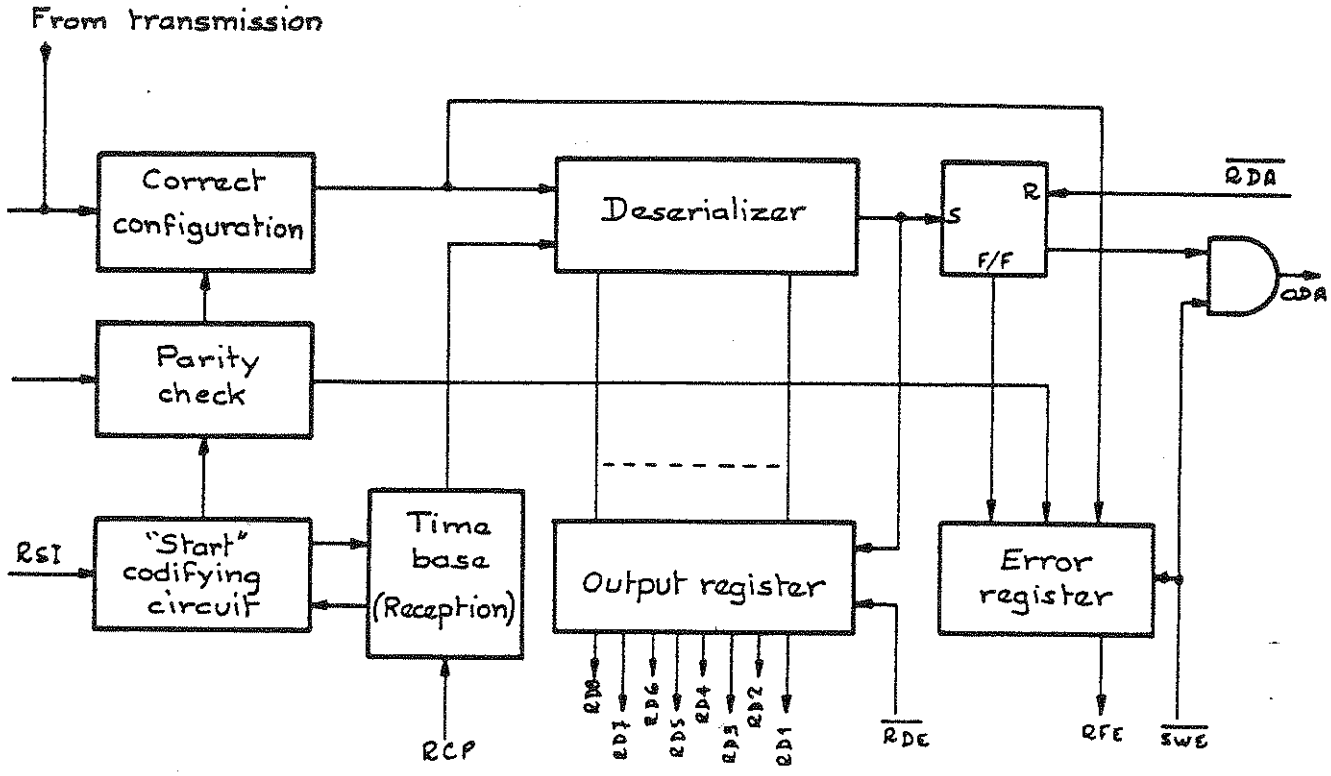


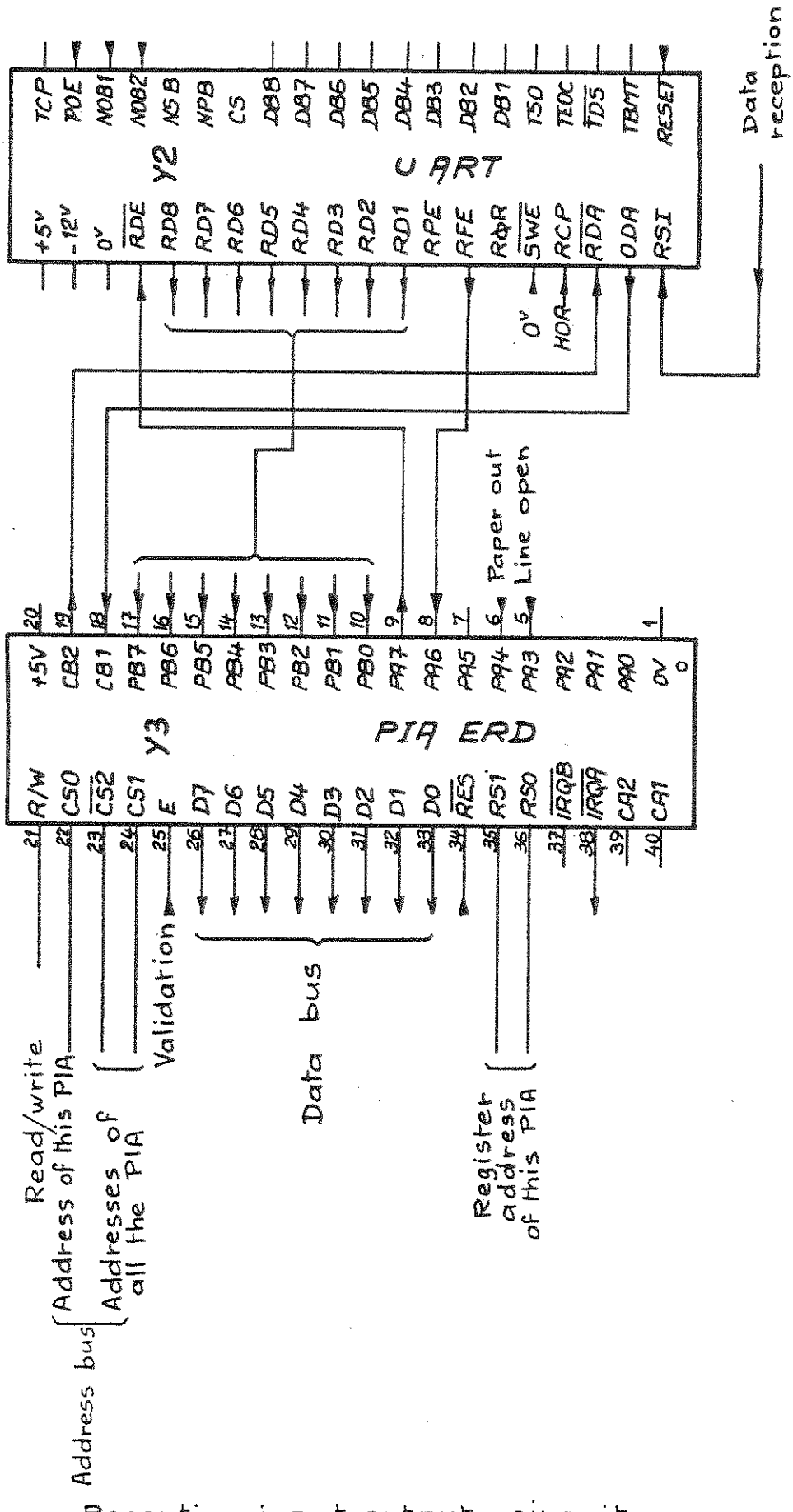
Timing diagram of transmission function

4.3 RECEPTION INPUT-OUTPUT CIRCUIT

("PIA ERD + IT/ADA" board)

One part of the UART circuit (Y2) generates the reception function. The inputs ($\overline{SWE}$ and $\overline{RDE}$), connected to logic 0 V, select the "ODA" output at TTL level. The clock signal "HOR", coming from the "PIA CLAVIER + MPU" board, controls the reception time base in (Y2) through the input (RCP).

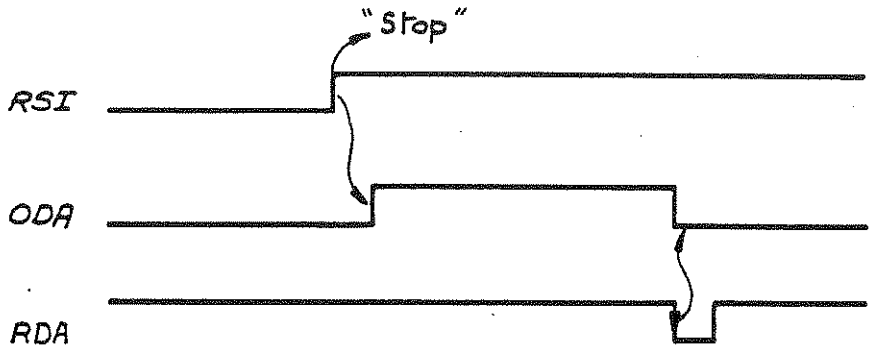




Reception input-output circuit

The character is received at input (RSI). A logic level "1" on the output (ODA) indicates that the complete character has been received and transferred into the output register. The data (RD1 to RD5) is then presented at the output of the UART circuit (Y2) at the last significant unit of the character. The unused outputs (RD6 to RD8) remain constantly at zero. The output (ODA) is reset to zero by the trailing edge of a pulse which appears at input ($\overline{RDA}$). The output (RFE) changes to "1" in the event of incorrect character constitution ("start", units, "stop").

The detection of "paper out" and "line open" inform the microprocessor that it must produce the corresponding interrupts.



Timing diagram of reception function

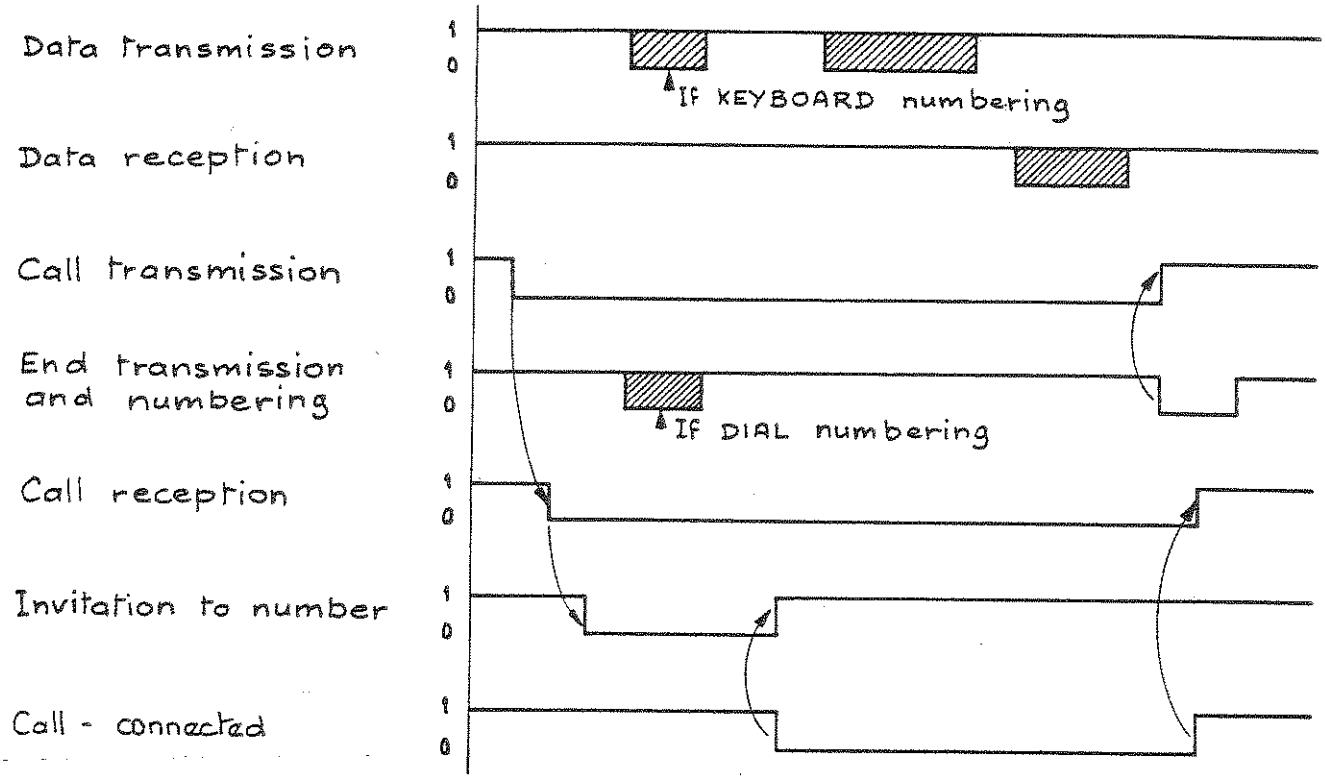


Diagram of data transferred during call transmission

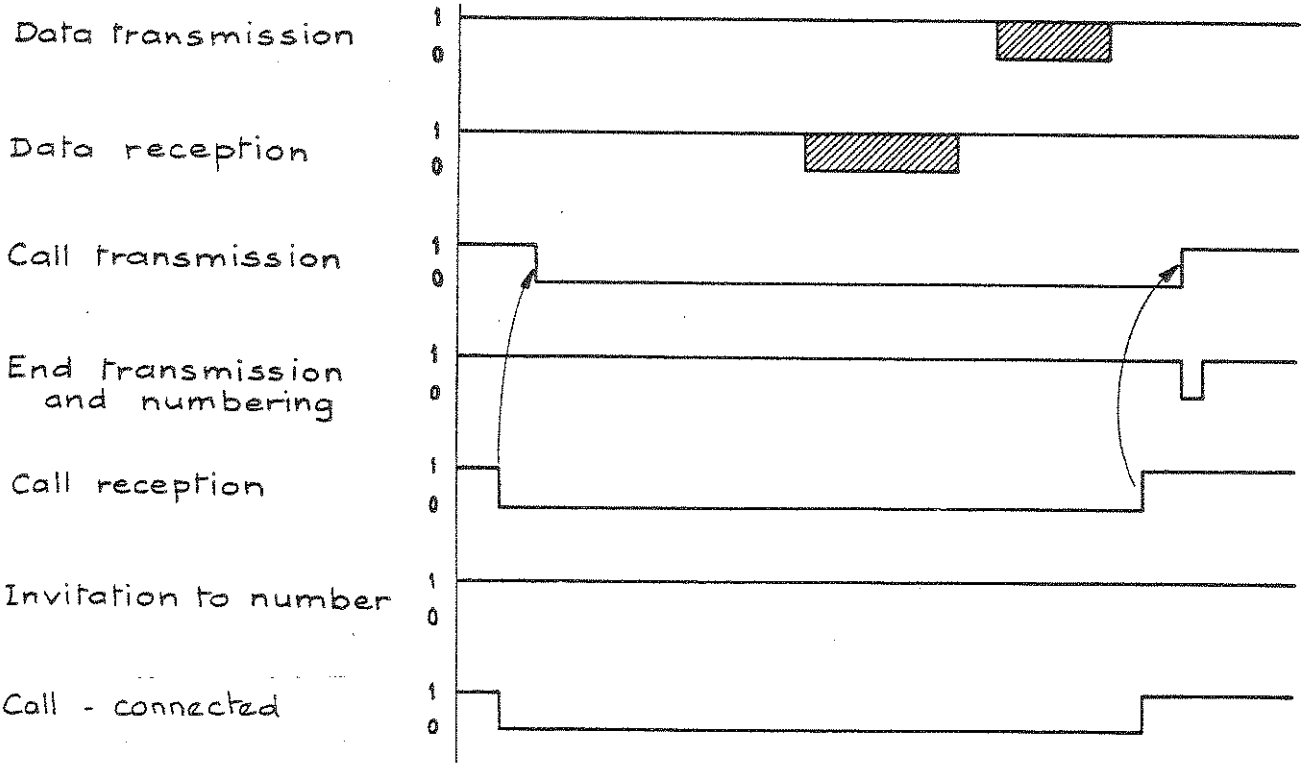


Diagram of data transferred during call reception

4.4 MANAGEMENT OF TRANSMISSION PATH SUPERVISION DATA

("PIA ERD + IT/ADA" board)

Transmission path supervision is obtained by the ADAPTATION board of the unit. The real time clock consisting of two monostables (Y1-7) and (Y1-9) (see NOTE) permanently provides the various timing pulses required.

The circuit supervising the transmission path informs the microprocessor, through the "PIA IT/ADA" input-output circuit (X4), which answers it according to the following preestablished timing sequence :

1) Calling subscriber

- Call transmission : the output (PA7) of PIA changes to level "0" and stays there until the "end transmission" occurs.
- Call reception (call acknowledgement) : if the call has been received, the output (PA5) of PIA receives a logic level "0" which remains present until the "call-connected" disappears.
- Invitation to number : the input (PA4) of PIA receives a logic level "0" which changes to "1" when the "call-connected" appears.
- Numbering : if the numbering is made from the KEYBOARD, it is transmitted to the "data transmission" output (TS0) of the UART circuit (Y2). If a DIAL is used for numbering, the number is transmitted to the PIA output (PA6).
- Call - connected : when the call has been put through, the output (PA3) receives a level "0".
- End transmission : the output (PA6) of PIA changes to "0" at the end of the call thus bringing the "call transmission" signal to level "1".
- The end of the call is confirmed by a logic "1" which appears at the "call reception" input (PA5) and by "call-connected" at (PA3).

2) Called subscriber

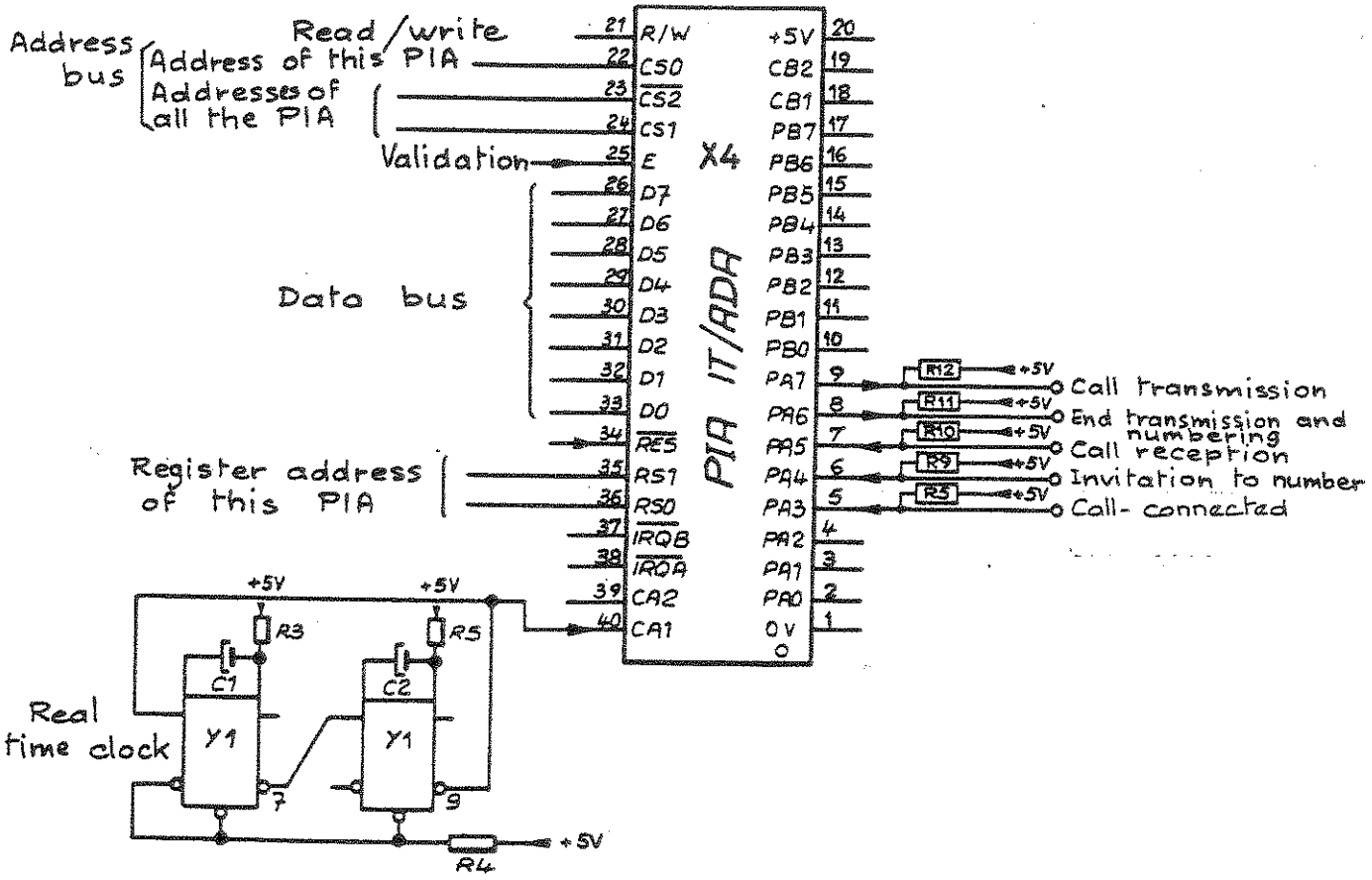
- Call reception and call-connected : the inputs (PA3) and (PA5) receive a level "0" which is held throughout the call.
- Call transmission : the output (PA7) changes to level "0" to confirm call reception and is held there until the end of call information is received.
- End of call returning "call-connected" "(PA3) and "call reception" (PA5) to level "1".

NOTE : Monostable (Y1-7) signifies : monostable corresponding to ouput (7) of package (Y1).

(Y1-9) pulse duration : 1.8 ms typical.

(Y1-7) pulse duration : adjusted through R6 ("PIA ERD + IT.ADA") in such way that t(Y1-7) + t(Y1-9) = 20 ms.

- End transmission : the end of the call is detected by a change of state of "call reception". "PIA" transmits a level "0" to (PA6) which resets call transmission (PA7) to "1" thus confirming a break in the call by switching the correspondent's "call reception" and "call-connected".



4.5 AUXILIARY DEVICES, ALARMS

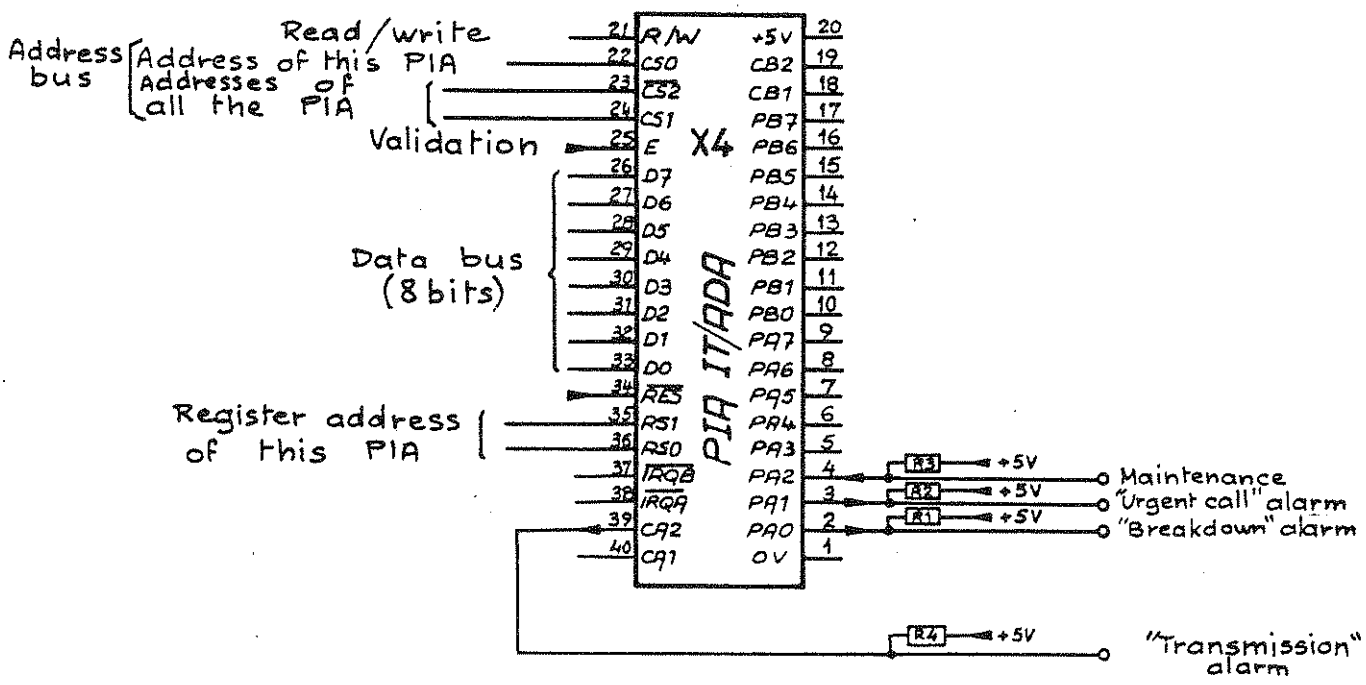
("PIA ERD + IT/ADA" and "ADAPTATION" boards)

The "Maintenance" signal coming from some types of "ADAPTATION" boards applies a logic "0" to the input (PA2) of the "PIA IT/ADA" input-ouput circuit (X4) in certain configurations of the unit on-line. The switching of this signal to the high level prevents the use of the unit in the "LOCAL" mode.

When a received call is accompanied by an audible alarm control ("FIGURES" J), the "urgent call alarm" signal from output (PA1) of PIA changes to level "0".

The "breakdown alarm" signal at output (PA0) of PIA, repeats the OPERATIONAL CONSOLE alarms by changing to zero.

The "transmission alarm" signal, at output (CA2) of PIA changes to "0" for all incoming or outgoing transmissions in synchronization with the "call reception" signal.



4.6 TRANSMISSION PATH ADAPTATION CIRCUITS

("ADAPTATION" board)

See the TECHNICAL DOCUMENT specific to ADAPTATION.

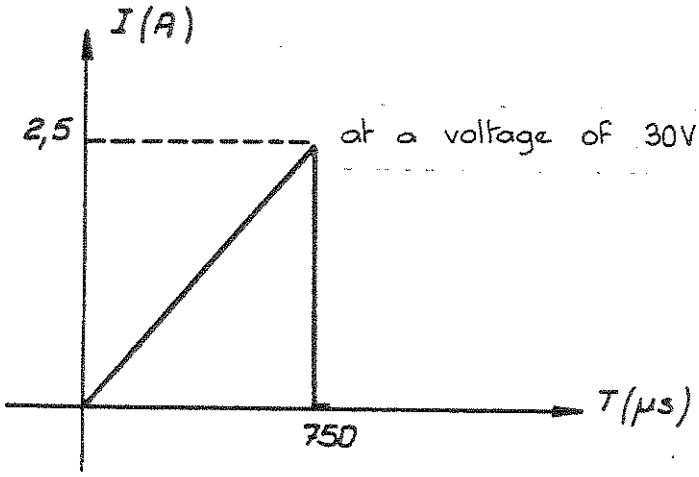
5 – PRINTING

5.1 PRINTING DEVICE

5.1.1 Characteristics

-- Writing speed	: 15 characters/s
-- Electromagnet power supply voltage (see NOTE)	: 30 V ± 2 %
-- Electromagnet excitation time (see NOTE)	: 750 µs ± 10 µs

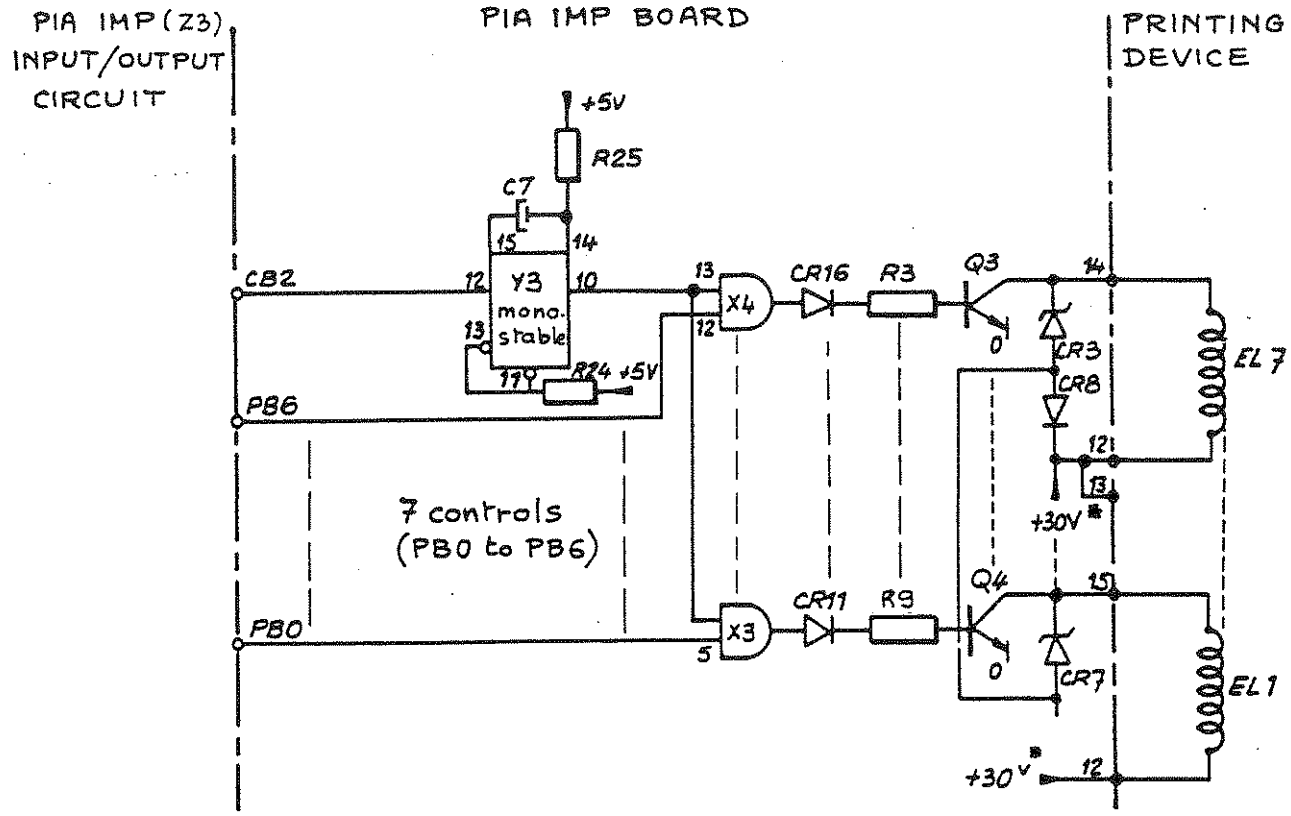
NOTE : The electromagnets are excited by a signal with the following characteristics :



5.1.2 PRINTING DEVICE INPUT-OUTPUT CIRCUIT

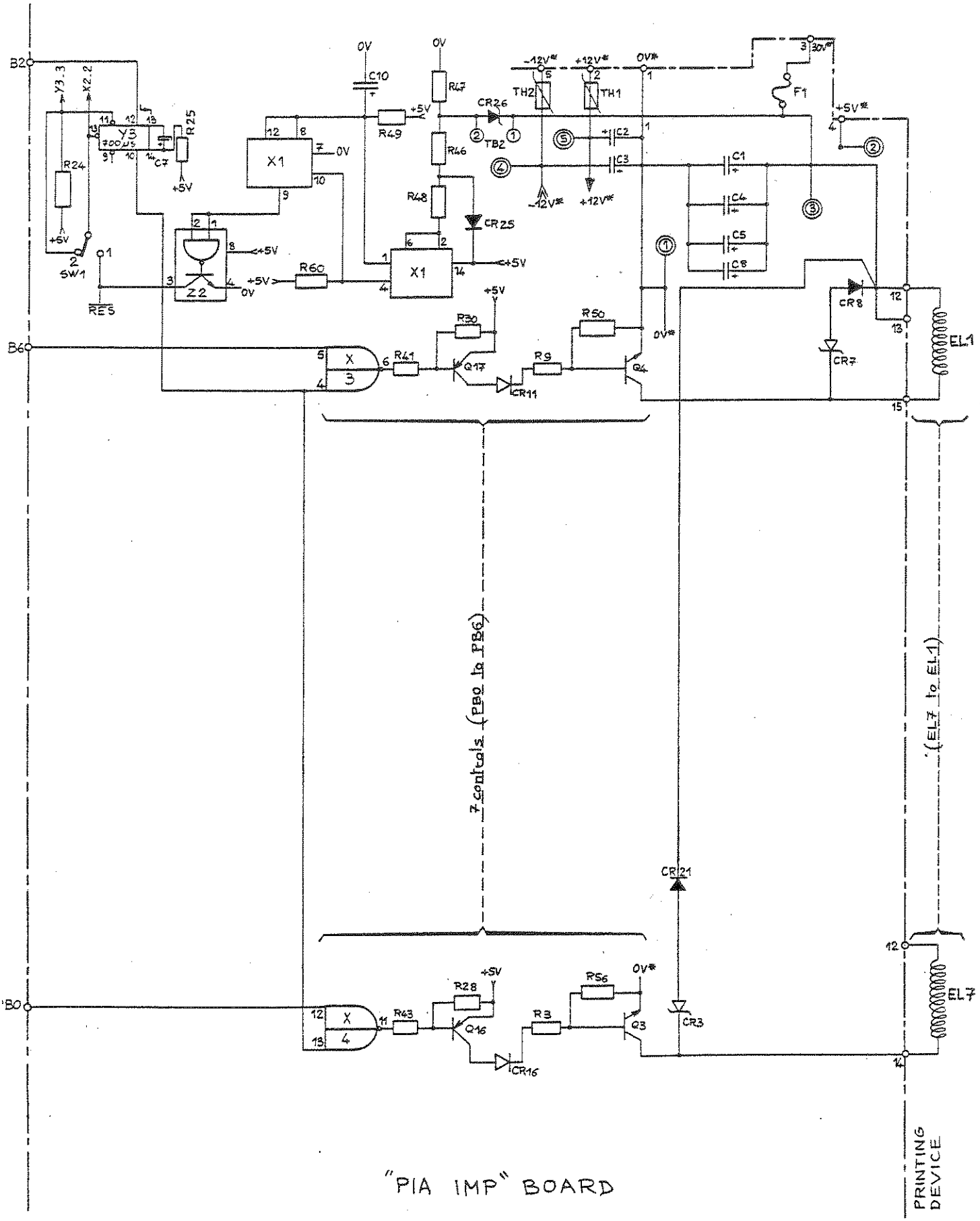
(«PIA IMP» board, plate 5-1)

The control of the 7 electromagnets (EL1 to EL7) of the PRINTING DEVICE needles is provided by 7 identical amplifiers. The amplifiers are controlled by signals "PB0" to "PB6" supplied by the "PIA IMP" input-output circuit (Z3).



The needle controls "PB0" to "PB6" are validated by a pulse supplied by the monostable (Y3). The monostable is triggered by the signal "CB2" from the "PIA IMP" input-output circuit (Z3).

The diodes (CR1 to CR8), connected in parallel to the coils of the electromagnets (EL1 to EL7), clamp the overvoltages at the blocking of transistors (Q1 to Q7) controlling the electromagnets.


"PIA IMP" BOARD
PRINTING DEVICE
7 controls (PB0 to PB6)
(EL7 to EL1)
B2
B6
B0
Y3.3
X2.2
Y3
700µs
C7
R25
R24
SW1
RES
X1
Z2
C10
R47
R49
R46
R48
CR26
CR25
TB2
TH2
TH1
-12V*
+12V*
0V*
30V*
F1
+5V*
C1
C2
C3
C4
C5
C6
R60
R30
R41
Q17
R9
CR11
R50
Q4
CR8
CR7
EL1
CR21
R28
R43
Q16
R3
CR16
R56
Q3
CR3
EL7

5.1.3 Complementary data

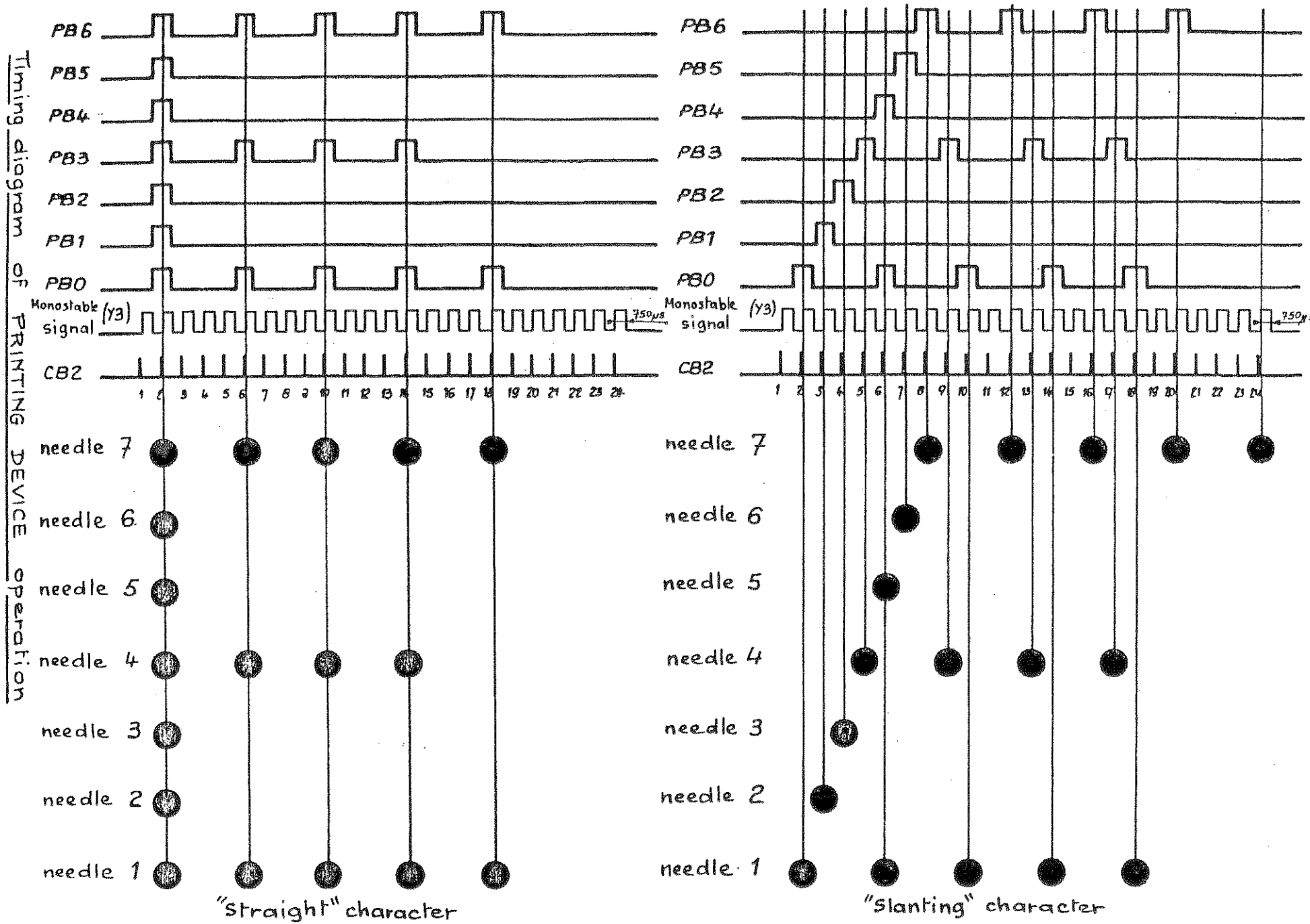
SUPERVISION OF + 30 V*

(«PIA IMP» board, plate 5-2)

In case of absence of PRINTING DEVICE control voltage (+ 30 V*) (i.e. fuse F1 blowed) or if its value is lower than 21 V for over 80 ms, a reinitialization of the unit is triggered automatically.

As much as the default persists, that reinitialization is maintained permanently, and the unit cannot be utilized.

That function is realized through a circuit constituted by triggers (X1) which control the signal «RES» (Restart) through the amplifier (Z2).


Timing diagram of PRINTING DEVICE operation
PB6
PB5
PB4
PB3
PB2
PB1
PB0
Monostable signal (Y3)
750μs
CB2
needle 7
needle 6
needle 5
needle 4
needle 3
needle 2
needle 1
"Straight" character
"Slanting" character

5.2 ADVANCE AND RETURN-TO-BEGINNING OF LINE SYSTEM

(SENSOR, "ASSERVISSEMENT" board, POWER AMPLIFIER, DRIVE MOTOR)

NOTE CONCERNING THIS PARAGRAPH: The symbol * , following some signals allows them to be distinguished from their homonyms (e.g. "Col" and "Col*").

5.2.1 General

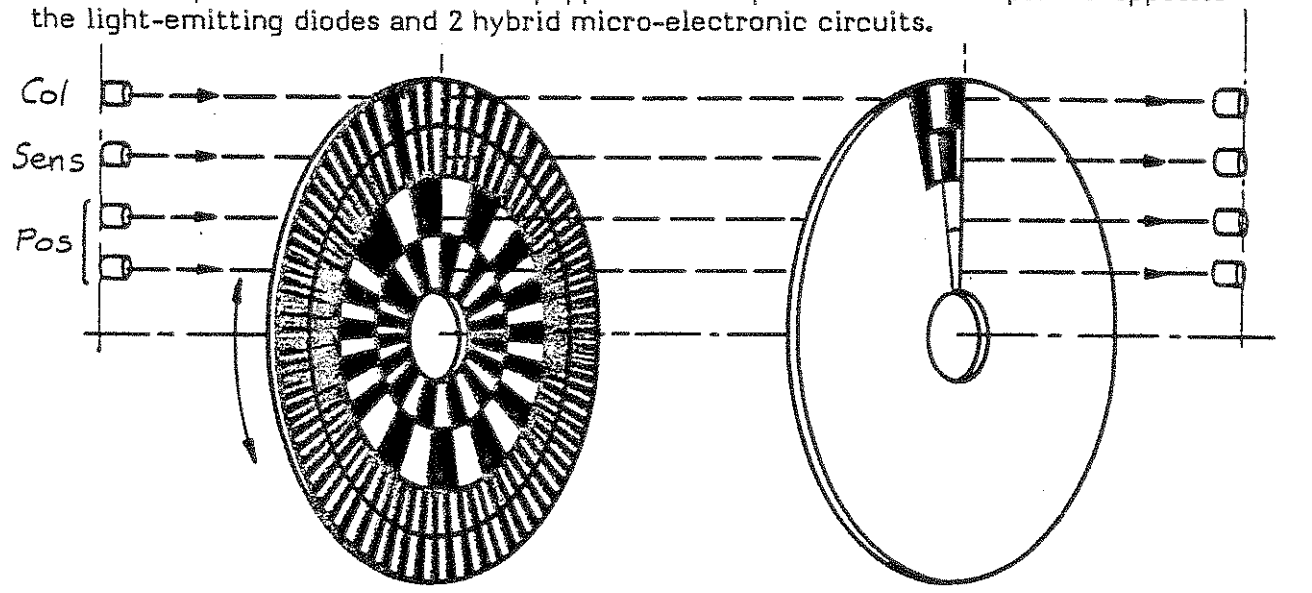
The advance and return-to-beginning of line system consists of several functional units :

- SENSOR
- Logic data generator circuit
- Tachogenerator
- Digital-to-analog converter
- Servo controls
- Selection and summing circuit
- DRIVE MOTOR amplifier
- DRIVE MOTOR

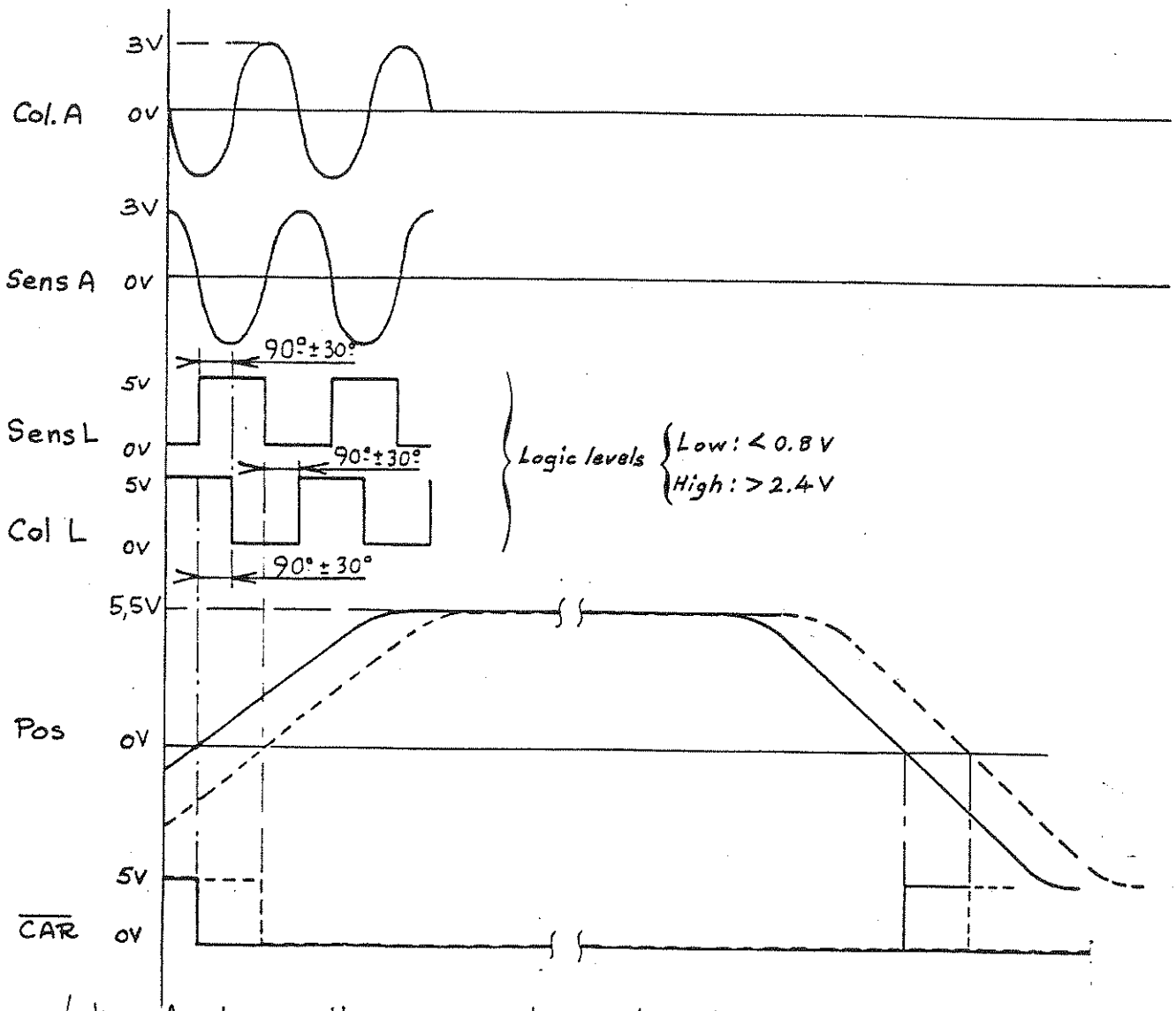
5.2.2 SENSOR

The SENSOR basically consists of :

- a transmitter printed circuit board equipped with 4 light-emitting diodes placed along the same radius,
- a mobile glass disc representing 4 coaxial tracks, each formed of alternating black and transparent sectors, i.e. :
  - track 1 known as Column "Col" ,
  - track 2 known as Direction "Sens",
  - track 3 known as Negative Position "Pos -",
  - track 4 known as Positive Position "Pos +",
- a fixed mask or diaphragm, made of glass and containing a window consisting of 4 coaxial tracks, i.e. :
  - track 1 known as Column "Col",
  - track 2 known as Direction "Sens",
  - track 3 known as Negative Position "Pos -",
  - track 4 known as positive Position "Pos +",
- a receiver printed circuit board equipped with 4 photo-transistors placed opposite the light-emitting diodes and 2 hybrid micro-electronic circuits.



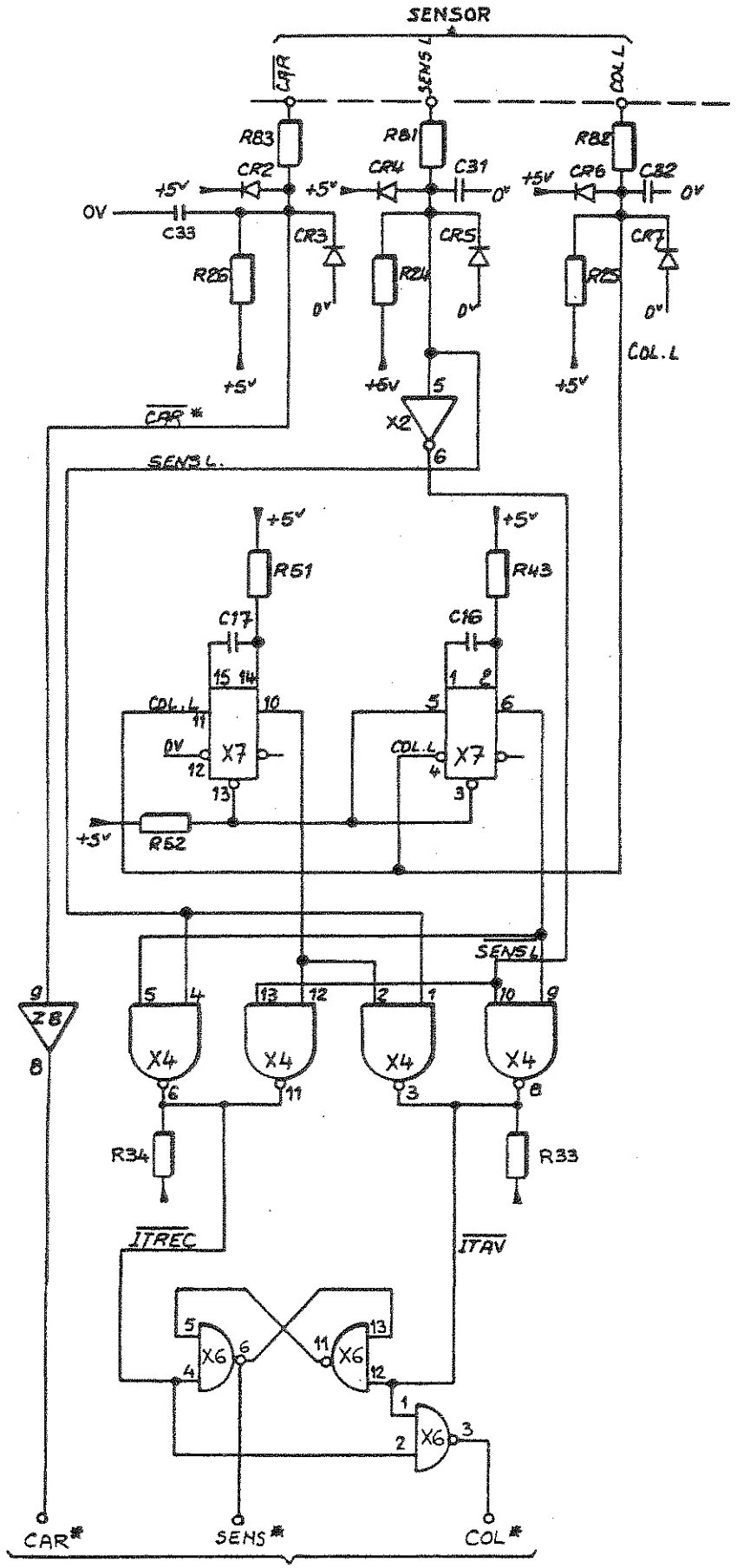
The micro-electronic circuit amplifies the "Col" and "Sens" signals with a constant gain. The "Pos +" and "Pos -" signals drive a differential amplifier whose output supplies the "Pos" synthesis signal. The "Col" and "Sens" signals are amplified and output directly in the form of Analog Column signal "Col A" and Analog Direction signal "Sens A". They are used to generate the Logic Column signal "Col L" and Logic Direction signal "Sens L". The "Pos" signal is used to generate the Character logic signal "$\overline{CAR}$".



Note: Analog voltages are typical values.

Timing diagram of signals supplied by the SENSOR

A character represented by one period of the «$\overline{CAR}$» signal contains 14 columns, i.e.14 low to high edges or high to low edges.



"PIA IMP" board, "PIA IMP" input-output circuit (Z3)

Logic data generator circuit

5.2.3 LOGIC DATA GENERATION CIRCUIT

("ASSERVISSEMENT" board)

The logic data generation circuit consists of :

- a circuit generating "$\overline{\text{ITAV}}$" (drive) and "$\overline{\text{ITREC}}$" (carriage return) interrupt signals,
- a unit converting the "$\overline{\text{ITAV}}$" and "$\overline{\text{ITREC}}$" signals into "Sens*" (direction) and "Col*" (column) signals required by the microprocessor,
- a circuit inverting the "$\overline{\text{CAR}}$" (character) signal.

The "$\overline{\text{CAR}}$" logic signal coming from the SENSOR is complemented by the inverter (Z8-8) (see NOTE) which supplies the "CAR*" signal. The "Col L" (Column Logic) signal from the SENSOR triggers the monostable flip-flops (X7-6) on a low to high edge and (X7-10) on a high to low edge.

The "Sens L" (Direction Logic) signal from the SENSOR is applied directly to the NAND gates (X4-6) and (X4-3) and is also complemented by the inverter (X2-6) the output of which drives the NAND gates (X4-8) and (X4-11).

The resistors (R24 to R26) at + 5 V load the open-collector outputs of the SENSOR.

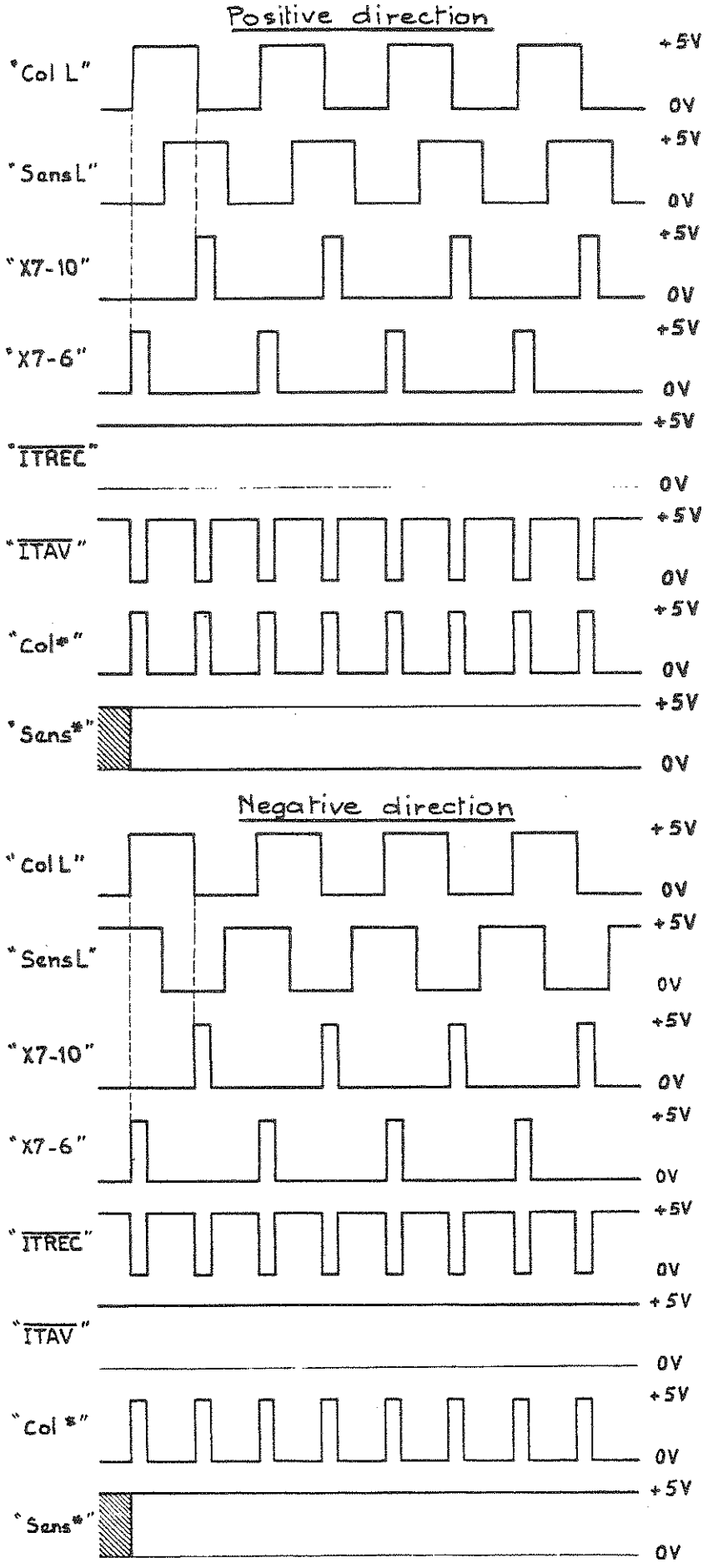
The diodes (CR2 to CR7) protect the logic stages against any possible overvoltages.

Interference present in the input signals are filtered by the following RC circuits :

- "$\overline{\text{CAR}}$" : R83 - C33
- "Col L" : R82 - C32
- "Sens L" : R81 - C31

The gates (X4), loaded by the resistors (R33) and (R34) combine the "Sens L", "$\overline{\text{Sens L}}$" and "X7-6", "X7-10", signals, two by two, in order to obtain the "$\overline{\text{ITREC}}$ and "$\overline{\text{ITAV}}$" signals. (X7-6) and (X7-10) pulse duration : 120 µs typical each.

NOTE : Inverter (Z8-8) signifies the inverter corresponding to ouput (8) of package (Z8).



LOGIC DATA TIMING DIAGRAMS

In the Drive mode, in the positive direction, gates (X4-8) and (X4-3) supply pulses on "$\overline{\text{ITAV}}$" whereas "$\overline{\text{ITREC}}$" obtained from gates (X4-6) and (X4-11) is at level "1". In the Carriage Return mode, in the negative direction, "$\overline{\text{ITAV}}$" changes to "1" and the pulses appears at "$\overline{\text{ITREC}}$".

The RS flip-flop stores the carriage drive or return status on the basis of the "$\overline{\text{ITAV}}$" and "$\overline{\text{ITREC}}$" signals and supplies the "Sens*" signal to the "PIA IMP" input-output circuit (Z3).

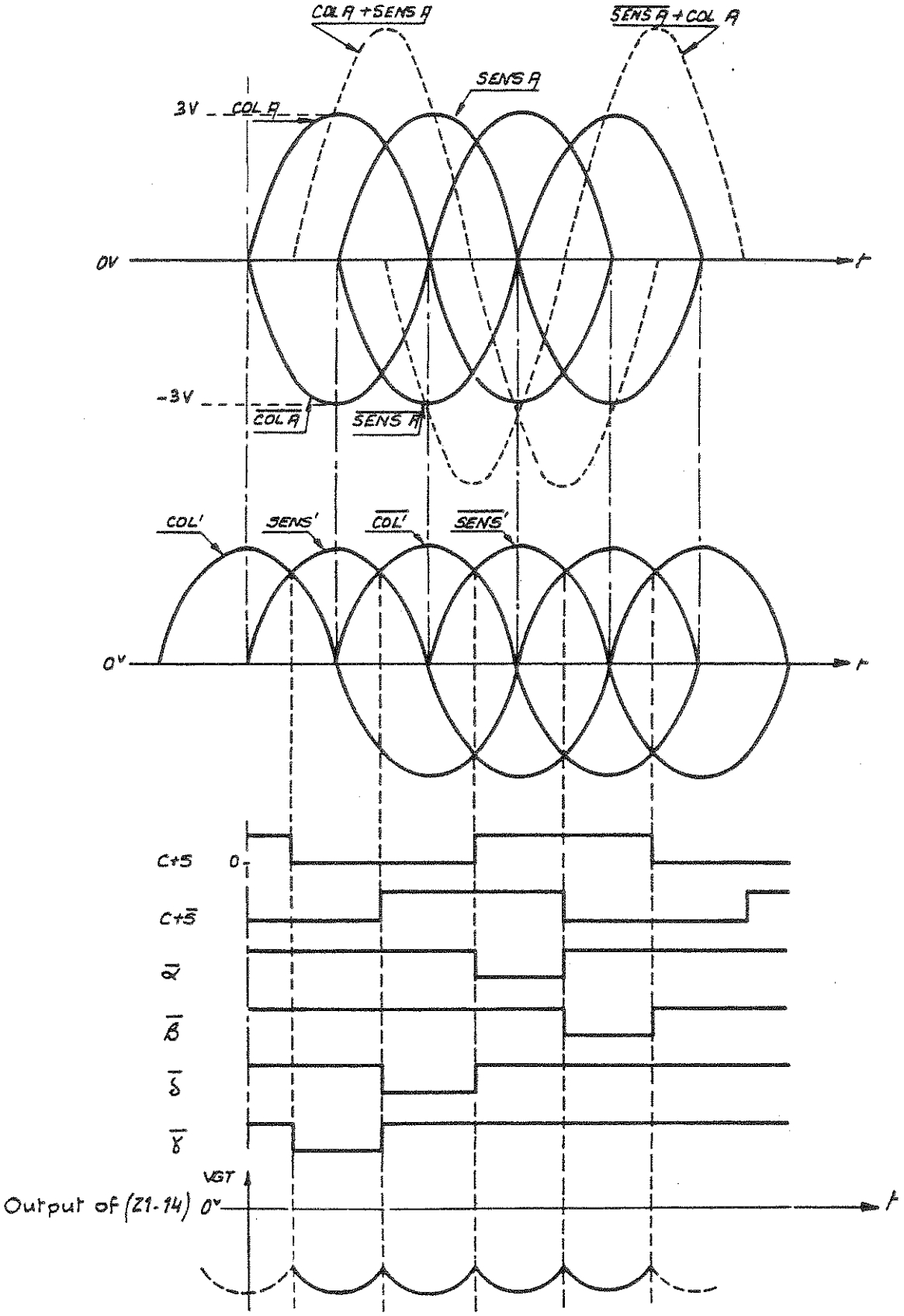
The NAND gate (X6-3) (see NOTE), combines the "$\overline{\text{ITAV}}$" and "$\overline{\text{ITREC}}$" signals to supply the "Col*" signal to the "PIA IMP" input-output circuit (Z3).

The "Sens*" signal informs the microprocessor of the carriage movement mode. The "CAR*" signal enables the microprocessor to down-count the characters in the line of writing from 69 to 32 and then from 31 to 1, in the Carriage Return mode (see paragraph : "Selection and Summing circuit" for down-counting). The "Col*" signal is used for :

- counting the columns of a character in the following mode : Position Servo-control (carriage halt), Speed Servo-control (drive) and Out-of-position Servo-control (position shift),

- for down-counting the 28 columns of the 1st character in the Carriage Return mode at the start of a line, in order to increase the precision of the Servo-control.

NOTE : NAND gate (X6-3) signifies : the "NAND" gate corresponding to output (3) of package (X6).



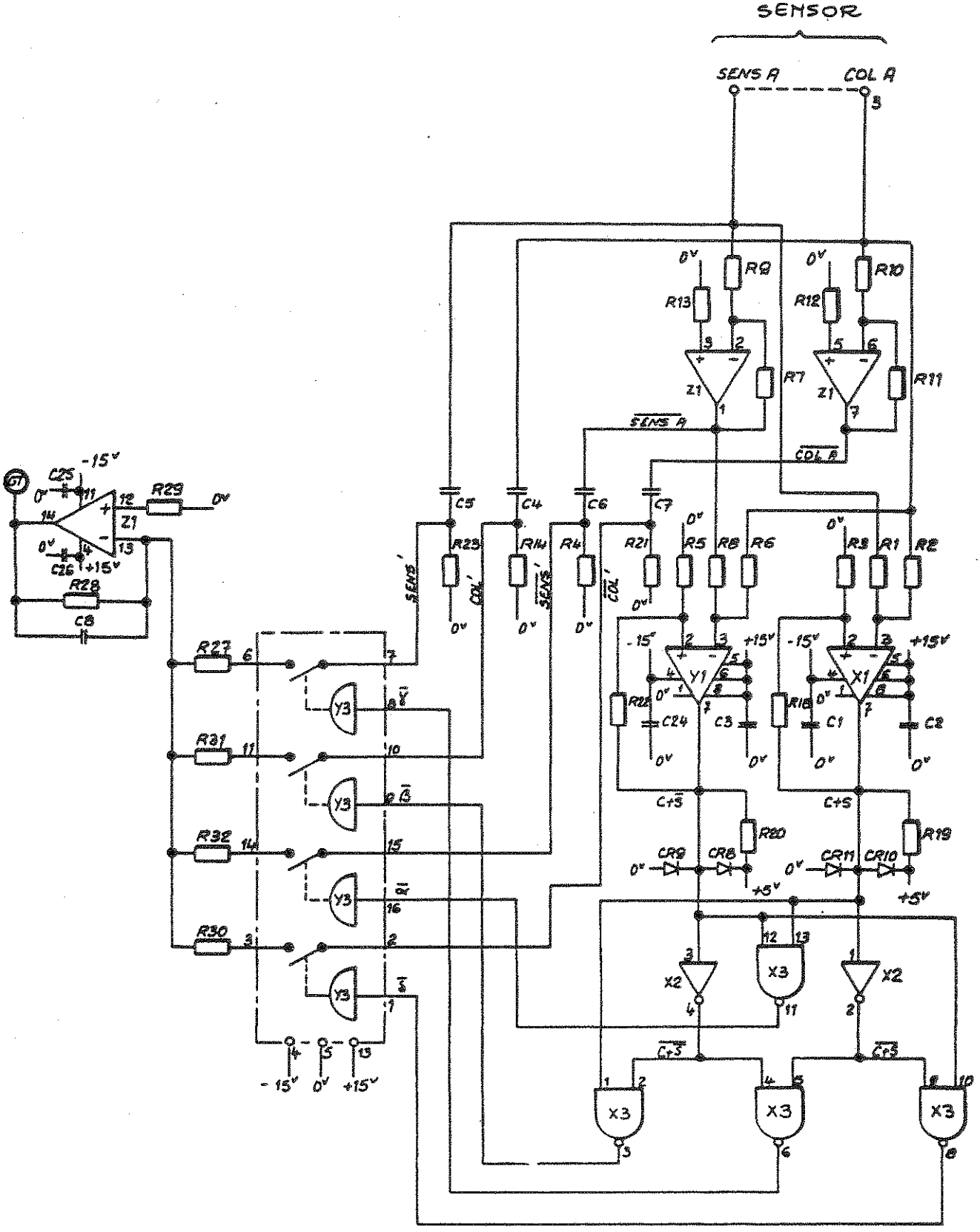
Timing diagram of tachogenerator

5.2.4 Tachogenerator

("ASSERVISSEMENT" board)

The Tachogenerator consists of an electronic circuit generating the true speeed signal from analog coming from the SENSOR.

The SENSOR supplies analog "Sens" (direction) and "Col" (column) signals with a constant amplitude and a variable frequency proportional to the speed of rotation of the mobile disc, i.e. to the speed of movement of the carriage. From the derivative of the signals and their complements, 4 signals are obtained, phase-shifted 90° with respect to one another, and whose amplitude is proportional to the frequency. By combining the basic signals and their complements, the electronic circuit generates logic signals used for sampling the higher or lower peaks of the derived signals and, according to the direction of rotation, provide a d-c voltage the instantaneous value of which is directly proportional to the true speed of the carriage at that moment.



Tachogenerator

The "Sens A" and "Col A" signals from the SENSOR are inverted by the operational amplifiers (Z1-1) (See NOTE) and (Z1-7) in order to obtain the "$\overline{\text{Sens A}}$" and "$\overline{\text{Col A}}$" signals.

The operational amplifiers (Y1) and (X1) are Schmitt trigger connected. They receive respectively the sums of "$\overline{\text{Sens A}}$" and "Col A" via (R8) and (R6), and of "Sens A" and "Col A" via (R1) and (R2). At the output, they supply the respective logic signals "C + $\overline{\text{S}}$" and C + S". As these amplifiers have an open-collector output, + 5 V is applied to this output through resistors (R20) and (R19).

The purpose of diodes (CR8, CR9, CR10 and CR11), is to protect the following logic inputs by clamping, at 0 V and + 5 V, the changeover of the amplifiers to positive or negative saturation when the equipment is turned on.

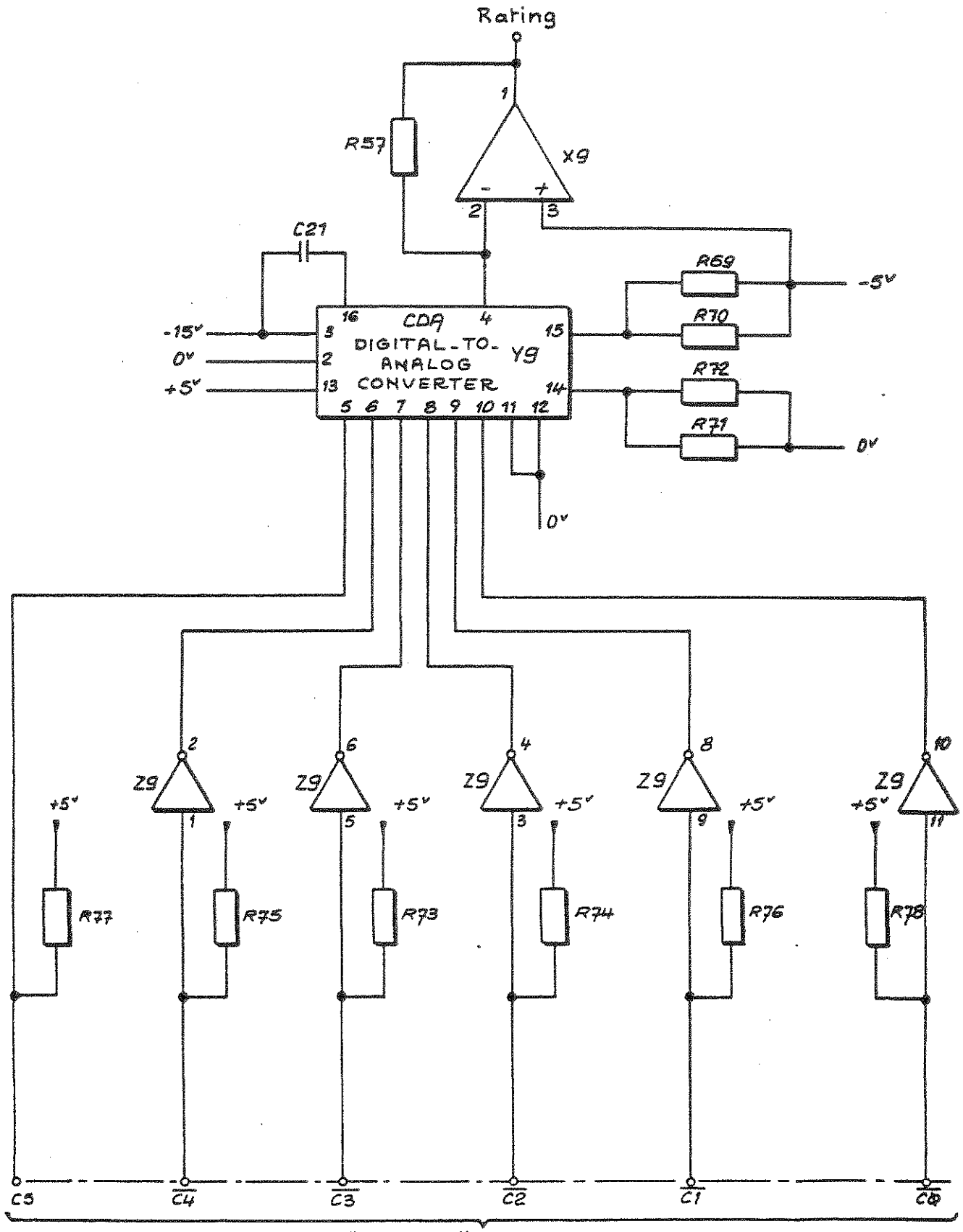
The inverters (X2-4) and (X2-2) respectively receive signals "C + $\overline{\text{S}}$" and "C + S" and supply signals "$\overline{\text{C + S}}$" and "$\overline{\text{C + S}}$".

NAND gate (X3-11) receives signals "C + S" and "C + S" and supplies synthesis signal "$\overline{\alpha}$" which controls electronic switch (Y3-16).

The control signals "$\overline{\beta}$", "$\overline{\delta}$" and "$\overline{\gamma}$" of the electronic switches (Y3-9), (Y3-1) and (Y3-8) are supplied respectively by NAND gates (X3-3), (X3-8) and (Y3-6) from and in order, signals "C + S" and "$\overline{\text{C + S}}$", "C + $\overline{\text{S}}$" and "$\overline{\text{C + S}}$", and "C + $\overline{\text{S}}$" and "C + S".

The electronic switches (Y3) thus allow sequential transmission of the upper part of the positive half sinewave of each of the "Sens' ", "Col' ", "$\overline{\text{Sens' }}$", "$\overline{\text{Col' }}$ " signals. These signals are obtained from respective signals "Sens A", "Col A", "$\overline{\text{Sens A}}$" and "$\overline{\text{Col A}}$" after passing through circuits (R23-C5), (R14-C4), (R4-C6) and (R21-C7). The signals are applied to the "contacts" of the switches in order to be summed together once the switches are closed ; the summing is applied to the negative input of the operational amplifier (Z1-14) which supplies an almost continuous inverted signal whose level is proportional to the true speed of the carriage.

NOTE : Operational amplifier (Z1-1) signifies : operational amplifier corresponding to output (1) of package (Z1).



"PIA IMP" board
("PIA IMP" input-output circuit(Z3))

Digital-to-analog converter

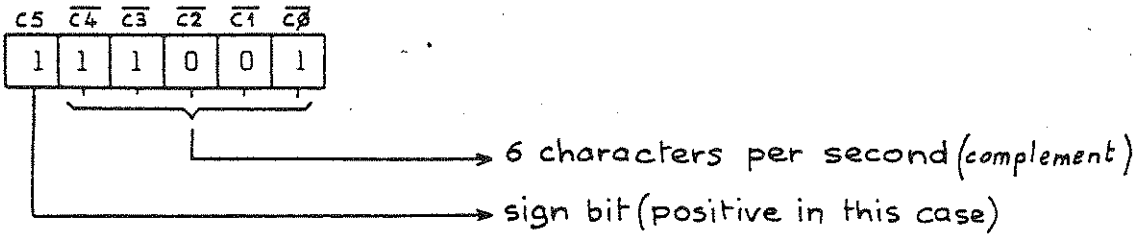
5.2.5 Digital-to-analog converter
("ASSERVISSEMENT" board)

The "PIA IMP" input-output circuit (Z3) on the "PIA IMP" board supplies 6 logic signals "$\overline{C\emptyset}$", "$\overline{C1}$", "$\overline{C2}$", "$\overline{C3}$", "$\overline{C4}$" and "C5" known as the "speed rating", which represent the maximum theoretical typing speed corresponding to telegraph operation speed.

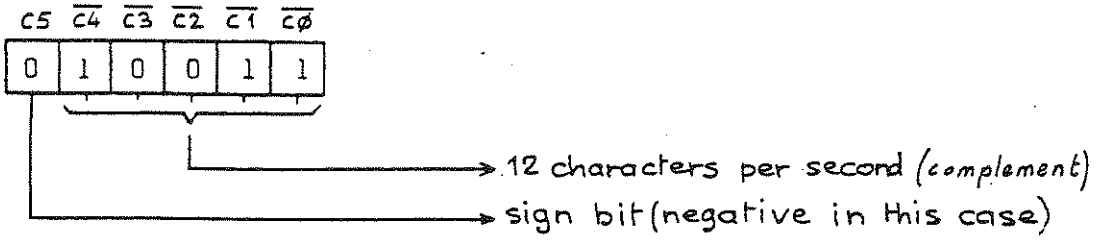
These signals subdivided into 5 movement speed bits "$\overline{C\emptyset}$" to "$\overline{C4}$" and one movement direction bit or sign "C5" which has the value "1" for positive movement from the left to the righ, and "0" for a negative movement from the right to the left. The advance speeds are coded in binary.

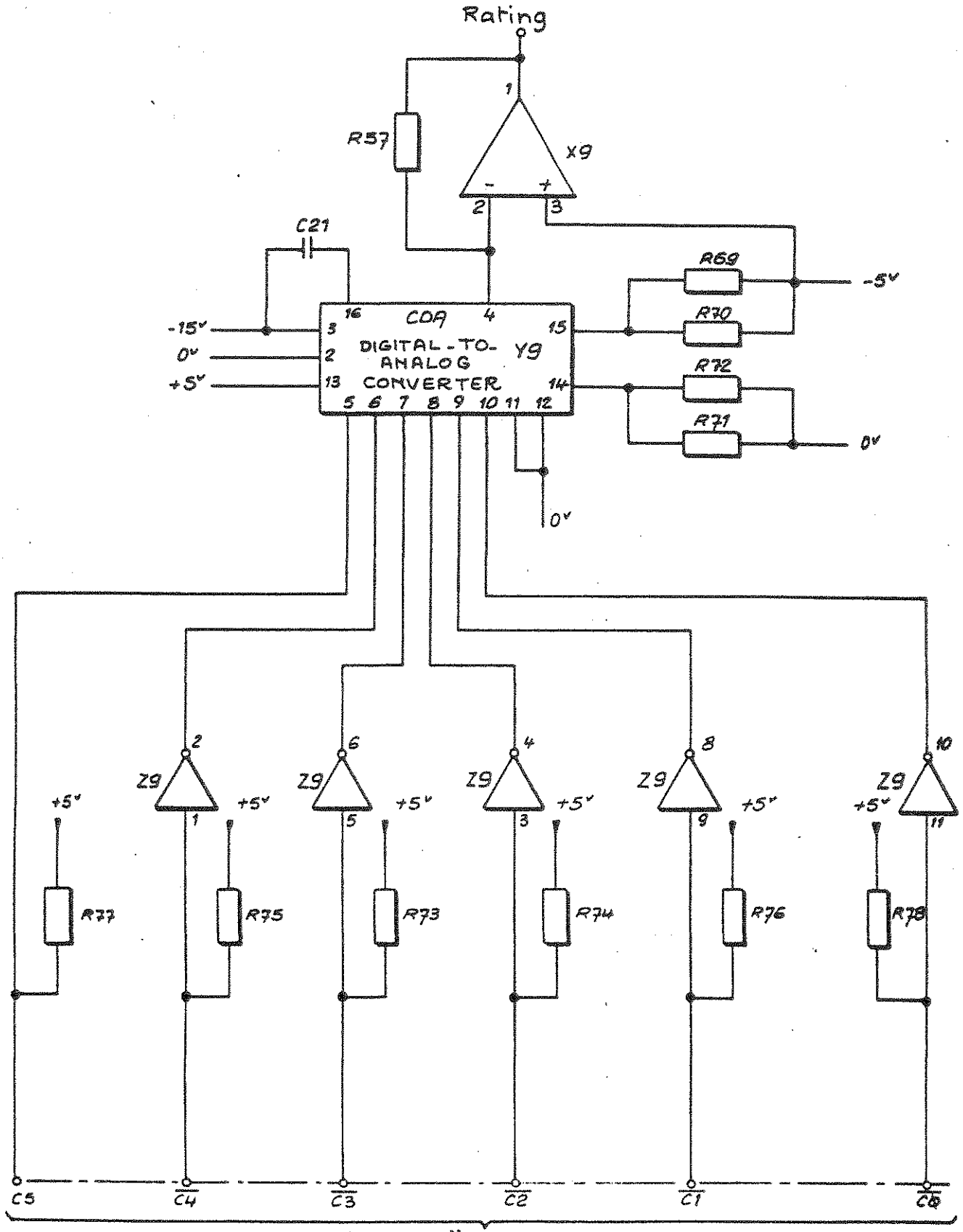
Example

For a maximum permitted speed of 6 characters per second, the rating is :



For a maximum permitted speed of 12 characters per second, the rating is :





"PIA IMP" board
("PIA IMP" input_output circuit (Z3))

Digital-to-analog converter

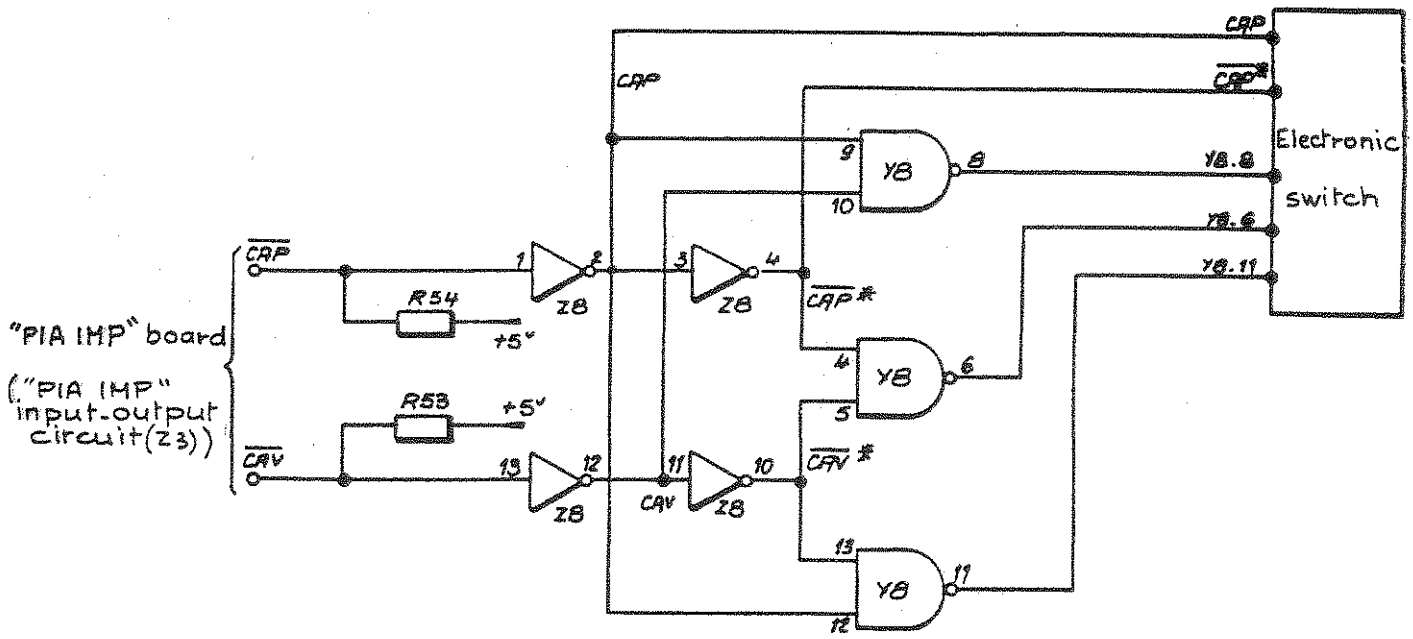
The rating "111111" corresponds to the stoppage of the PRINTING DEVICE whereas rating "000000" is used to order maximum acceleration (saturation of the DRIVE MOTOR amplifier) during a carriage return.

The digital-to-analog converter circuit is designed to transform the digital speed rating signals into a synthesis analog signal in order to compare it to the true speed and position signals.

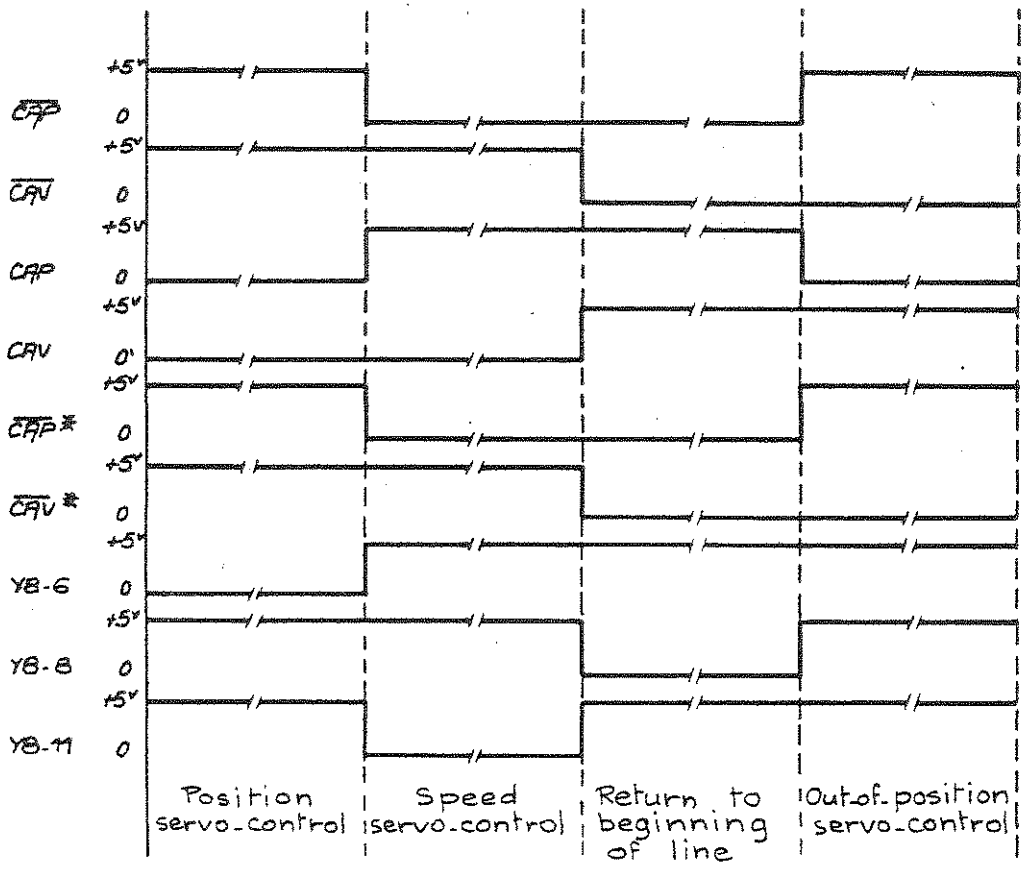
The signals "$\overline{C\emptyset}$" to "$\overline{C4}$" are complemented by inverters (Z9-10) (see NOTE), (Z9-8), (Z9-4), (Z9-6) and (Z9-2) and then applied to the digital inputs of the digital-to-analog converter "CDA" (Y9) which generates a DC current whose value depends on a binary code applied to its input. This current is converted into an "Rating" amplified voltage by operational amplifier (X9). It is used in the selection circuit.

The resistors (R77), (R75), (R73), (R74), (R76), and (R78) supply logic level "1" at the inputs of inverters (Z9) and digital-to-analog converter "CDA" (Y9) by a connection to the +5 V.

NOTE : Inverter (Z9–10) signifies : the inverter corresponding to output (10) of package (Z9).



Servo-controls



Timing diagram of servo-controls

5.2.6 Servo-controls

("ASSERVISSEMENT" and "PIA IMP" boards)

The Servo-controls are provided from an input-output circuit (Z3) located on the "PAI IMP" board by a wired logic circuit.

The input-output circuit (Z3) supplies logic speed and position Servo-control signals which, combined with their complements, order the opening or closing of the electronic switches in the selection circuit according to the Servo-control mode to be provided.

The various Servo-control modes are as follows :

- position Servo-control (start of line or character),
- speed Servo-control (carriage advance),
- return to beginning of line (carriage return),
- out-of-position Servo-control (positive or negative overshoot of more than 3 columns with respect to the position control).

Operating details of each configuration are given in the paragraph entitled "Selection and Summing Circuit".

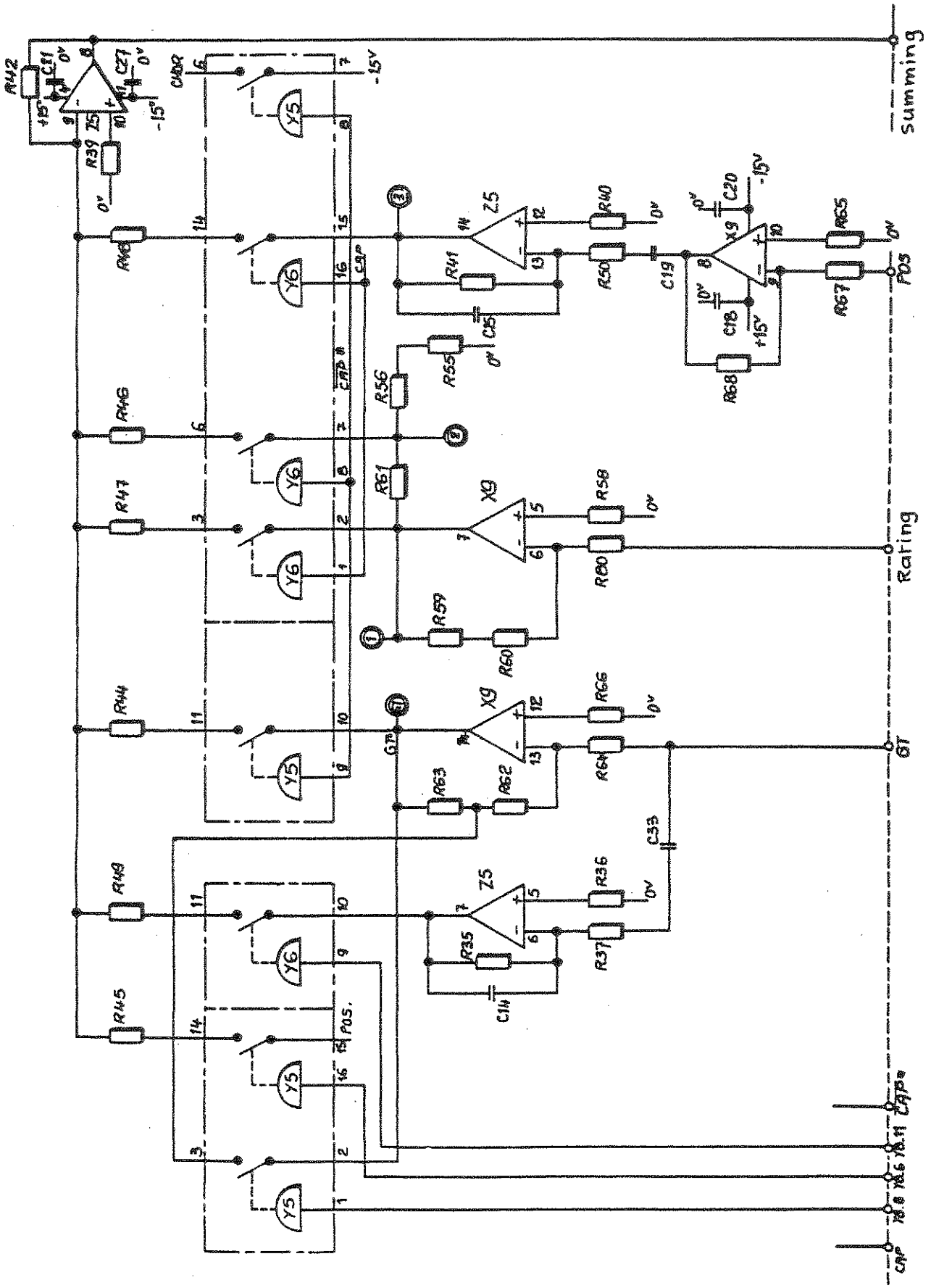
The "$\overline{CAP}$" position Servo-control and "$\overline{CAV}$" speed Servo-control signals, coming from the input-output circuit (Z3) are amplified and complemented by two inverters (Z8–2) (see NOTE) and (Z8–12) which supply respective signals "CAP" and "CAV".

The signals "CAP" and "CAV" are amplified and complemented by the two inverters (Z8–4) and (Z8–10) which provide signals "$\overline{CAP}^{*}$" and "$\overline{CAV}^{*}$".

The NAND gates (Y8–8), (Y8–6) and (Y8–11) produce respective control signals (Y8–8), (Y8–6) and (Y8–11) from the "CAP" and "CAV", "$\overline{CAP}^{*}$" and "$\overline{CAV}^{*}$", and "$\overline{CAV}^{*}$" and "CAP" data.

The resistors (R54) and (R53) supply the logic level "1" at the input of inverters (Z8-2) and (Z8-12) by connection to the + 5 V.

NOTE : Inverter (Z8–2) signifies : inverter corresponding to output (2) of package (Z8).



Selection and summing circuit

5.2.7 Selection and summing circuit

("ASSERVISSEMENT" board)

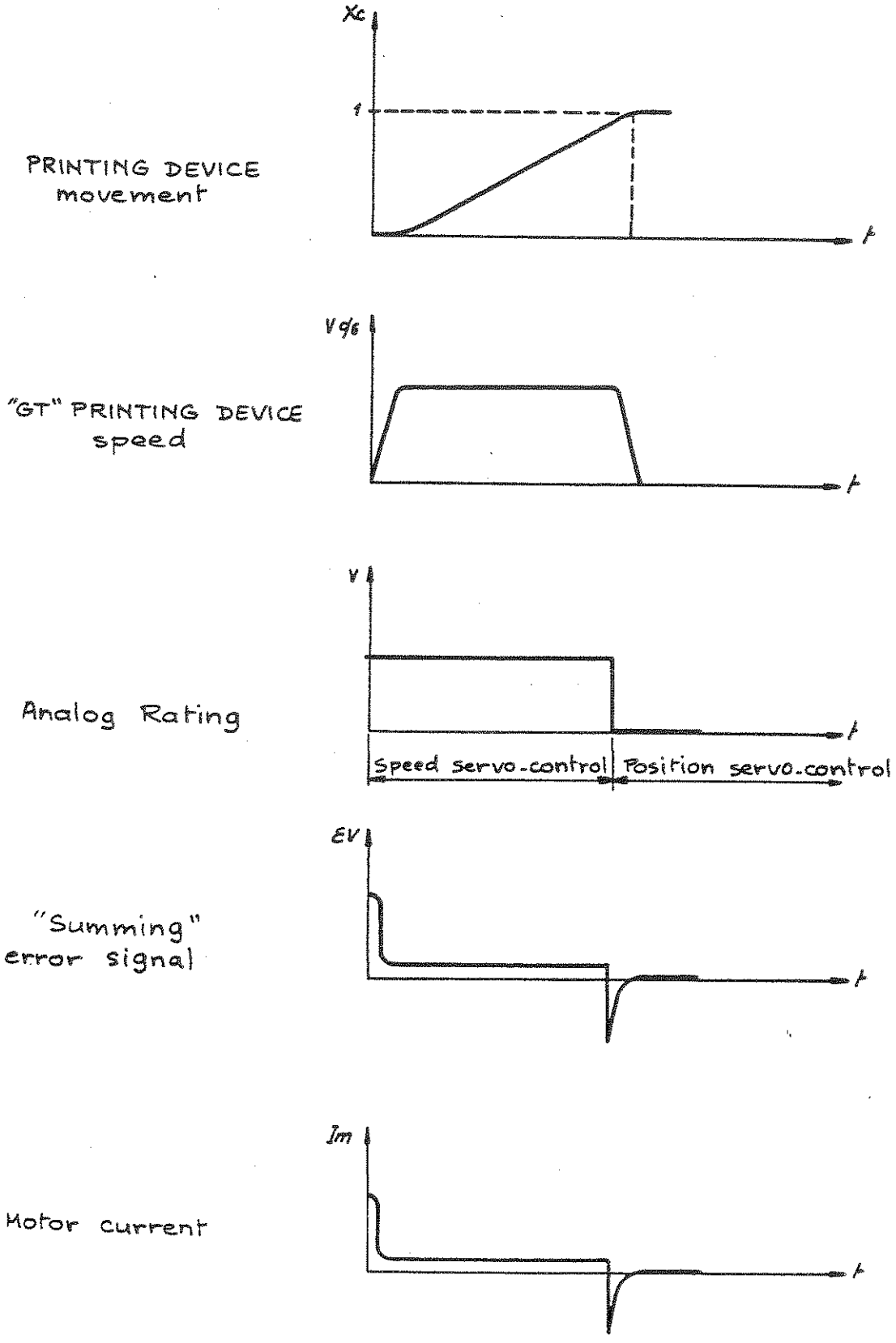
The purpose of the selection and summing circuit is to sum the signals corresponding to the maximum theoretical speed, the true speed and the position of the PRINTING DEVICE according to the operating mode governed by the Servo-control signals.

To do this, it receives the "Rating", Tachogenerator "GT" and Position "Pos" signals as well as the "CAP" position Servo-control signal, its amplified complement "$\overline{CAP}^*$" and its combinations "Y8–8", "Y8–6" and "Y8–11" with "$\overline{CAP}^*$", the "CAV" speed Servo-control signal and its amplified complement "$\overline{CAV}^*$".

The "Rating" signal from the Digital-to-Analog Converter (Y9) is applied to the operational amplifier (X9-7) through resistor (R80). The output of (X9-7) is applied directly to the electronic switch (Y6-2) (see NOTE) and, through resistor (R61), to electronic switch (Y6-7). The resistors (R56) and (R55) fix the output potential with respect to the power supply O V.

The "GT" signal from the Tachogenerator is applied to operational amplifier (X9-14) through resistor (R64) whose gain is controlled either by resistors (R64) and (R62-R63) when the electronic switch (Y5-2) is open, or by resistors (R64) and (R62) when the switch is closed. The "GT^*" amplified output signal is applied to the electronic switch (Y5-10). In parallel, the "GT" signal is derived and sent to operational amplifier (Z5-7) with its RC filter (R35-C14) whose ouput is applied to electronic switch (Y6-10).

NOTE : Electronic switch (Y6–2) signifies : the switch corresponding to input (2) of package (Y6).



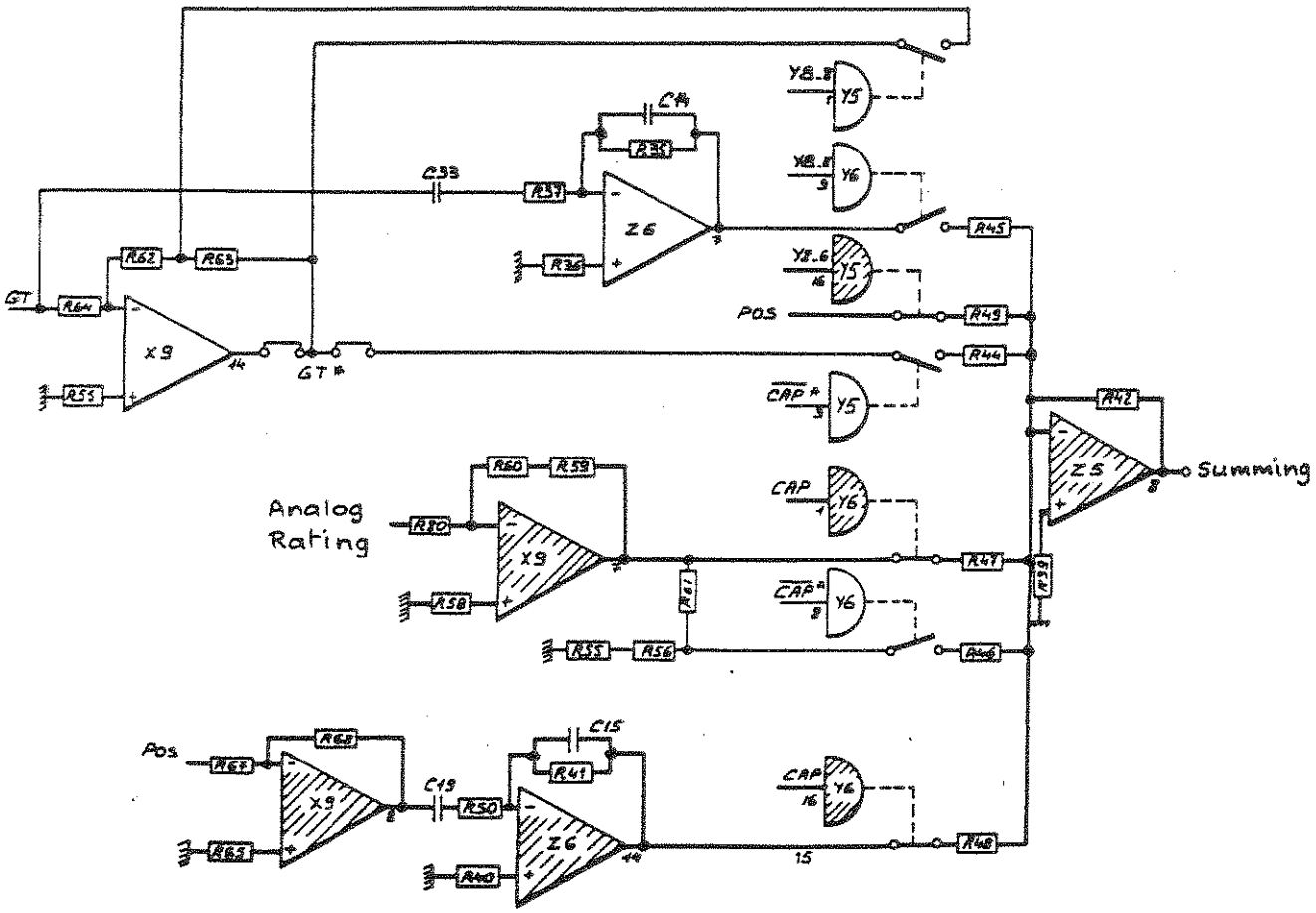
Timing-diagram of analog signals

The "Pos" signal from the SENSOR is applied to operational amplifier (X9-8) the output of which is applied through (C19) and (R50) to operational amplifier (Z5-14) mounted with an RC filter (R41-C15). The output signal from the amplifier appears on electronic switch (Y6-15). Furthermore, the "Pos" signal appears directly on electronic switch (Y5-15).

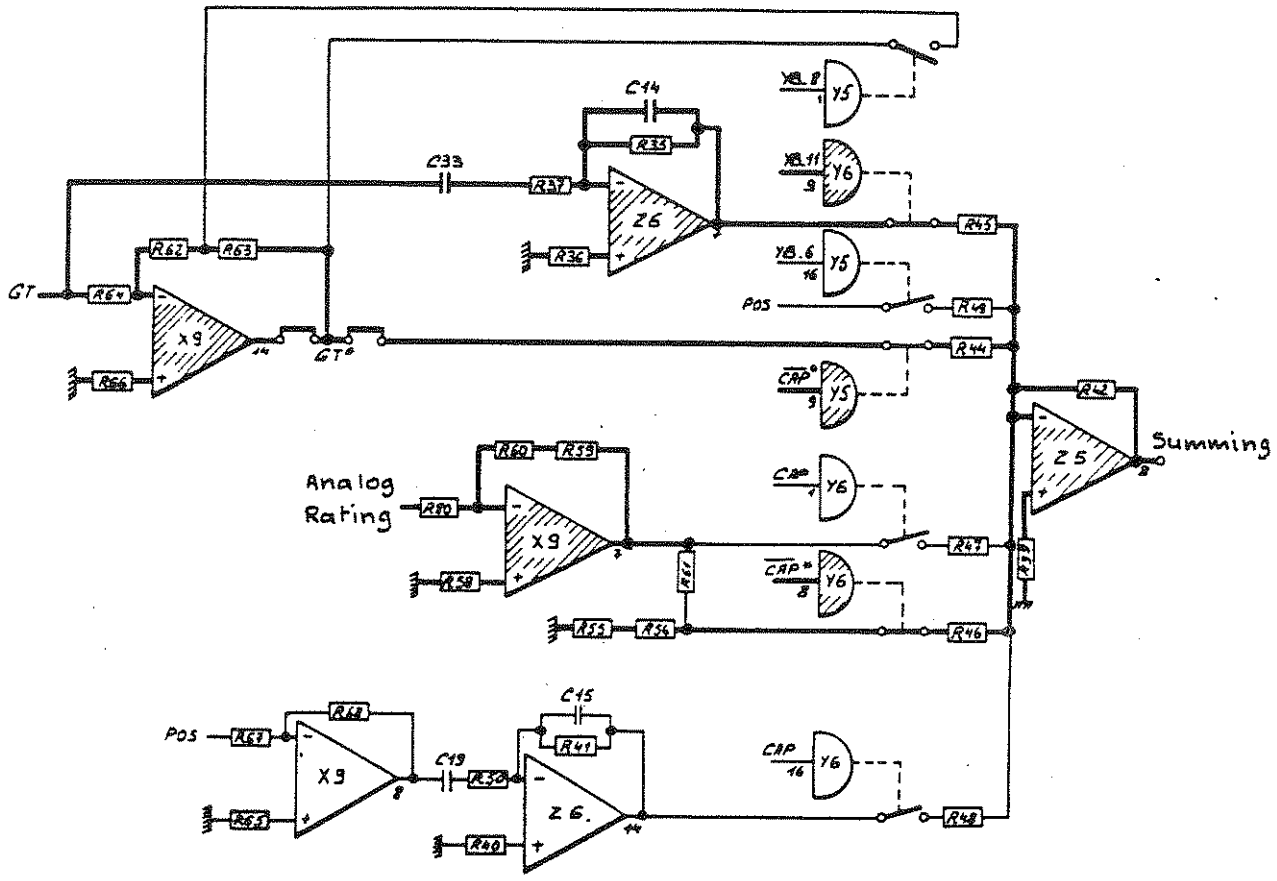
The Servo-control signals (see diagram in "Servo-controls" paragraph) close the switches by setting the gate input to zero. Depending on the operating mode required by the microprocessor, the Servo-control signals close certain contacts in order to sum the signals driving operational amplifier (Z5-8). The produced "Summing" signal controls the DRIVE MOTOR amplifier.

Summings are accomplished through resistors (R45), (R49), (R44), (R47), (R46) and (R48) according to four modes of operation :

- position Servo-control : The operational amplifier (X9–7) supplies a zero "Rating" voltage which is added to the "Pos" signal by controlling the closing of respective switches (Y6–1) and (Y5–16) by the "CAP" and "Y8–6" signals. The operational amplifier (Z5–8) supplies a "Summing" error voltage which controls the DRIVE MOTOR until the carriage stops if it is in motion, or holding the carriage stationary if it is already stopped. The closing of switch (Y6–15) by the "CAP" signal allows the derivative of the "Pos" signals to be added to the two other signals thus confirming the position Servo-control by phase advance correction. This Servo-control mode is retained within a range of ± 3 columns about the theoretical position of the character.



- speed Servo-control : the amplifier (X9–7) supplies a "Rating" voltage corresponding to the requested speed which is summed with the "GT*" signal coming from amplifier (X9–14), by closing respective switches (Y6–8) and (Y5–9) by the "$\overline{CAP}$*" signal. The "Summing" error voltage from amplifier (Z5–8) controls the DRIVE MOTOR. The closing of the switch (Y6–9) by signal "Y8–11" adds the derivative of the "GT" signal to the two other signals in order to stabilize the system by phase advance correction. The electronic switch (Y5–8) controlled by the "$\overline{CAP}$*" signal is not used.



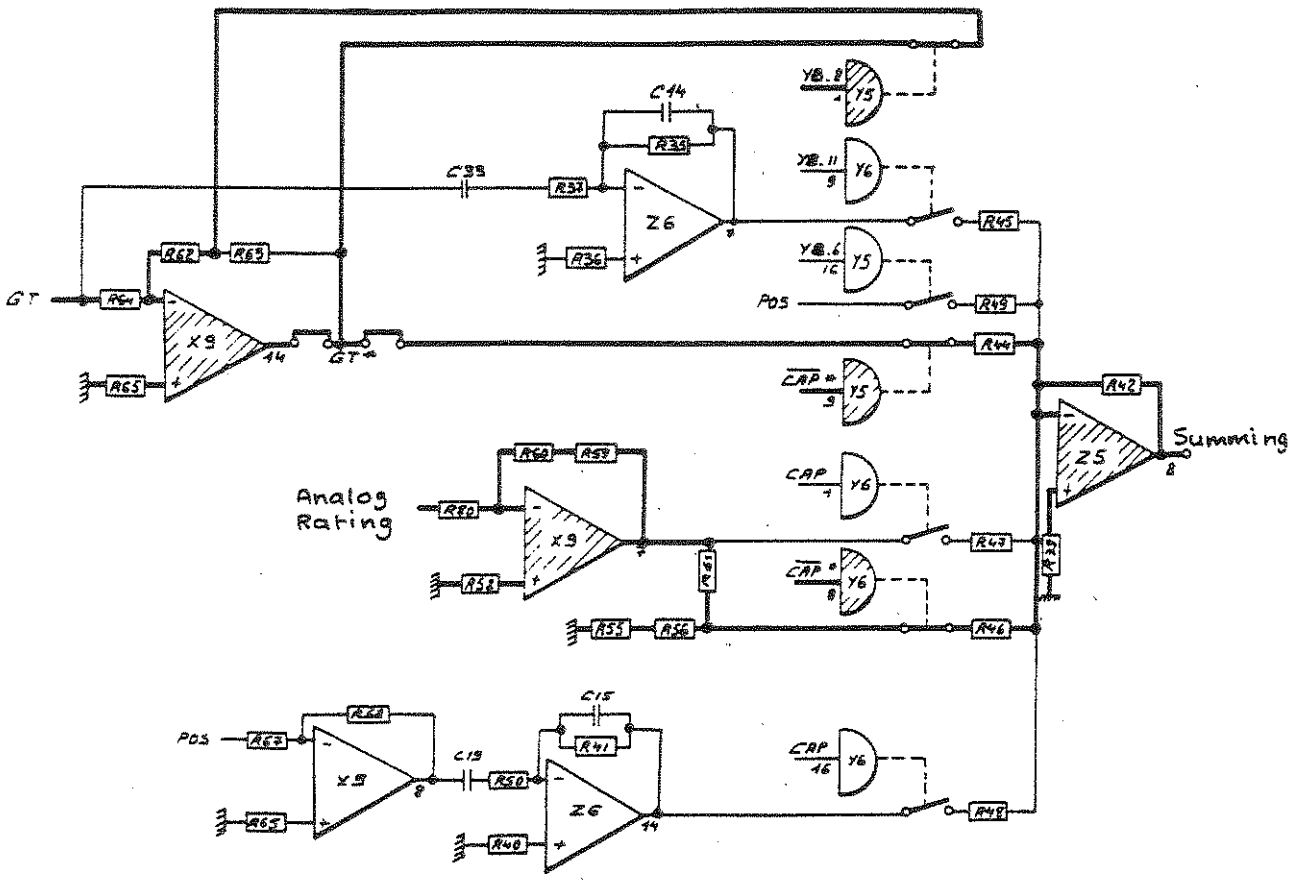
- Return to beginning of line (carriage return) : the operation consists in three separate phases :

  . acceleration of the carriage during which time the speed is maximum, up to detection of the 31st character,

  . deceleration of the carriage by a decreasing analog rating, after the last character whose columns are down-counted.

  . servo-control of the carriage position about the line start position resulting in Position Servo-control.

During the two first phases, the amplifier (X9-7) supplies a maximum, then decreasing, "Rating" voltage which is added to the "GT*" signal by closing the respective switches (Y6-8) and (Y5-9) through the "$\overline{CAP}$*" signal. In parallel, signal (Y8-8) closes switch (Y5-1) which short-circuits resistor (R63) to decrease the gain of the amplifier (X9-14) and make the "Rating" signal preponderant over the "GT*" signal whereby a greater speed is obtained for the same rating. Amplifier (Z5-8) supplies the "Summing" error voltage which controls the DRIVE MOTOR.

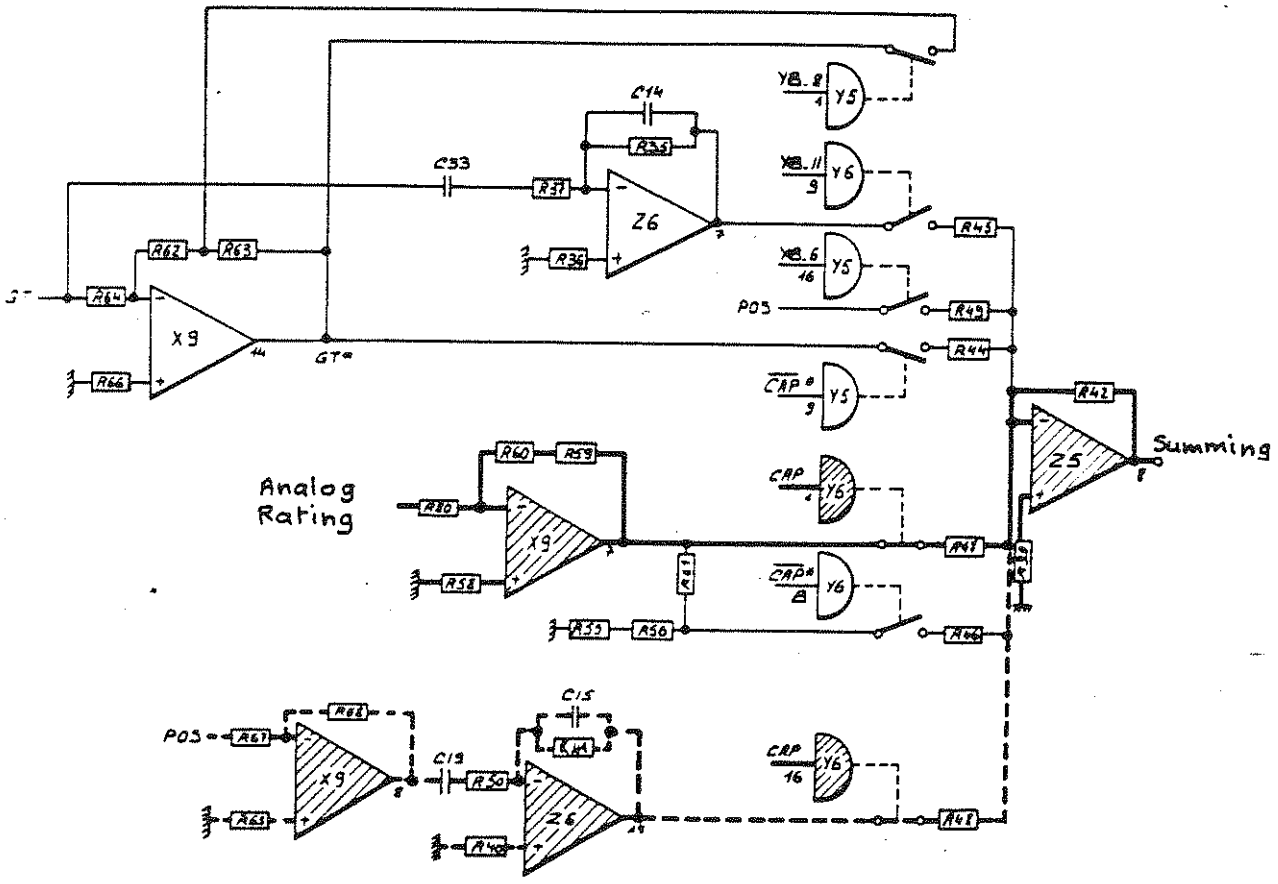


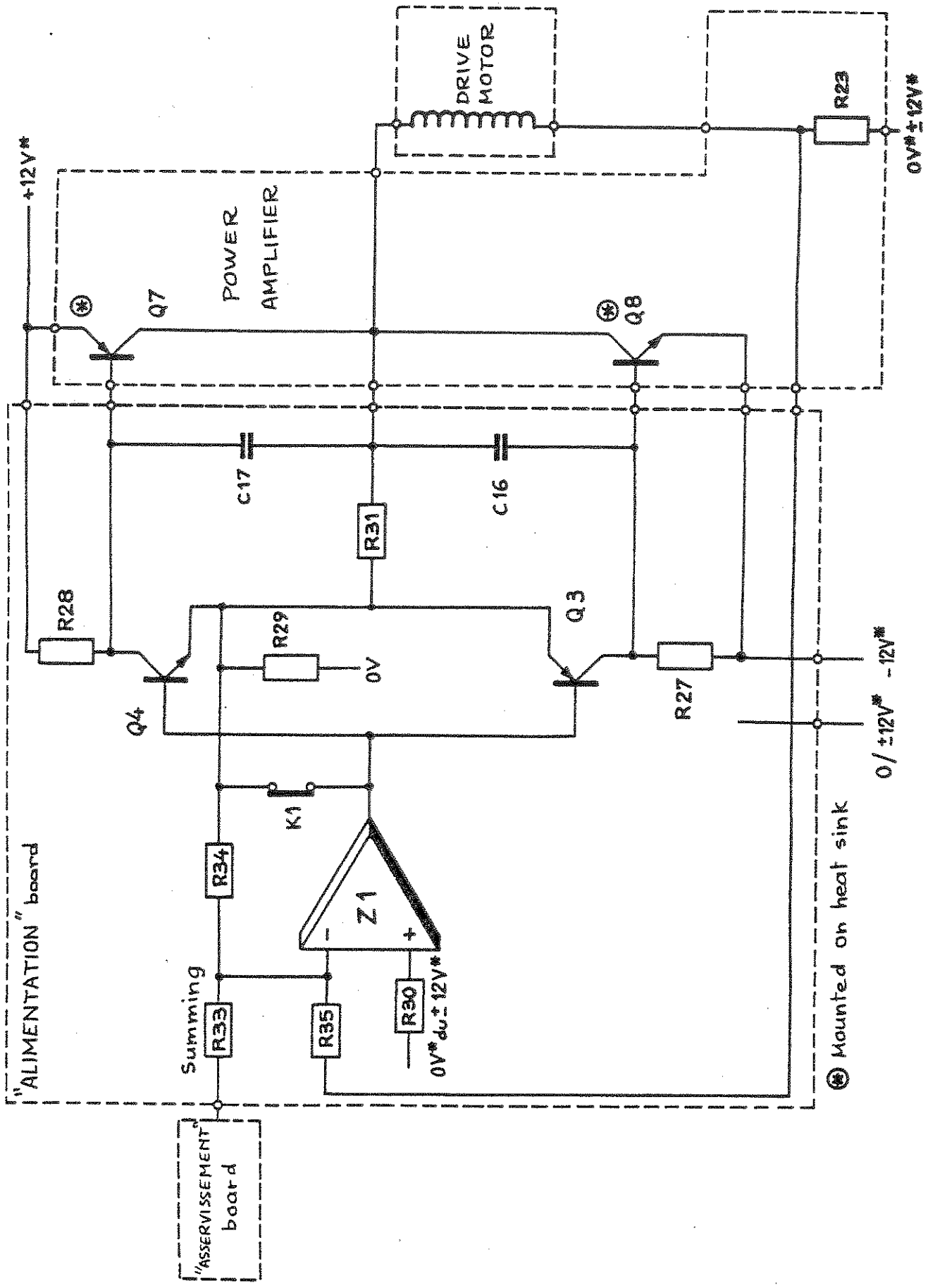
NOTE : When the carriage return is made from a position of less than 32 characters, the first stage is suppressed.

- out-of-position servo-control : this operating mode is a complementary safety feature for position servo-control. Beyond the tolerance of + 3 columns of position servo-control, the carriage undergoes an out-of-position digital servo-control limited to + 28 columns (one character). Beyond this value, the microprocessor orders a change to the speed servo-control mode, carriage return to the mechanical limit and then advance to search for the beginning of line.

Summing, performed in order to obtain the "Summing" error signal controlling the DRIVE MOTOR, is based on the summing obtained during position servo-control. At the + 3 column threshold, the switch (Y5-16) opens disconnecting the "Pos" signal. The analog "Rating" voltage increases in proportion to the number of shift columns, thus tends to bring the carriage back to its theoretical balance position.

The derivative signal of "Pos", still summed with the analog "Rating" voltage in the out-of-position servo-control mode, has no influence on summing since the movement of the carriage is relatively slow.





Drive motor amplifier

5.2.8 DRIVE MOTOR amplifier

("ALIMENTATION" board and POWER AMPLIFIER)

The DRIVE MOTOR amplifier on the "ALIMENTATION" board receives the "Summing" signal from the "ASSERVISSEMENT" board. The signal drives the operational amplifier (Z1) which, depending on whether the signal is positive or negative, controls the cascade of transistors (Q3–Q8) or (Q4–Q7) of the POWER AMPLIFIER located at the back of the unit.

Resistor (R23) generates a feedback voltage proportional to the current in the DRIVE MOTOR. The voltage is applied at the input of amplifier (Z1) via resistor (R35). The value ratios of resistors (R33–R34) and (R35–R34) determine the gain of amplifier (Z1) for each input signal, thus providing summing between the "Advance" order and its execution.

The power stage on the POWER AMPLIFIER is driven by two sources (+ 12 V*) (see NOTE) and (- 12 V*) of the ± 12 V* POWER SUPPLY.

The stages previous to these are located on the "ALIMENTATION" board.

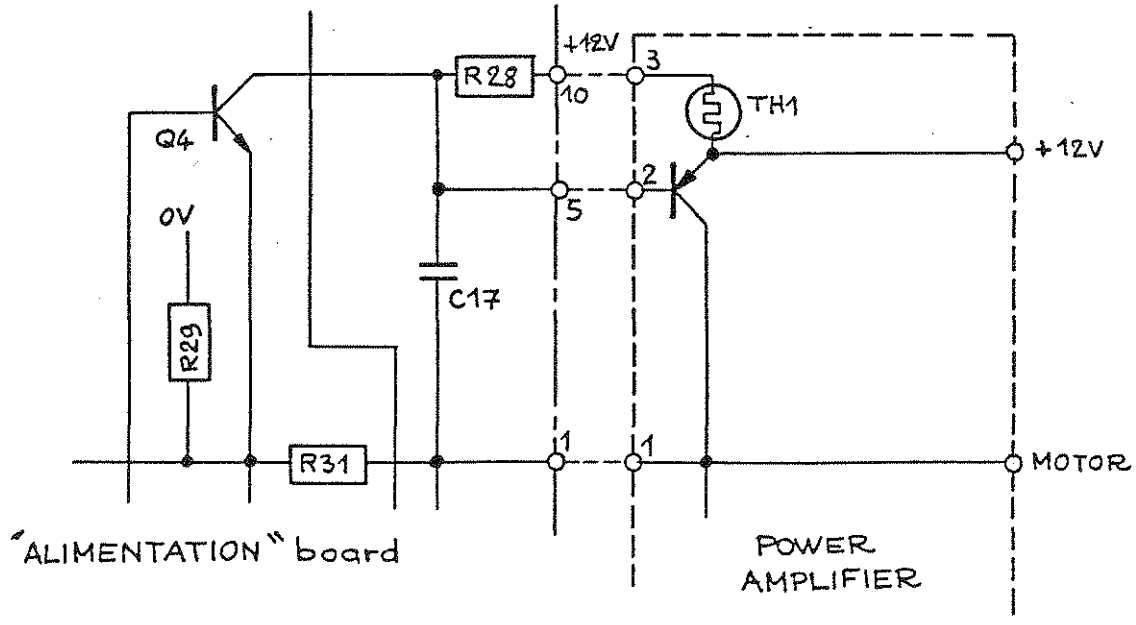
The gain of the output stage is determined by a pair of resistors (R29–R31) whereas the total gain of the amplifier is fixed by the resistors (R23–R33–R35).

The relay (K1) controlled by the initialization circuit blocks the DRIVE MOTOR amplifier during the initialization phase of the microprocessor and of the input-output circuits. The relay control mode is described in the "Initialization circuit" paragraph.

NOTE : The power supply sources assigned with the symbol * are "high current" sources.

Complementary data

A thermistor (TH1) ensures a protection from the short - circuits between 30 V* and 12 V*.



5.2.9 DRIVE MOTOR

The permanent magnet DRIVE MOTOR has the following characteristics :

- power supply voltage (u) : 12 V
- starting torque : 20 cm N
- torque per amp : 2.9 cm N/A
- electro-motive force : $3V/10^3$ r.p.m.
- maximum speed at nominal voltage : 3400 r.p.m.
- time constant at nominal voltage : 50 ms

5.3 LINE FEED

(LINE FEED MOTOR, PLATEN, PAPER ADVANCE, "PIA PERFO + AMPLI" and "PERSONNALISATION" boards)

The line feed device consists of a PLATEN controlled by a stepping motor through a reduction gear.

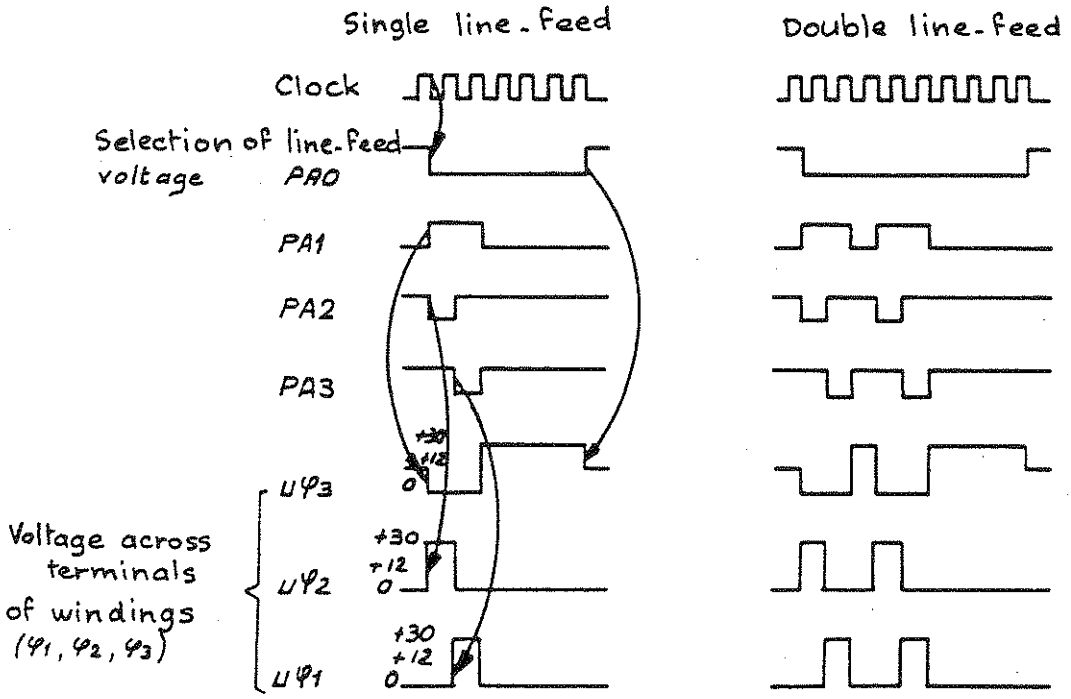
5.3.1. LINE FEED MOTOR

The stepping motor is a three-phase variable reluctance motor. During the line feed, the motor phases are supplied at 30 V. When the motor is stationary, to maintain sufficient torque, one phase remains energized at 12 V.

5.3.2 LINE FEED MOTOR input-output circuits

("PIA PERFO + AMPLI" and "PERSONNALISATION" boards)

The selection of single or double line feed is made on input (PA6) of input-output circuit (Z3) of the "PERSONNALISATION" board by means of switch (SW2).

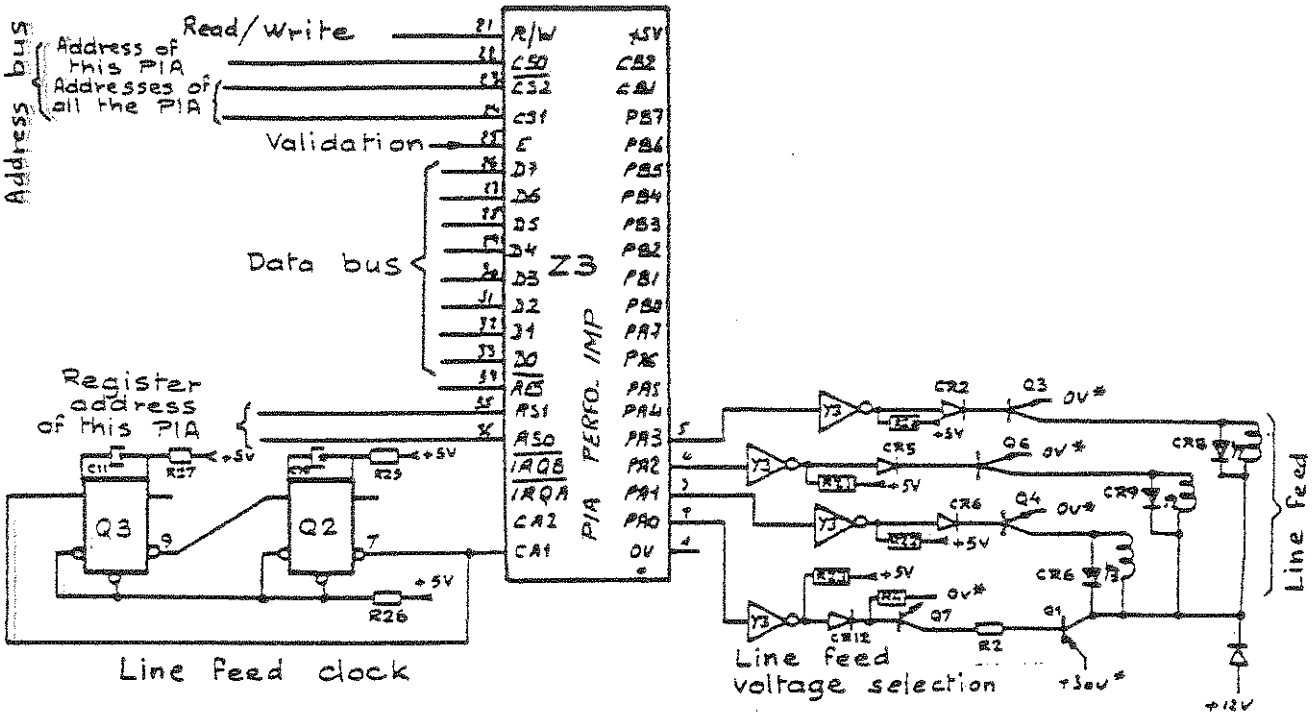


The three phases of the motor ($\varphi 1, \varphi 2, \varphi 3$) are controlled successively during one line feed clock period. After the line feed control, $\varphi 3$ still remains energized at 30 V for three clock periods in order to allow the LINE FEED MOTOR to become stabilized.

Clock period : t(Z4-9) + t(Z4-7) i.e. 560 s + 6.600ms = 7.16ms (typ.)

A circuit controlled by "line feed voltage selection", obtained from the output (PA0) of input-output circuit (Z3), allows + 30 V and + 12 V voltage switching.

In the event of a double line feed, following cycle $\varphi 1, \varphi 2$ and $\varphi 3$ of the first line feed, the three phases are controlled again during the same cycle. The stabilization time occurs after the second cycle.



Line feed input-output circuit

5.4 RIBBON DRIVE AND REVERSING SYSTEM

("PIA IMP", "PIA PERFO + AMPLI" boards, RIBBON ASSEMBLY (LEFT), RIBBON ASSEMBLY (RIGHT).

5.4.1 General

The ribbon advance and reversing system consists of :

- an input-output circuit generating the "Cde AV.RUB" (ribbon advance control) signal, located on the "PIA PERFO + AMPLI" board,
- an advance and reversing control circuit located on the "PIA IMP" board,
- a spool (N°1), mechanically connected to the shaft of a direct current motor (M1) and forming the RIBBON ASSEMBLY (LEFT),
- a spool (N°2), mechanically connected to the shaft of a direct current motor (M2) via an irreversible gear-wormscrew reduction arrangement, and an eyelet or ribbon tension detector, forming the RIBBON ASSEMBLY (RIGHT).

5.4.2 RIBBON ASSEMBLIES (LEFT AND RIGHT)

- Ribbon without eyelet

Motor (M1) is permanently connected to + 5 V*. Motor (M2) is energized during the time taken to return to beginning of line by the PRINTING DEVICE, with + 12 V* or with - 12 V* depending on the direction in which the ribbon is moving. The reversing control takes place as follows :

When spool n° 1 is empty and spool n° 2 full, the tension on the ribbon is increased because spool n° 2 tends to wind the ribbon in whereas its attachment to spool n° 2 prevents this from taking place.

This increase in tension causes the "Tension detector" lever controlling the reversal of direction to move.

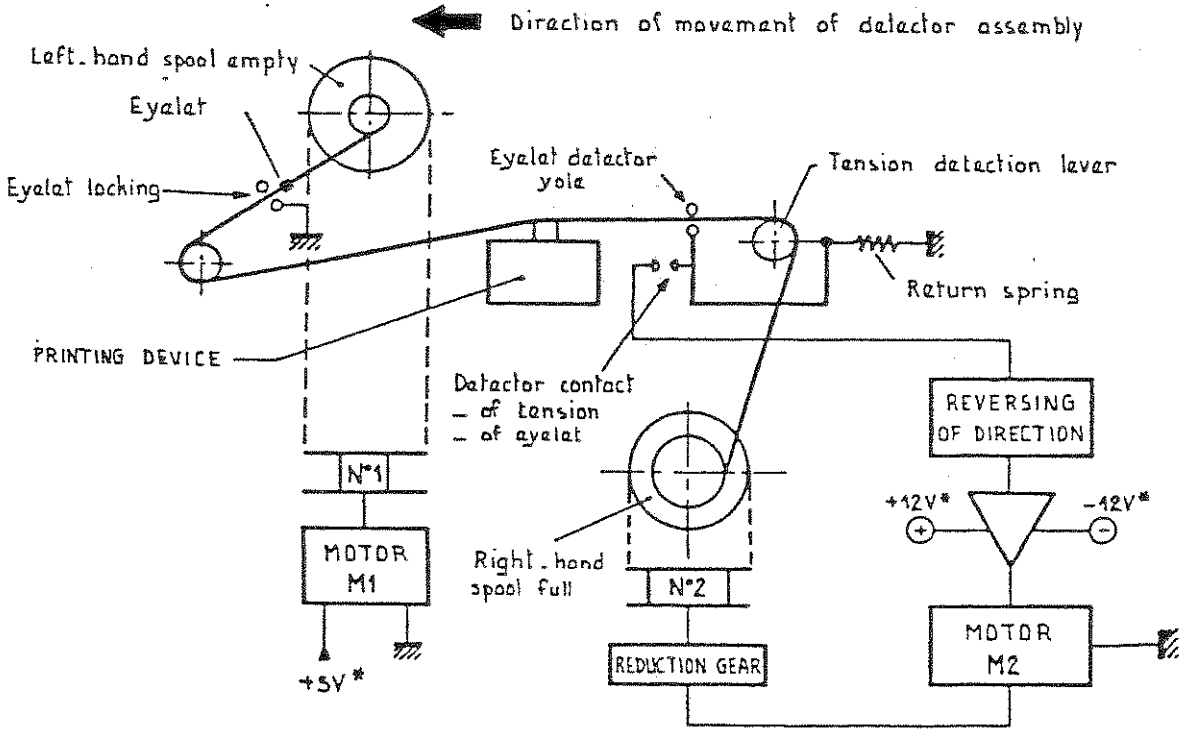
- Ribbon with eyelet

Here, operation is identical but the "tension detector" function of the lever is provided by the "Eyelet detector" lever when the eyelet locks into it.

5.4.3 System input-output circuit

On each carriage return, the input-output circuit ("PIA PERFO-IMP", (Z3) supplies the "Cde AV.RUB" (ribbon advance control) signal via output (CA2). The real time clock (see paragraph : MANAGEMENT OF TRANSMISSION PATH SUPERVISION DATA is also used as a time reference in order to obtain a 400 ms duration "Cde AV.RUB" signal.

NOTE : The power supply sources assigned with the symbol * are "high current" sources.



RIBBON DRIVE AND REVERSING SYSTEM

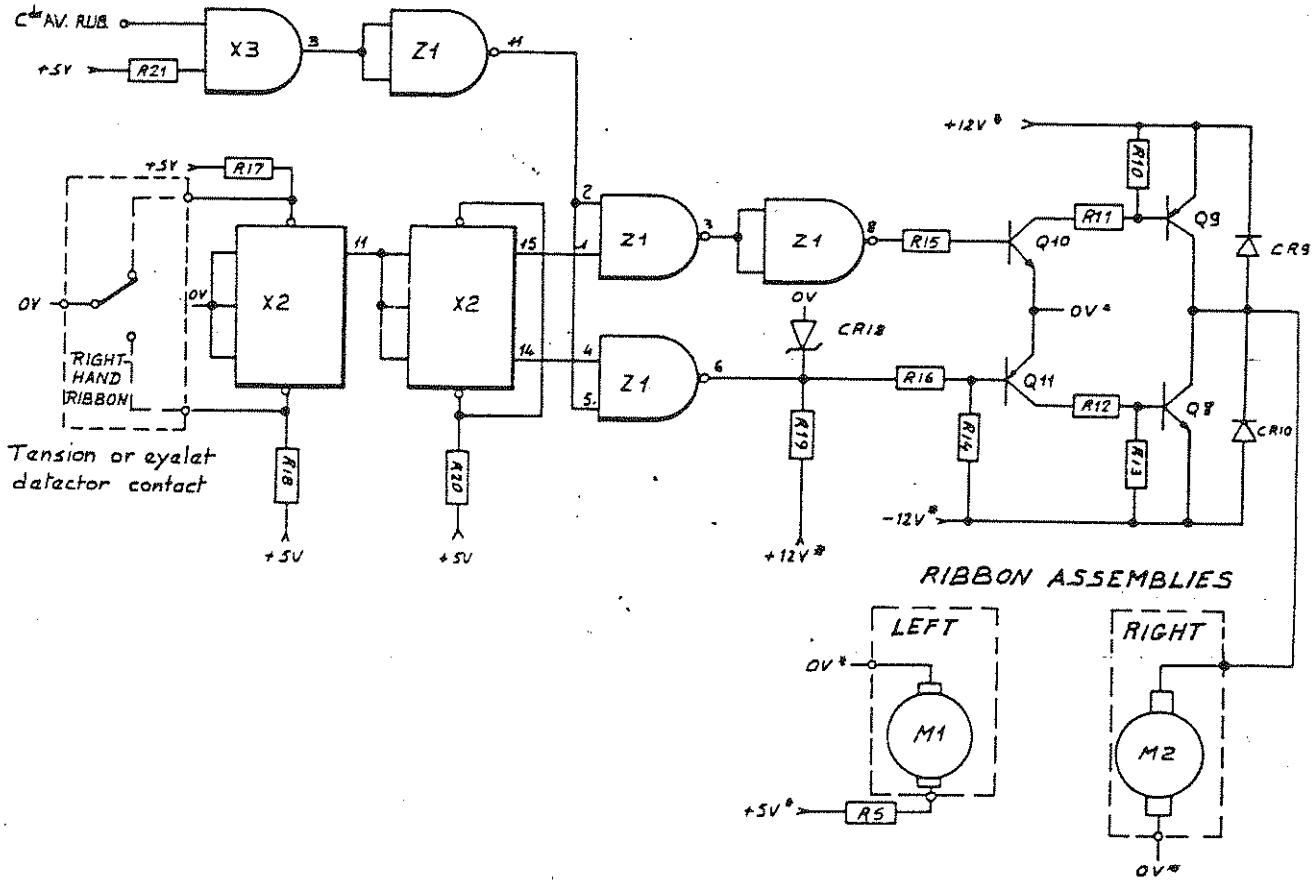
5.4.4 Advance and reversing controls (plate 5-1)

The "Cde AV.RUB" (ribbon advance control) signal is applied to one input of AND gate (X3-3) the other input of which is held at level "1" through resistor (R21). The output is inverted by NAND gate (Z1-11) which drives NAND gates (Z1-3) and (Z1-6).

Flip-flop (X2-11) eliminates any bounce which occurs on the closing of the eyelet or tension detector contact. The storage of the state of reversal is ensured by flip-flop (X2-14 and 15).

When output (15) of flip-flop (X2) is set to logic level "1" and when there is a ribbon advance control present, the transistor (Q10) becomes saturated thus causing the saturation of transistor (Q9) through the resistor bridge (R10 and R11) ; motor (M2) then turns clockwise. When output (15) of flip-flop (X2) is at logic level "0", a logic "1" is applied to input "4" of the NAND logic gate (Z1) ; operation is identical to that described above ; the saturation of transistor (Q8) makes motor (M2) turn counter-clokwise. When there is no ribbon advance control, transistors (Q8 and Q9) are blocked while motor (M2) is off.

The bridge consisting of resistor (R19) and diode (CR18) prevents (Q11) from being saturated when the mains voltage is cut off.



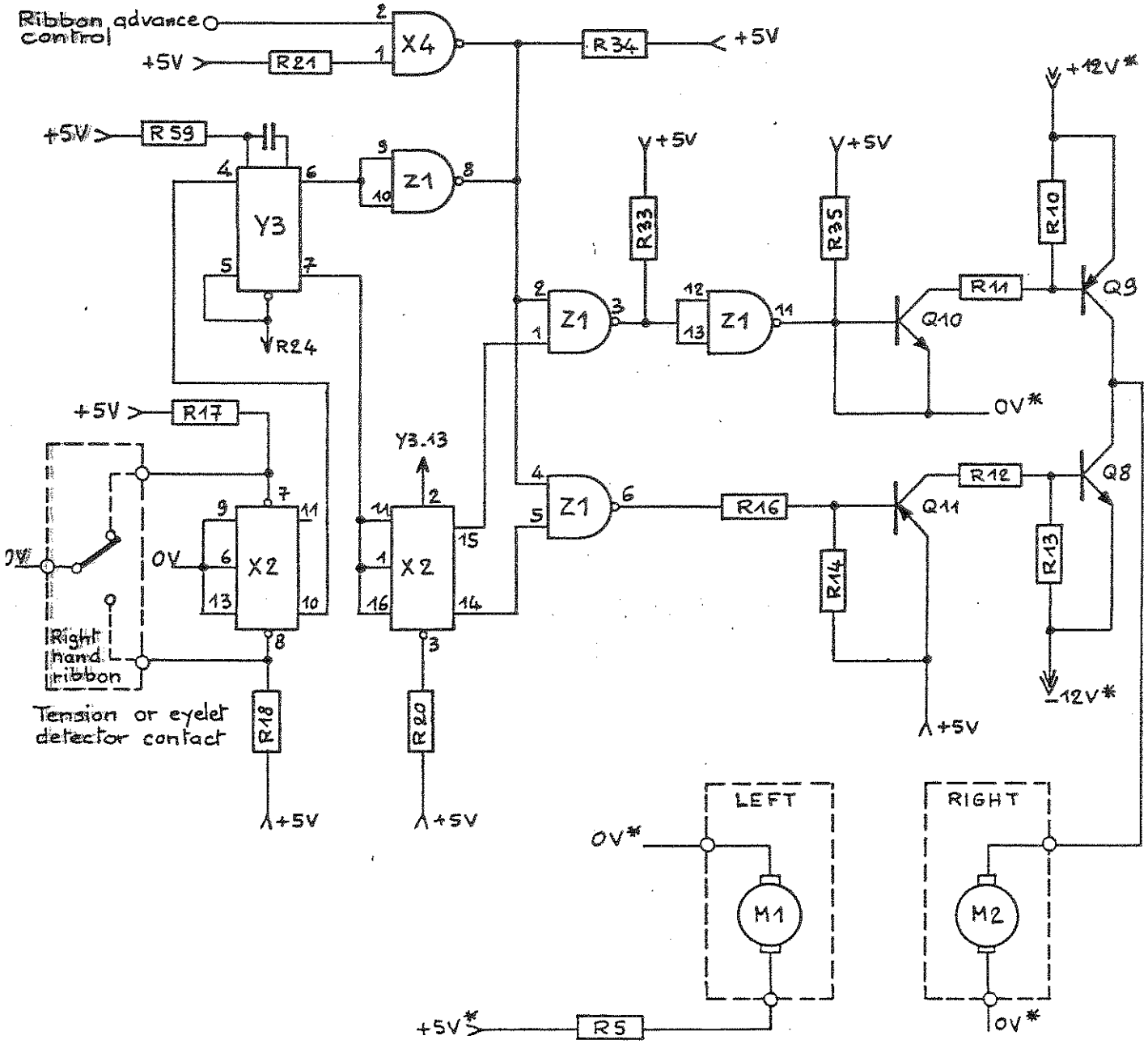
Advance and reversing controls

5.4.5 Complementary data

Ribbon advance controls (Plate 5-2)

The «Cde AV.RUB» (ribbon advance control) signal is applied to one input of NAND gate (X4-2) the other input of which is held at level «1» through resistor (R21). The control pulse proceeding from (X4-3) drives inputs «2» and «4» of (Z1).

Flip-flop (X2-10) eliminates any bounce which occurs on the closing of the eyelet or tension detector contact. The storage of the state of reversal is ensured by flip-flop (X2-14 and 15) and is applied to inputs «1» and «5» of (Z1). The monostable (Y3-7) controls flip-flop (X2). Every time that the ribbon reversing control is activated, monostable (Y3-6) inhibits the control pulse proceeding from (X4-3). This arrangement forbids every possibility of simultaneous conduction of power transistors (Q8) and (Q9), supplied with opposite voltages. These circuits are protected by thermistors (TH1) on + 12 V input, and (TH2) on - 12 V input.



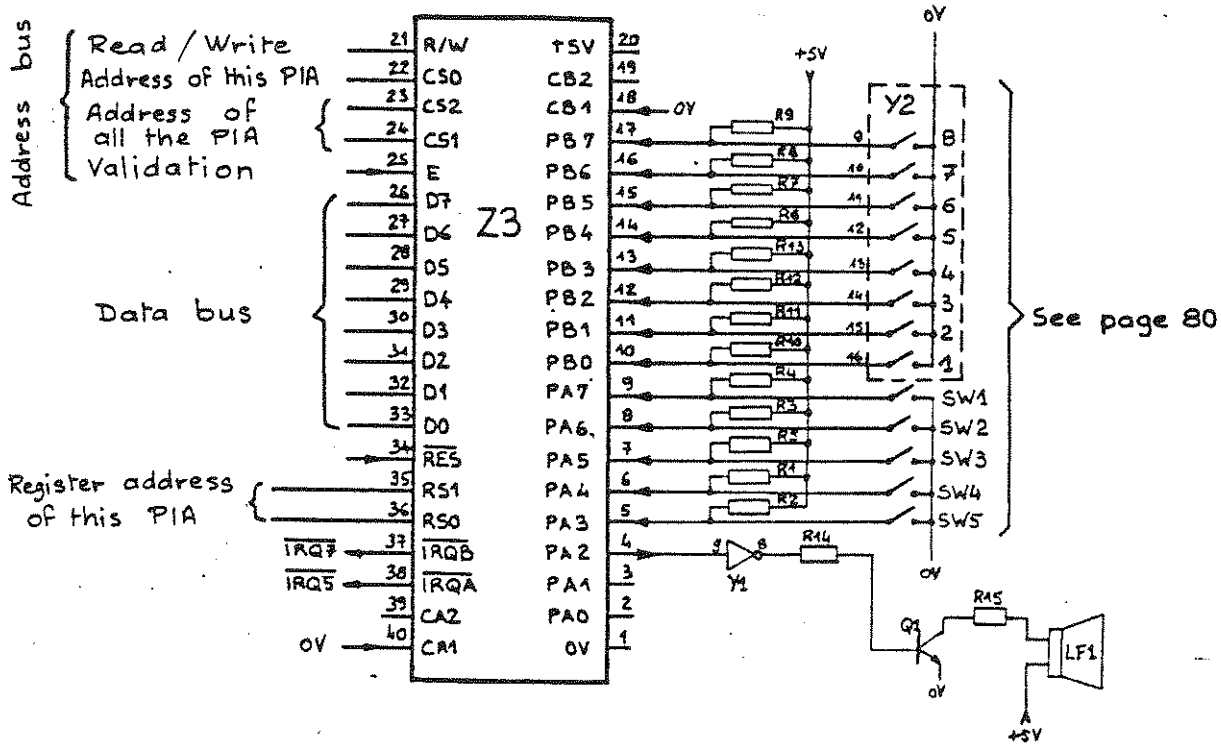
ADVANCE AND REVERSING CONTROLS

6 – PERSONALIZATION
(«PERSONNALISATION» board)

This board is equipped with all the controls allowing the equipment operation selection.

These controls are provided by switches (SW1 to SW5), accessible to the operator, and by D.I.L. switch (Y2) which is accessible to the maintenance technician. The switches set a logic "1" or logic "0" on inputs (PA3 to PA7 and PB0 to PB7) of the input-output circuit (Z3). The setting to "1" of the inputs (PA3 to PA7 and PB0 to PB7) is accomplished by aplying a power supply + 5 V via the resistors (R1 to R13).

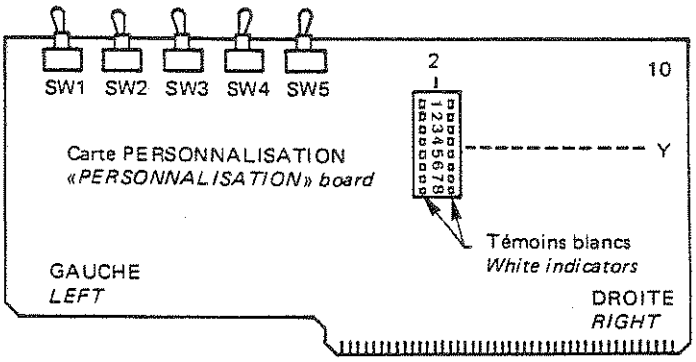
The audible alarm (FL1) is controlled through resistor (R15) by the saturation of transistor (Q1) caused by the application of a logic "0" to the input of inverter (Y1).



SWITCH SETTINGS OF THE "PERSONNALISATION" BOARD

INTERRUPTEURS ACCESSIBLES A L'OPERATEUR *SWITCHES WITHIN THE REACH OF THE OPERATOR*			
INTERRUPTEUR *SWITCH*	FONCTION *FUNCTION*	LEVIER A GAUCHE *TOGGLE TO LEFT*	LEVIER A DROITE *TOGGLE TO RIGHT*
SW 1	Etat du PERFORATEUR lors de la réception d'un appel *State of TAPE PUNCH when receipt of an incoming call*	Mis en marche *ON*	Mis à l'arrêt *OFF*
SW 2	Interligne *Line feed*	Simple *Single*	Double *Double*
SW 3	Dégagement du texte *Text visibility*	Après 250 ms *After 250 ms*	Après 750 ms *After 750 ms*
SW 4			
SW 5	Nombre d'interlignes en fin de communication *Line feed number at the end of communication*	8	4

INTERRUPTEURS ACCESSIBLES A L'INSTALLATEUR OU A L'AGENT DE MAINTENANCE *SWITCHES WITHIN THE REACH OF THE FITTER OR MAINTENANCE PERSONNEL*			
INTERRUPTEURS *SWITCHES* *Y2*	FONCTION *FUNCTION*	TEMOIN BLANC APPARENT A GAUCHE *WHITE INDICATOR VISIBLE ON THE LEFT*	TEMOIN BLANC APPARENT A DROITE *WHITE INDICATOR VISIBLE ON THE RIGHT*
1	Communication *Communication*	SIMPLEX *Simplex*	DUPLEX *Duplex*
2	Possibilité d'exploitation qu'après échange d'indicatif à l'établissement de la communication *Operating possibility only after exchange of answer-back codes when the communication in through*	Inoperant *Inoperative*	Operant *Operative*
3	Alarm sonore (défaut) *Sound alarm (fault)*	Permanente *Permanent*	Fugitive *Momentary*
4	Déclenchement de l'émetteur d'indicatif par la séquence de signaux «CHIFFRES» «D» *Trigger of the answer-back unit by the sequence of «FIGURES» «D» signals*	Impossible *Impossible*	Possible *Possible*
5			
6	Perforation de «CHIFFRES» «D» *Punching of «FIGURES» «D»*	Sans *Without*	Avec *With*
7			
8	Transmission *Transmission*	Simple courant passif *Single current passive*	Double courant ou simple courant actif *Double current or single current active*



NOTA : Le changement de position des interrupteurs (Y2) s'effectue par appui sur les témoins blancs.

NOTE : Position change of switches (Y2) is carried out by depressing white indicators.

7 – TAPE PUNCHING
(TAPE PUNCH, «PIA PERFO + AMPLI» board)

7.1 GENERAL

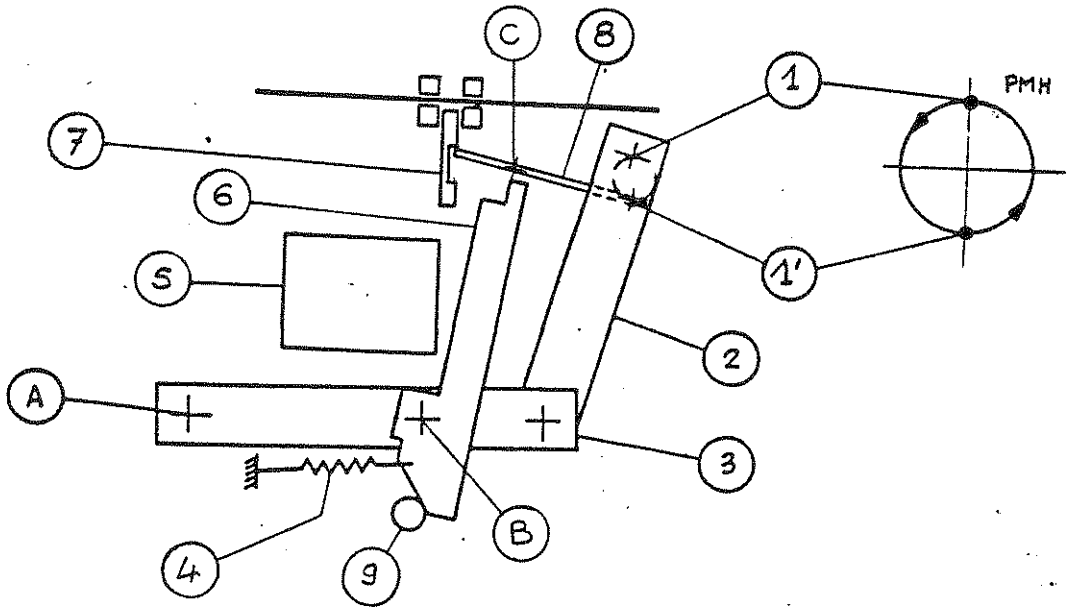
The TAPE PUNCH is equipped with a ferro-magnetic sensor mounted on an excentric, defining the feed and punch sequence from a mechanical origin (upper neutral point "PMH").

Back spacing of the punched tape is obtained by means of a pawl integral with the BACK-SPACER key. The pawl meshes directly with the ratchet wheel of the feed control in order to make one back spacing step.

7.2 PUNCHING DEVICE

One revolution of the eccentrics represents on punch step. The position of the mechanical parts is represented according to the position of the eccentrics. Rod (2) is coupled to eccentric (1) and to rod (3), the pivoting point (A) of which is fixed.

The armature (6) of electromagnet (5) pivots on shaft (B) of rod (3) and bears against stop (9) under the effect of spring (4).



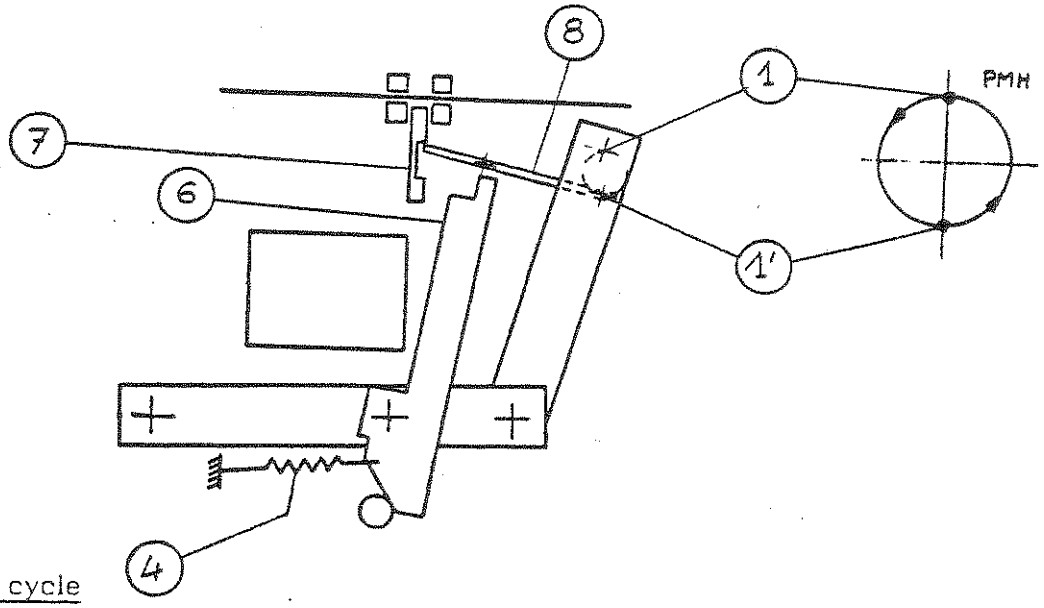
Return lever (8) of punch (7) pivots on shaft (C) ; it is actuated by eccentric (1'), diametrically opposed to eccentric (1).

7.2.1 Cycles with punching

Start of 1st cycle

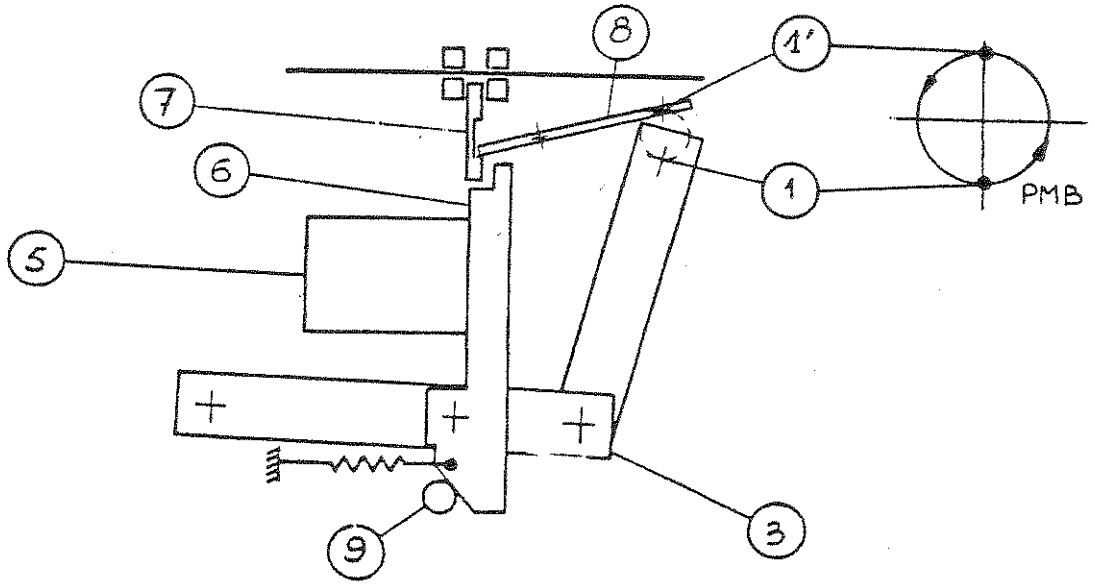
The mechanical parts are in the following configuration :

- eccentric (1) is in the high position,
- eccentric (1') is in the low position,
- lever (8) is in the high position in the groove of punch (7),
- armature (6) clears the end of punch (7) under the effect of spring (4).



Middle of 1st cycle

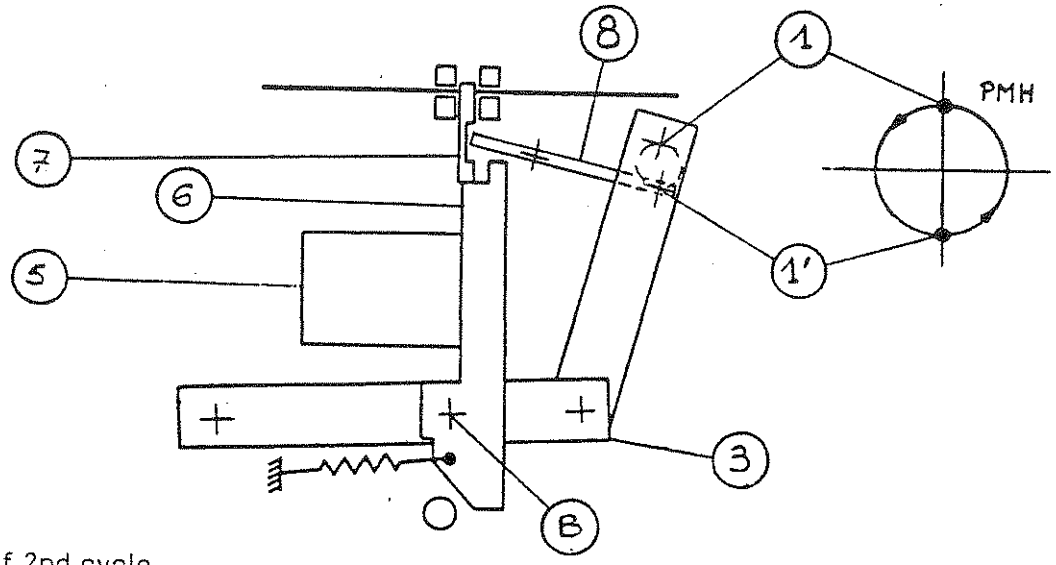
- eccentric (1) is in the low position while eccentric (1') is in the high position,
- lever (8) bears against the bottom part of the groove of punch (7),
- armature (6) bears against electromagnet (5) under the effect of rod (3) and stop (9).



The electromagnet (5) is energized at the moment of control generated by the electronic logic associated with the TAPE PUNCH ("PIA PERFO + AMPLI" board).

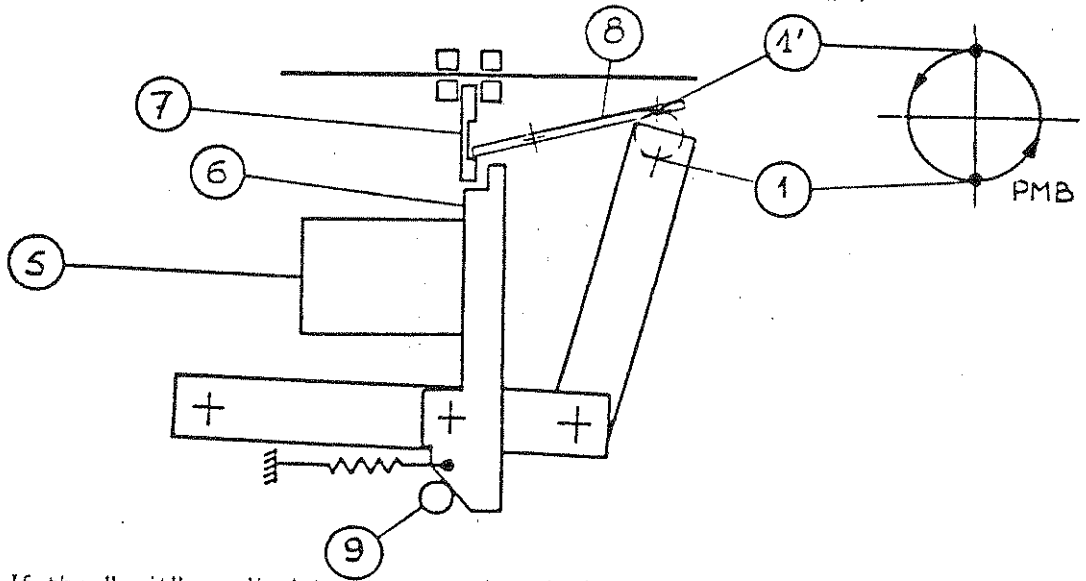
End of 1st cycle and stard of 2nd cycle

- eccentric (1) is in the high position,
- eccentric (1') is in the low position,
- being retained by electromagnet (5), armature (6) drives punch (7) to move upwards as it is fastened at (B) to rod (3)
- lever (8) is lifted into the groove of punch (7) under the effect of eccentric (1') in order to allow the punch to rise.



Middle of 2nd cycle

- eccentric (1) is in the low position
- eccentric (1') is in the high position,
- armature (6), still retained by electromagnet (5), returns to bear against stop (9),
- lever (8) pulls punch (7) downwards under the effect of eccentric (1').



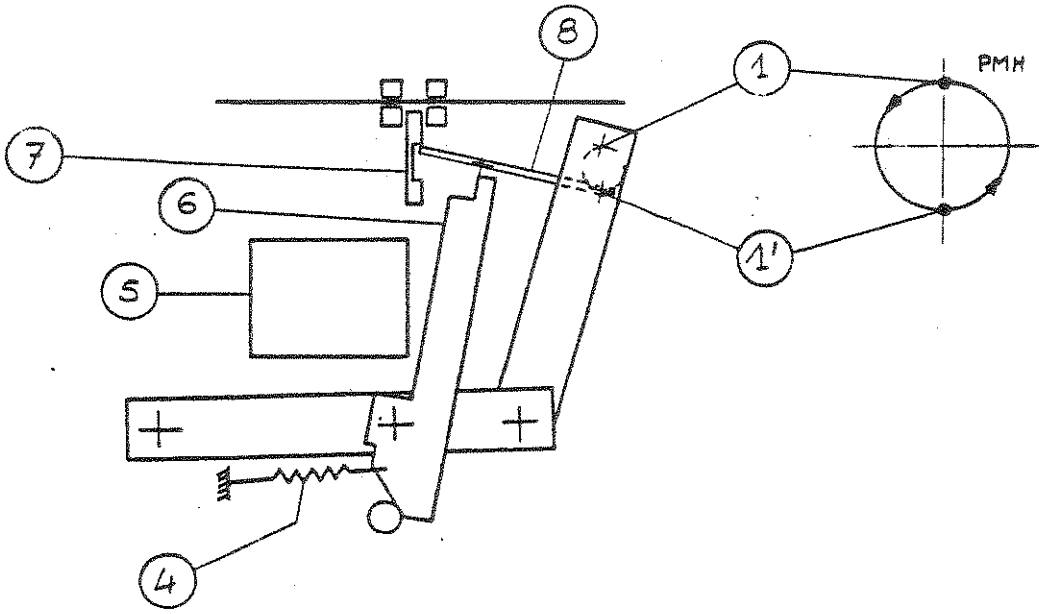
If the "unit" applied to the associated electronic logic requires further punching operations, the electromagnet will remain energized up to the middle of the 3rd cycle ; otherwise, the electronic logic cuts off the power supply and operation is resumed at the beginning of the 1st cycle.

7.2.2 Cycles without punching

Start of 1st cycle

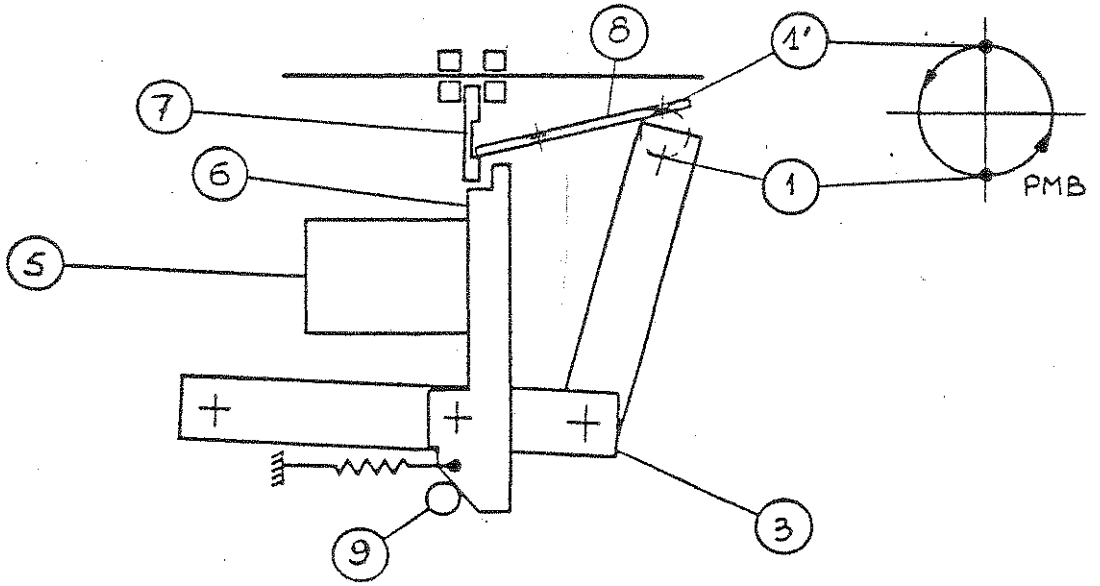
The mechanical parts are in the following configuration :

- eccentric (1) is in the high position,
- eccentric (1') is in the low position,
- lever (8) is in the high position in the groove of punch (7),
- armature (6) clears the bottom of punch (7) under the effect of spring (4).



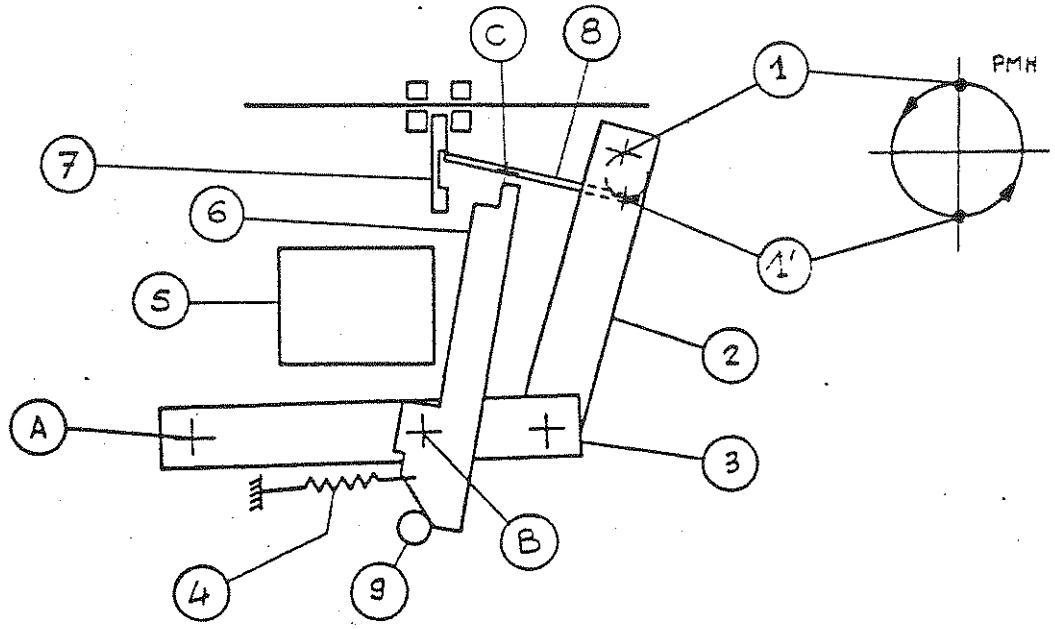
Middle of 1st cycle

- eccentric (1) is in the low position,
- eccentric (1') is in the high position,
- lever (8) bears against the lower part of the groove of punch (7),
- armature (6) bears against the electromagnet (5) under the effect of rod (3) and stop (9).



End of 1st cycle and start of 2nd cycle

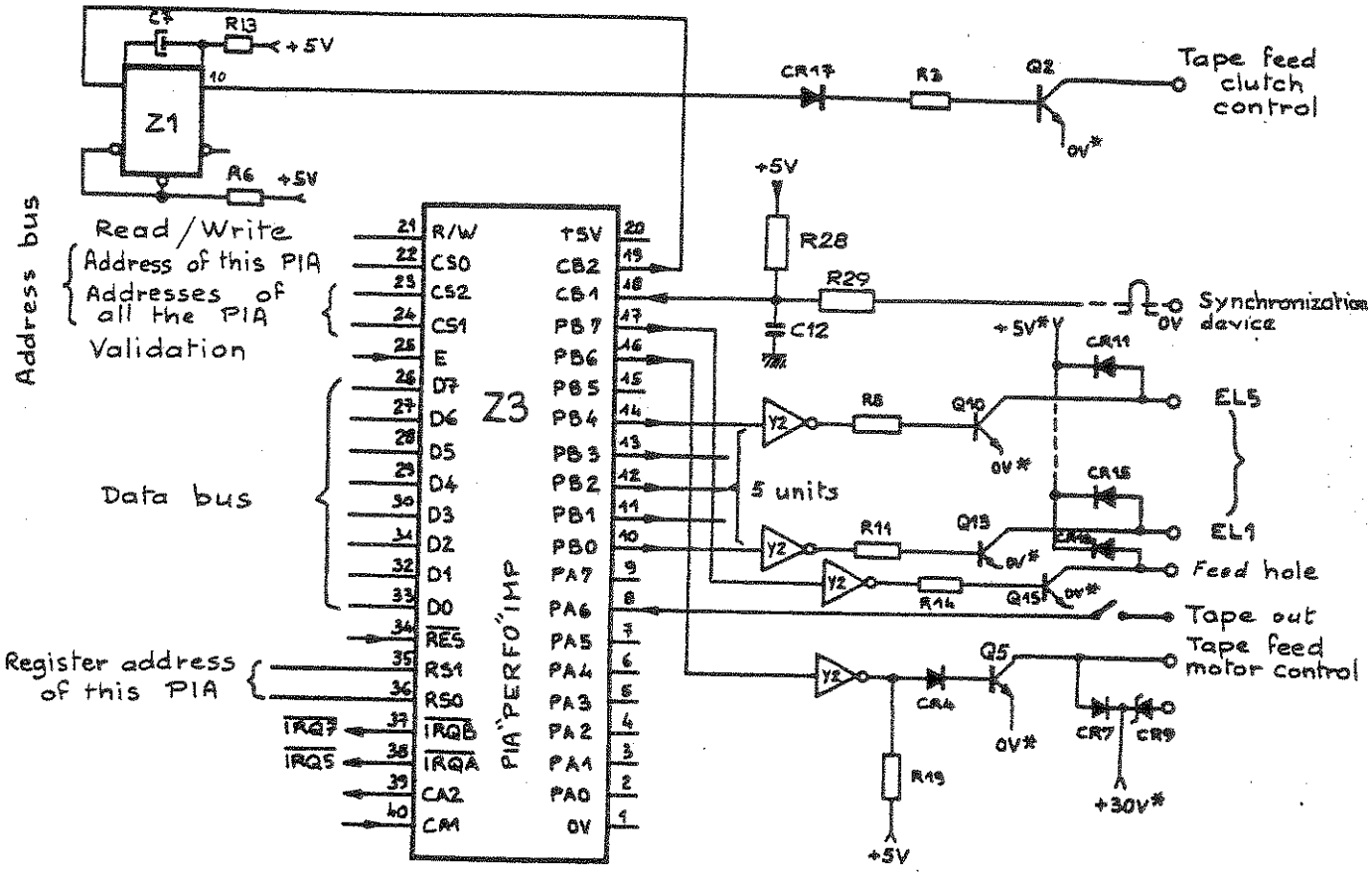
- eccentric (1) is in the high position,
- eccentric (1') is in the low position,
- lever (8) is in the high position in the groove of punch (7),
- armature (6) clears the bottom of punch (7) under the effect of spring (4).



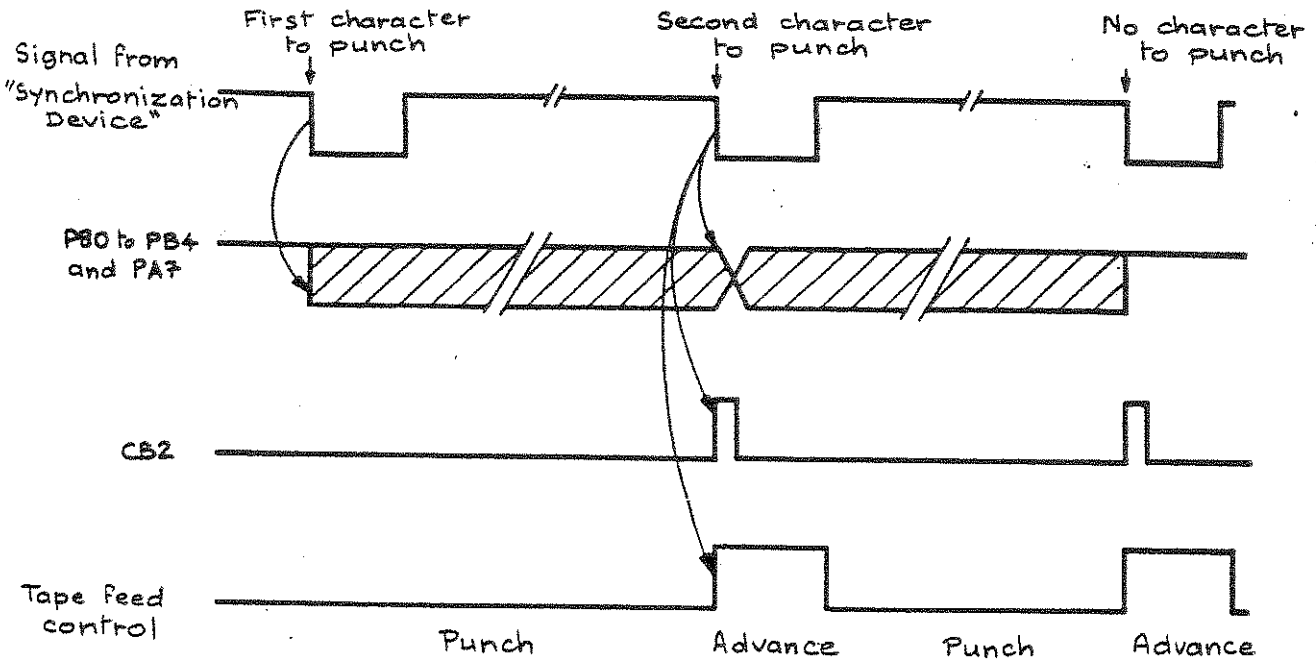
In fact, because electromagnet (5) is not energized, armature (6) is not held against it.

Armature (6) returns gradually to the idle position because it bears against stop (9).

If the "unit" applied to the associated electronic logic requires the punching of a hole, the device will behave as described in the 1st and 2nd cycles with punching, otherwise the middle and end of the 2nd cycle in progress will be identical to those of the 1st cycle without punching.



TAPE PUNCH input-output circuit



Timing diagram of tape feed control

7.3 TAPE PUNCH INPUT-OUPUT CIRCUIT

("PIA PERFO + AMPLI" board)

General

The D-C motor drives a pulley via a belt. The signal used as reference to the mechanics and the electronics of the equipment is provided from a device consisting of :

- soft-iron core integral with the pulley,
- magnet coil,
- processing electronical circuit.

The motor also supplies the energy required for punching the 5-units and the feed hole. The "unit" and feed hole electromagnets are used only for controlling the punches.

The advance control electromagnet releases a ratchet wheel notch by notch used for feeding the punched tape.

Operation of control electronic

The selection of the TAPE PUNCH applies a logic level "0" to (PB6) of the "PIA PERFO + IMP" input-output circuit (Z3). Through inverter (Y2), transistor (Q5) becomes conductive and energizes the motor.

The TAPE PUNCH applies the signals obtained from the "Synchronization device" to the input (CB1) of PIA. The punch and feed hole electromagnets, selected by outputs (PB0 to PB4 and PB7) of the input-output circuit (Z3) are supplied with + 5 V.

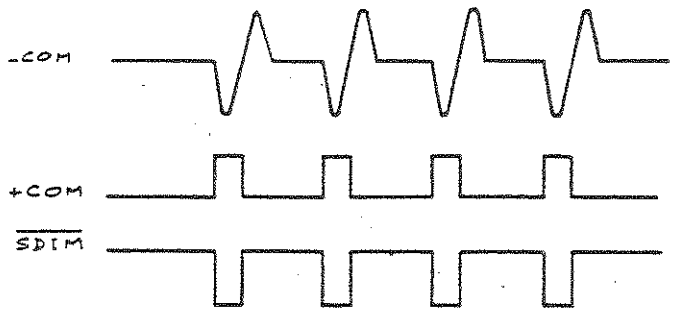
The RC filter (R29-C12) suppresses any interference present while resistor (R28) sets a logic level "1" at the input of the PIA.

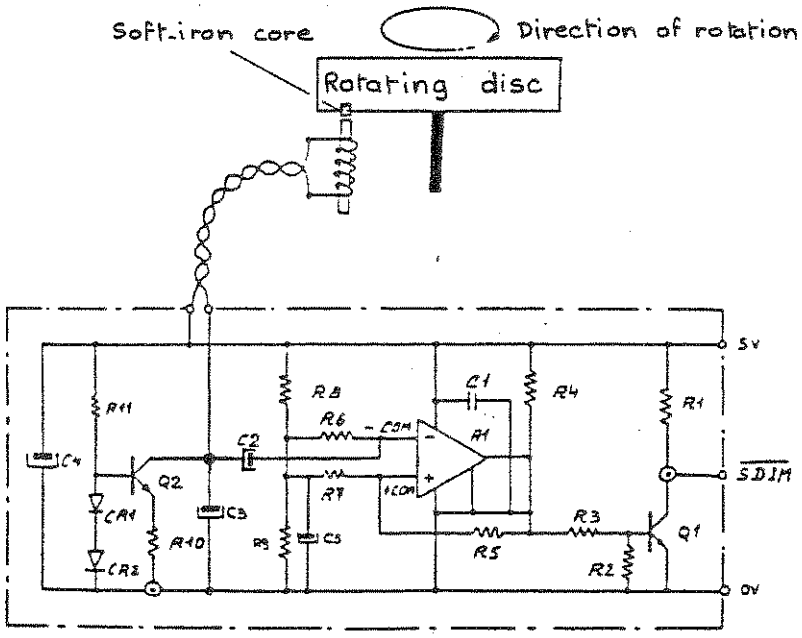
To allow the last punched code to be read before tape feed occurs, monostable (Z1) applies a tape feed control pulse. The monostable is triggered by output (CB2) of PIA if there is a signal present, coming from the "Synchronization device", and if a character was punched during the preceding cycle. (Z1) pulse duration : 3.3 ms (adjusted).

A control switch detects the end of the tape by applying a logic "0" to input (PA6) of (Z3).

7.4 SYNCHRONIZATION DEVICE (TAPE PUNCH)

The magnetic flux of coil carrying an electric direct current varies each time the soft-iron core passes. This results in potential fluctuation at the terminals of capacitor (C3) charged and discharged at constant current through transistor (Q2) connected as a constant current generator. The potential fluctuation at capacitor terminals (C3) is applied on"-COM"input of the operational amplifier (A1) connected as Schmitt trigger through deviator circuit (R6, R8, C2). The resulting signal is then inverted through transistor (Q1).





8 – ABBREVIATED NUMBERING («NUMEROTATION ABREGEE» board)

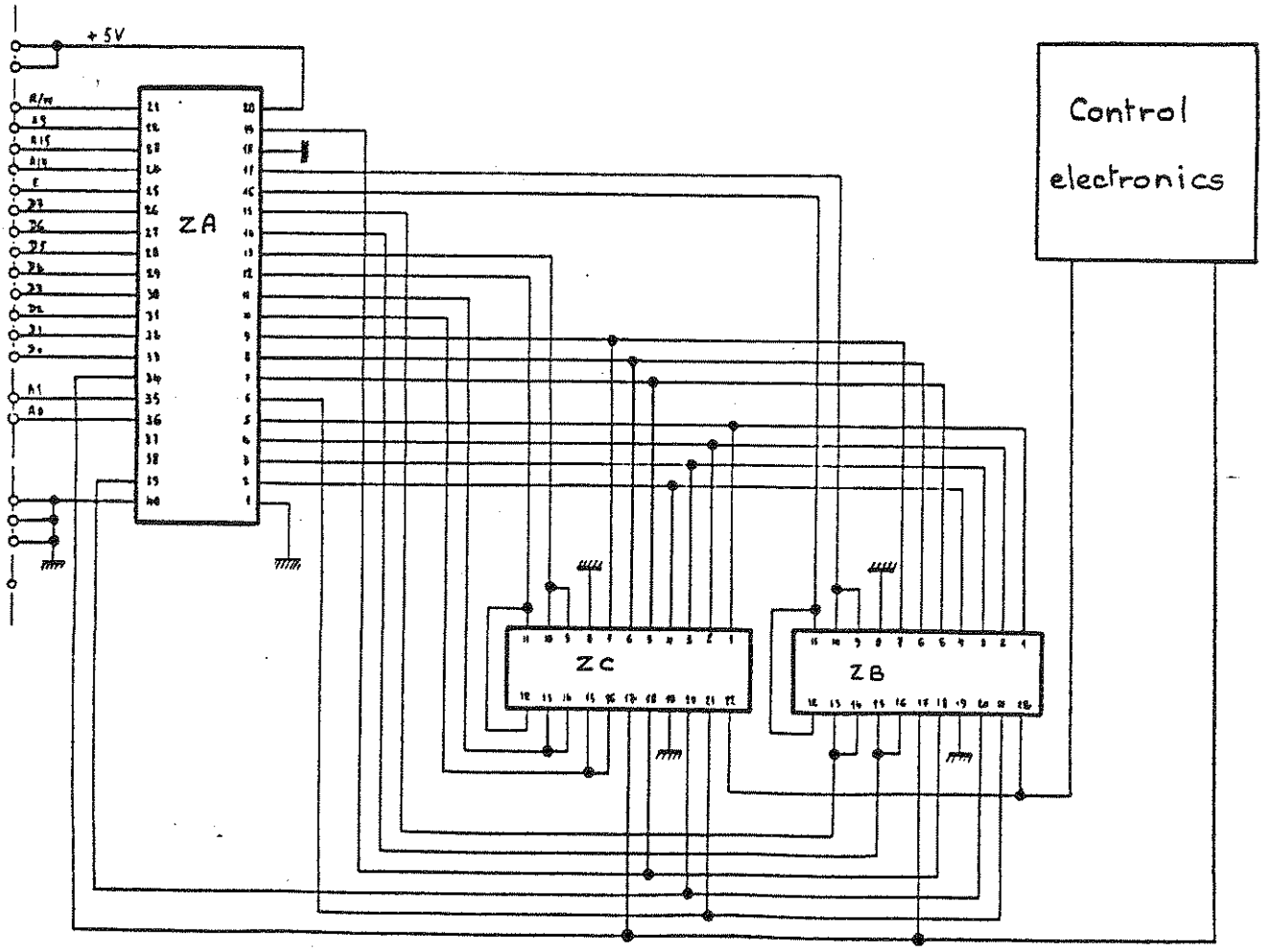
8.1 GENERAL

The "NUMEROTATION ABREGEE" board consists of :

- an input-output circuit (ZA),
- two working memories (ZB and ZC) in which the 10 subscriber numerals are stored,
- an electronic circuit ensuring the following functions :
  - power supply of memories (ZB and ZC) when the power fails or is switched off,
  - initialization on switching on,
  - charging of the accumulator (BT1 and BT2).

8.2 INPUT-OUTPUT CIRCUIT AND MEMORIES

The initialization of the input-output circuit (ZA) at (ZA-34) , the enabling "CE2" (ZB-17 and ZC-17) and the power supply (ZB-22 and ZC-22) for the memories, are ensured by the controls electronics.

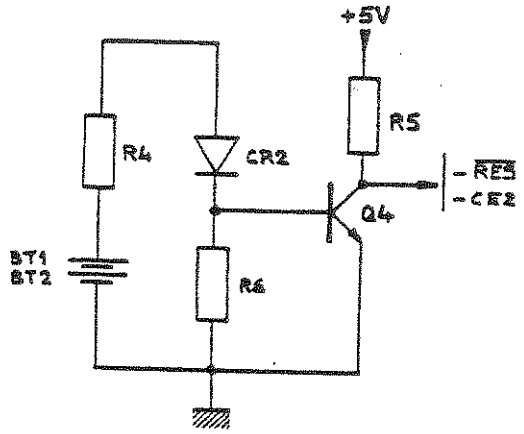


8.3 CONTROL ELECTRONICS

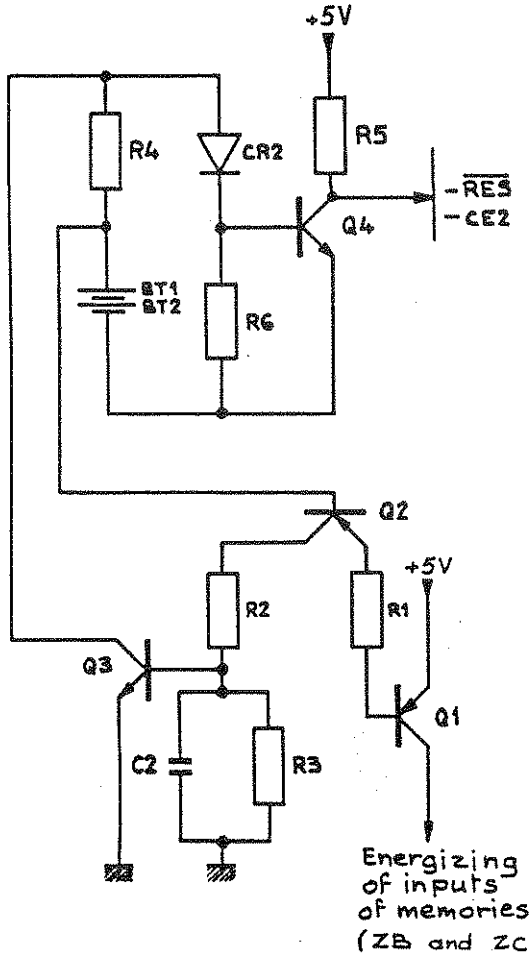
8.3.1 Power supply of memories with unit switched off

In order to preserve the subscriber numerals in the memories, (ZB and ZC) are permanently energized. When the unit is not switched on, the accumulator (BT1 and BT2) energizes the memories (ZB and ZC) via diode (CR1).

8.3.2 Initialization on turning on



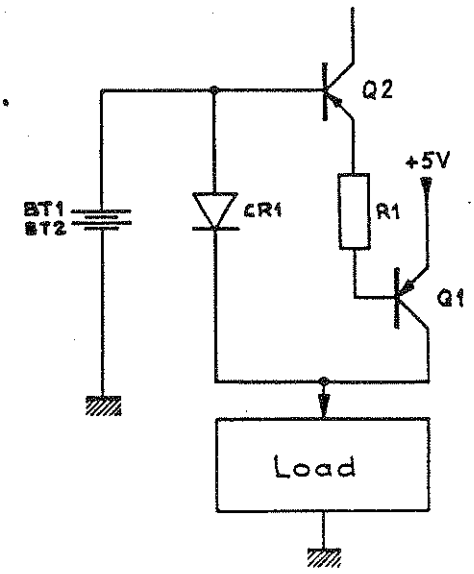
1) Accumulator (BT1 and BT2), through resistors (R4 and R6) and diode (CR2), saturates transistor (Q4) thus causing switching to state "0" on the inputs ($\overline{RES}$) on the input-output circuit (ZA) and (CE2) of memories (ZB and ZC).



2) The + 5 V voltage is established on the emitter of transistor (Q1). Therefore, (Q1) as well as (Q2) become slightly conductive. Capacitor (C2) is thus charged according to the time constant (R2C2) until transistor (Q2) conducts, applying a level "0" to the anode of diode (CR2). Transistor (Q4) becomes blocked thus applying + 5 V to inputs ($\overline{RES}$) of (ZA) and (CE2) of (ZB and ZC) through resistor (R5).

8.3.3 Accumulator charge circuit and + 5 V power supply of the memories

Once initialization is over, transistors (Q1 and Q2) are conducting. Diode (CR1) becomes blocked and the load is supplied by the + 5 V coming from transistor (Q1). Transistor (Q2) charges the accumulator (BT1 and BT2).



9 – POWER SUPPLY
(TRANSFORMER POWER AMPLIFIER 12 V POWER SUPPLY, «ALIMENTATION» and «RAM RPROM» boards)

9.1 MAINS FILTER AND LIGHTNING ARRESTOR "PARAFOUDRE"

The unit has a MAINS FILTER consisting of capacitors (C1 to C5), coils (L1 and L2).

The "PARAFOUDRE" board consists of the three resistors (VDR), the value of which varies according to the voltage applied across their terminals (V1 to V3). They protect the unit against possible overvoltages.